

October 2014

the pcb magazine

AN  PUBLICATION**END
OF
MARKETS
FOR
PCBS**

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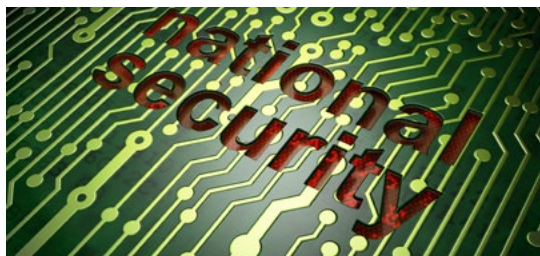
End Markets for PCBs

Our feature contributors have plenty to say about end markets for PCBs this month—from the future of the domestic mil/aero market (looking good!) to wearables, automobiles, very thin PCBs for smartphones, and more!

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NUMBER 10

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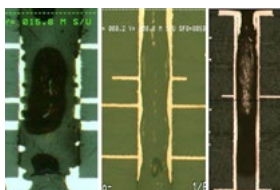


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New Young Voices Finding the Right Tune To Sing

by Ray Rasmussen

I-CONNECT007

The title of my column this month was provided by [Joe Fjelstad](#). It came in the form of a comment at the top of an email he sent to me a few months back. I think it perfectly describes the theme of this column, as does the quote below from an article about the BotFactory:

"The guys at [BotFactory](#) hate to solder. Their eyes start gleaming when they talk about how future generations of their new desktop circuit fabrication platform, Squink, could bring to an end the days of soldering for engineering students and hackers. It's messy. It's hot. They never want to do it again."

I recently came across a quote on the topic of change from Bill Gates, which I believe is quite appropriate as we all try to figure out where this technology is going. Gates said, "We always overestimate the change that will occur in the next two years and underestimate the change that will occur in the next ten. Don't let yourself be lulled into inaction."

Futurist [Ray Kurzweil](#) says this: "If we look at the life cycle of technologies, we see an early period of over-enthusiasm, then a 'bust' when disillusionment sets in, followed by the real revolution."

The market hype associated with printed electronics and 3D manufacturing over the years has suggested that these technologies will be game-changers. The speed at which they're "changing the game," in reality, may lull some folks to sleep as they see PE and 3D more as fads as opposed to new ways of making circuits.

That brings to mind another Kurzweil quote: "Our intuition about the future is linear. But the reality of information technology is exponential, and that makes a profound difference. If I take 30 steps linearly, I get to 30. If I take 30 steps exponentially, I get to a billion."

The Gartner Chart in Figure 1 was pulled from this press release back in August.

In my [June 2013 column](#), I posed the idea that the combination of 3D and PE technologies would create dramatic changes in the industry (more hype?). I suggested that the timing for this convergence (PE and 3D) and the PCB was somewhere in the future. But I don't believe that's the case anymore. Like the second half of Gates' quote on change and Kurzweil's on exponential change, we are likely underestimating what will occur over the next decade; things are changing exponentially.

For me, it's not what the guys at the Botfactory are doing, it's who is doing it. These aren't the industry experts, giant technology companies or huge EMS providers. It's the GenXers. They're by-passing the traditional industries entirely. They've gotten hold of cheap 3D printers along with the materials being developed for printed electronics and they're starting to build PCBs and assemblies. Sure, it is just rudimentary circuits now, but this will change. Think about it:





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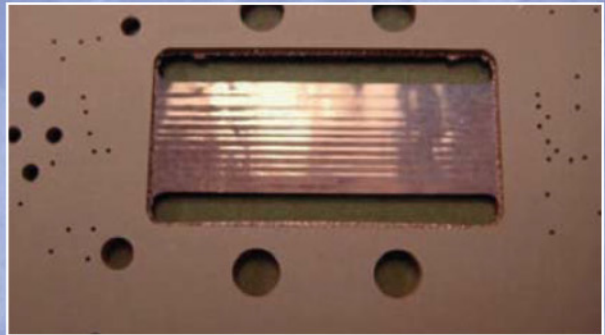
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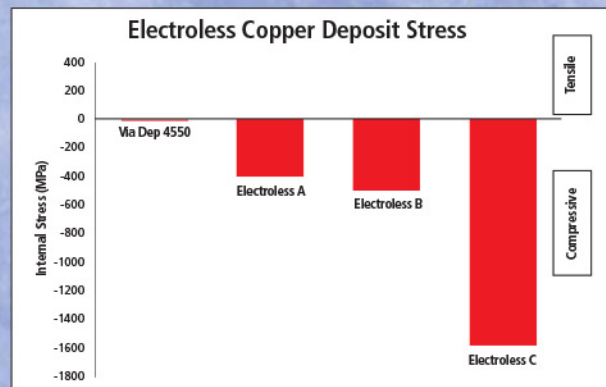
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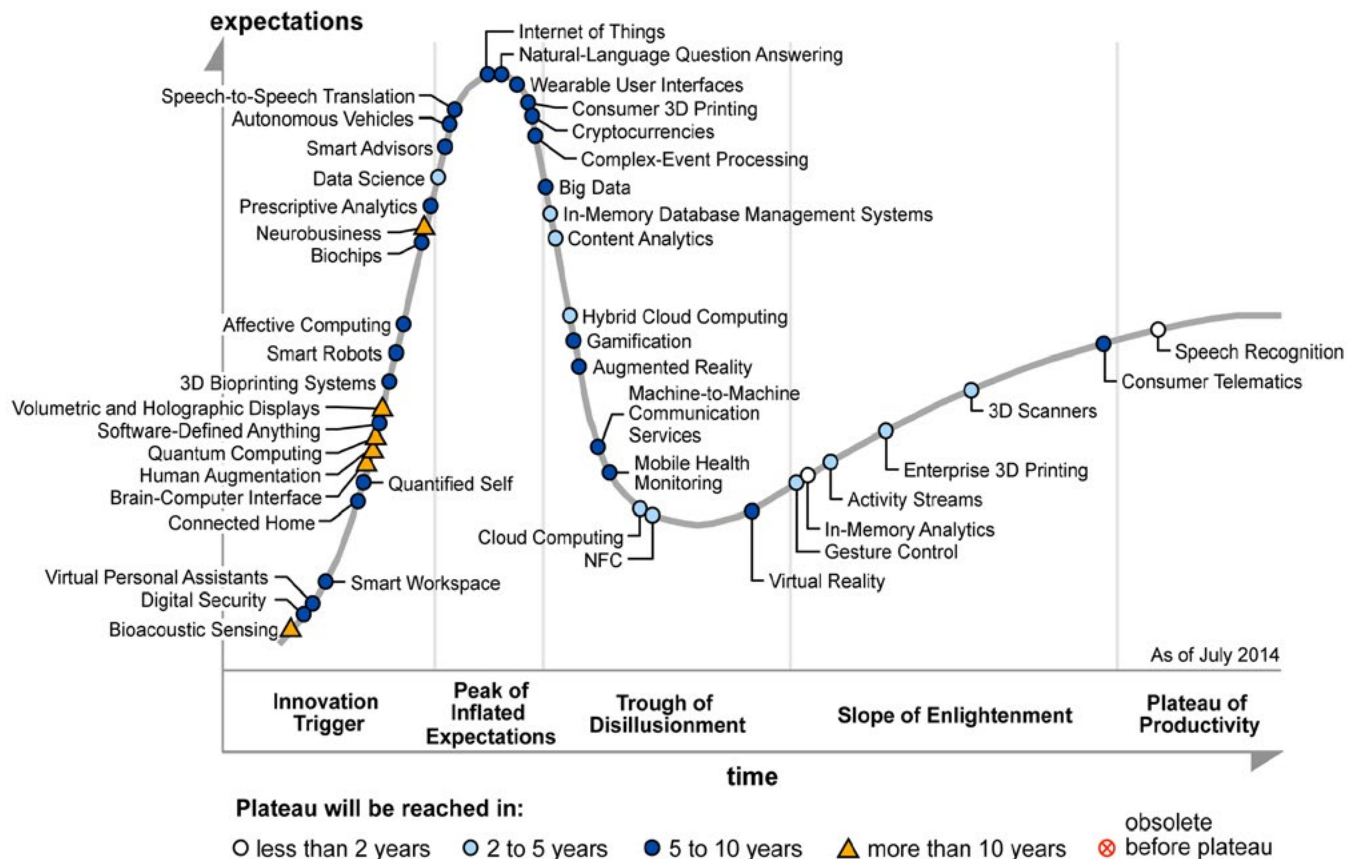


Figure 1.

They're working to topple (they don't realize it, yet) an industry worth a couple hundred billion dollars. If they have some success, they're going to pique the interest of the VC community.

These new circuit makers are in a great position, too, because the large materials companies working to advance the potential of the PE market are doing all the heavy lifting. Those materials and technologies are opening the door for the creative minds fresh out of college. For a few thousand crowd-funding dollars, these next-generation technology entrepreneurs are working to create the systems to build multilayer PCBs and assemblies. There is no doubt they will succeed as the materials and systems they need are being developed at lightning pace by R&D labs from academia, industry and governments around the world, all striving to capture a share of this huge new market.

This stuff is happening all around us, right now. Some of it is making the news, which I've

shared with you in this column in the past and more, today. To add more fuel to this revolution, I recently read that the U.S. government is buying 20,000 3D printers to give to high schools. I'm sure they're doing the same in Europe and Asia. Exponential change is underway.

I'm not frightened by all of this; I'm intrigued and excited. All of those young people we've been unable to attract into conventional PCBs and EMS are now coming. They're doing it in their own unique ways with their own timing. The timing is what we have to keep an eye on. The thing about exponential change is that it tends to blindside most of us. We hear the hype, don't see much happening, then, overnight, we're staring it, whatever it is, right in the face. That's where we are, today. We're exiting the hype cycle, mostly, and entering into a real, new phase of manufacturing based on 3D-PE.

Think of the possibilities. When an OEM can fabricate a PCB and assembly as needed, on the fly... Imagine the cost savings! It's an interesting scenario. But as these systems get dialed in, how do we stay relevant?

Inherent Problems

Having just published another issue of SMT Magazine dedicated to Tin Whiskers, I, like most of you, am dumbfounded by the amount of energy and resources we invest to breathe additional life into these traditional systems. Lead-free has only magnified many of the problems related to traditional solders.

Another welcomed consequence of the addition of thousands of young minds to our industry is that they'll likely provide quick solutions to many of the problems plaguing the reliability of the systems we're building. These simpler (on the surface) systems will require better, lower cost materials. Again, this work is already being done by the globally-interested 3D and PE materials suppliers. Certainly, we can see the day when traditional structures and methods of attaching components will no longer be the norm. There are just too many problems. On the horizon we'll see new schemes to meld functionality into interconnection platforms. Will they be Occam-like or take some other form? Check out what the folks at PARC are doing with embedded components. It's mind blowing: [PARC: 3D Printing Electronic Components Within Objects](#).

Based on what we're seeing, I don't believe the circuits of the future will be more of the same. If you're going to build thousands of PCBs and assemblies using these 3D-PE systems, they'll have to be built on a very reliable platform with the best materials. And with these fresh minds working on the problems, unhindered by 50 years of PCB or assembly experience, I predict they'll come up with some pretty elegant solutions. They aren't going to stick with something that's broken. That's what's really exciting. No legacy systems to deal with, just fresh thinking using cutting-edge equipment and materials.

The Bigger Picture

The PCB industry generates \$50–\$60 billion in revenue today. The PE industry, by some es-

timates, could reach \$300 billion in a decade or so. [IDtechEx](#) predicts a \$77 billion PE industry by 2023 with only about 20% of that related to circuits. If that \$300 million market size holds true it would mean PE circuits could represent about \$60 billion. Now, some of that will be in new PE enabled products, but a portion will come from the PCB segment. And with the new capabilities of 3D combined with PE, along with advances in robotics and the trillion-dollar market forecast for the Internet of Things (IoT), new markets will emerge. Circuits will be everywhere and on everything. Many products won't have a PCB in the traditional sense, but circuits will most likely still connect things.

Here's a question that we should all ponder, going forward: Are we in the PCB fabrication and PCB assembly business, or are we in the circuit making and circuits' assembly business?

Is it Our Industry?

I know some of you might feel like the industry is under attack from PE and now 3D printing, but I see it a bit differently. These technologies are coming whether we like it or not. And the fresh, young minds will invigorate and transform the industry into something new. Now, we can embrace the technologies along with the new entrants or fight them kicking and screaming to the end. I see a ton of opportunity for us all in the former and disaster and demise for us in the latter. I only know of a few PCB and EMS companies that are dabbling in 3D-PE technologies, but I'm sure there are more. I hope my passion for this topic is received as it is intended: to inform our readers as to what I see happening. I certainly welcome your comments. They can be published and shared with the rest of the industry or kept private. Just let me know. **PCB**



Ray Rasmussen is the publisher and chief editor for I-Connect007 Publications. He has worked in the industry since 1978 and is the former publisher and chief editor of *CircuiTree Magazine*. To read past columns, or to contact Rasmussen, [click here](#).

Up, Up, and Away: Reasons for Renewed Optimism in the Mil/Aero PCB Market

by John Vaughan

CIRCUIT SOLUTIONS LLC

In retrospect, the musings of the controversial German philosopher Friedrich Nietzsche would have provided some very accurate foresight had I considered it in the '80s as I embarked on a career in military printed circuit manufacturing: "That which does not kill us makes us stronger."

As anyone who has been in the military circuit board business in the last few decades will attest, it has been both extremely challenging (due to the many obstacles) and wonderfully rewarding (because our collective work supports our country and our war fighters). Along the way there have also been many decisions made by the DoD that have seemed totally misguided, counterproductive to our national security, detrimental to the domestic printed circuit industry and negatively impacted the overall sustainment of our defense industrial base.

The commercial off-the-shelf (COTS) initiative comes immediately to mind.

When I was a young man entering the U.S. printed circuit board industry in 1981, many domestic shops were bustling with activity in support of our nation's military. While the exact numbers are a little hard to pin down, my personal recollection is that there were north of 2,500 domestic circuit shops and hundreds of them were military approved (to the old Mil-P-55110 specification).

Today, there are barely 200 printed circuit manufacturing facilities in the United States. A review of the current Defense Logistics Agency database and Qualified Manufacturers Listing (QML-31032) reveals that as of August 2014 there were a total of 31 U.S. printed circuit fabricators certified to build military circuitry. For accuracy, it should be noted that Sanmina-SCI,



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TTM and Viasystems (recently acquired by TTM) have multiple certified facilities, so the total manufacturing site number is slightly higher.

In the 2005 industry report, [Linkages: Manufacturing Trends in Electronics Interconnect Technology](#), the National Research Council (NRC) determined that U.S. production of PCBs was less than 10% of the world output (whereas it had been more than 40% in the 1980s). Additionally, and for further perspective, according to a 2010 National Defense Industrial Association (NDIA) report, [Recovering the Domestic Aerospace and Defense Industrial Base](#), overall, the U.S. PCB industry shrunk by an estimated 74% from 2000–2010.

In terms of revenue, that same NDIA report defines the significant revenue losses in U.S. domestic PCB output as having reduced dramatically from \$11 billion in 2000 to less than \$4 billion by 2008.

Nietzsche quotes, history and bad news out of the way, there are some real reasons for optimism in the U.S. military and aerospace segments of the PCB industry.

In an earlier *Mil/Aero Markets* column, [Pentagon Budget Aftershocks](#) (The PCB Magazine, May 2014) I provided actionable intelligence for your review as you develop strategies to pursue funded DoD programs and specific opportunities in the RF/microwave sector related to electronic warfare initiatives.

There are also significant legacy PCB opportunities outlined in a prior column, [Foreign Military Sales: Back to the Future for Sales Opportunities](#) (The PCB Magazine, March 2014).

To obtain more current information specific to the military and aerospace market, I reached out in mid-September to Sharon Starr, Director of Market Research at IPC, whom I consider the foremost industry authority in defining actual market conditions.

According to Starr:

“IPC estimates that the military and aerospace market for PCBs accounts for about 28% of the North American PCB market. This estimate is based on 2013 data collected from the industry and published in [IPC’s 2013-2014 Analysis & Forecast for the North American PCB Industry](#), which will be published later this month. This represents at least \$965 million.

IPC’s bottom-up method of estimating the size of the market produces a conservative estimate.

Sales growth for rigid PCBs in North America has been basically flat so far this year, with year-to-date sales to the mil/aero market down slightly as of July, while rigid PCB sales to other markets are up compared to the same period last year. The flexible circuit segment is seeing modest growth so far this year. As of July, mil/aero flex sales are outperforming sales to other markets. This information is from the September edition of IPC’s North American PCB Market Report, which is published monthly.”

(For a deeper dive into the growth potential for flexible circuits, please see the November 2013 column, [The Intersection of Unmanned Vehicle Systems and Electronics Technology](#).)

Therefore, through my interpretation of the data, a minimum of nearly \$1 billion of U.S. military and aerospace printed circuit manufacturing business will be available in 2015. For clarification, all of these opportunities would not be purely Mil-31032 requirements and would also be comprised of IPC Class 2 and Class 3 builds, effectively opening up the market for all U.S. based facilities that are ITAR registered and are certified to manufacture to IPC requirements.

More importantly, and to provide an opportunity for military and aerospace PCB growth sustainment and future growth, as we near the close of 2014 there have recently been two dramatic and long overdue legislative developments driven by the IPC that will positively impact the U.S. domestic PCB industry, particularly the military/aerospace sector:

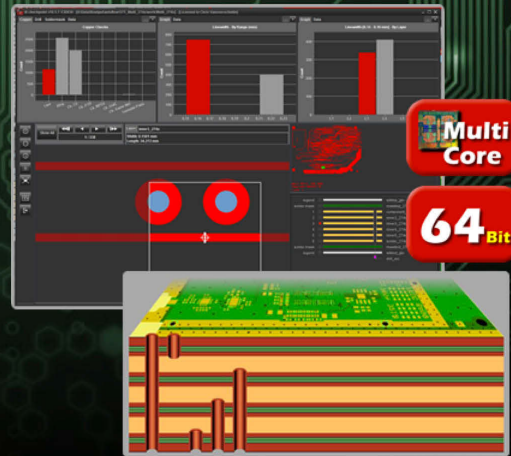
- On July 1, 2014 the U.S. Department of State published [a final rule for Category XI for Military Electronics](#) of the United States Munitions List (USML). This clarifies the treatment of PCBs under International Traffic in Arms Regulations (ITAR). The new rule states that PCBs “specially designed” for defense-related purposes will be controlled under USML Category XI. Additionally, any designs or digital data related to the “specially designed” PCBs will be controlled as technical data. This is a significant victory for the IPC and its members, who have long advocated that PCB designs should remain under the jurisdiction of ITAR when the end

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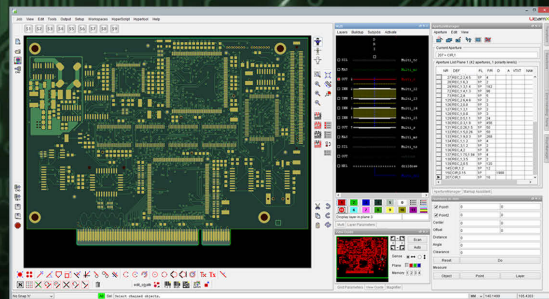
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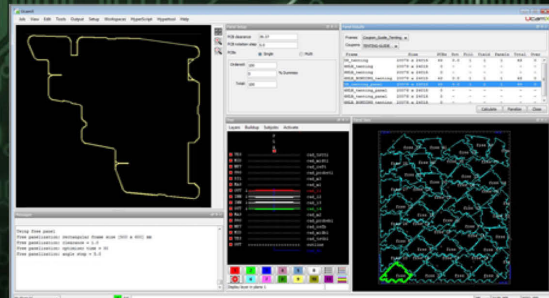
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item for which the board is designed is a USML item. This action provides a clearer standard for contractors who design, manufacture or source PCBs for military use. To learn more about the final rule, visit www.ipc.org/export-controls.

- On September 16, 2014, the [U.S. House of Representatives passed the Revitalize American Manufacturing and Innovation \(RAMI\) Act](#) with an impressive number of 100 co-sponsors, 50 Democrats and 50 Republicans. Also a top policy priority for IPC, RAMI provides an opportunity to grow advanced manufacturing in the United States through federal investment. The U.S. Senate is considering its version of the RAMI Act, introduced by Sens. Sharrod Brown (D-OH) and Roy Blunt (R-MO). If enacted into law, the RAMI Act will establish a National Network for Manufacturing Innovation (NNMI).

The bill has passed the Senate Commerce Committee and is awaiting a floor vote, with the hope that the Senate will pass its version before Congress adjourns this year. To note, there are already four NNMI in existence and the RAMI Act would add others. To that end, there is an active Request for Information (RFI) to industry by the DoD relative to the next NNMI selections. The purpose of the RFI is to solicit input from industry and academia that the DoD will consider as part of an effort to select and scope the technology focus area for future NNMI centers known as Institutes for Manufacturing Innovation (IMIs). The DoD is requesting responses that will assist in the selection of a technology focus area from those currently under construction, based upon evidence of national security requirement, economic benefit, technical opportunity, relevance to industry,



Figure 1: In June, IPC executives met with President Obama's senior advisor on manufacturing policy to offer support for the NNMI.

business case for sustainability and workforce challenge.

The technical focus areas currently under consideration as the next NNMI's are: flexible hybrid electronics, photonics, engineered nanomaterials, fiber textiles, electronic packaging and reliability, and aerospace composites.

For electronics professionals, several of the NNMI's under consideration are clearly in our industry's wheelhouse, and you are encouraged to get active in the process. See my July 2014 summary of the IPC Executive Committee's meetings on Capitol Hill in the July 2014 issue of The PCB Magazine: [IMPACT 2014: IPC on Capitol Hill—Leadership in Promoting a Strong Manufacturing Economy](#), and to learn more about the sustained IPC effort that has resulted in the legislation referenced earlier and how to become involved in future efforts.

In my opinion, we are stronger for all that we have survived as an industry together, and the tide has now turned as PCBs that are de-

signed specifically for defense systems must now be manufactured in the United States and are under full ITAR and USML controls. The House and the Senate recognize the value of creating advanced manufacturing centers in the United States that are private/public/academia partnerships to drive innovation, and U.S.-based electronics OEMs are increasingly reshoring manufacturing opportunities to the U.S.

Enjoy the ride up, up and away; it has been a long time coming. **PCB**



John Vaughan is president of Circuit Solutions LLC, based in the Washington D.C. Metro Military market and providing integrated supply chain and program management solutions to the military C4ISR, Unmanned Systems and IED detect and defeat communities. To reach Vaughan, or to read past columns, [click here](#).

VIDEO INTERVIEW

Military Market Overview

by Real Time with...IPC APEX EXPO 2014



Regular columnist and this month's Cover Feature contributor John Vaughan discusses the state of the mil/aero market with Guest Editor Judy Warner.



realtimewith.com





Wearable Electronics Driving the Need for a New Level of Systems-in-Package Performance

by **Desmond Wong and Bill Burr**
TRANSSIP INC.

Impending limitations on the ability of planar interconnects to continue to satisfy the expectations created by Moore's Law are driving innovations in packaging technologies which in turn are enabling new applications to emerge. While wearable electronics have been with us for decades in the form of increasingly functional athletic devices and medical monitors, the missing link has been the ability of these devices to transmit information to a remote receiver in real-time. Developments in digital radio driven by the cellphone industry and the subsequent revolution in packaging in response to the need for miniaturisation of RF/wireless functionality are opening up a whole new range of applications. These applications

are set to skyrocket as semiconductor and packaging technologies enable smaller size, lighter weight, longer range, and higher efficiencies. One of the most promising blends emerging technologies for engineered materials with 3D embedded SiP, transcending the conflict between miniaturization and high performance typical of conventional materials.

Introduction

As electronics have become lifestyle items, first in the form of cellphones and subsequently tablets and an expanding range of devices, the functionalities required by this evolution no longer necessarily scale according to Moore's Law. The added value perceived by the end customer is seen in many different ways. This suggests that miniaturization itself is no longer the sole vector, but that a complementary approach is emerging which combines functionality and

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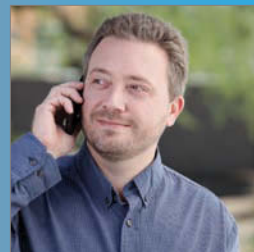
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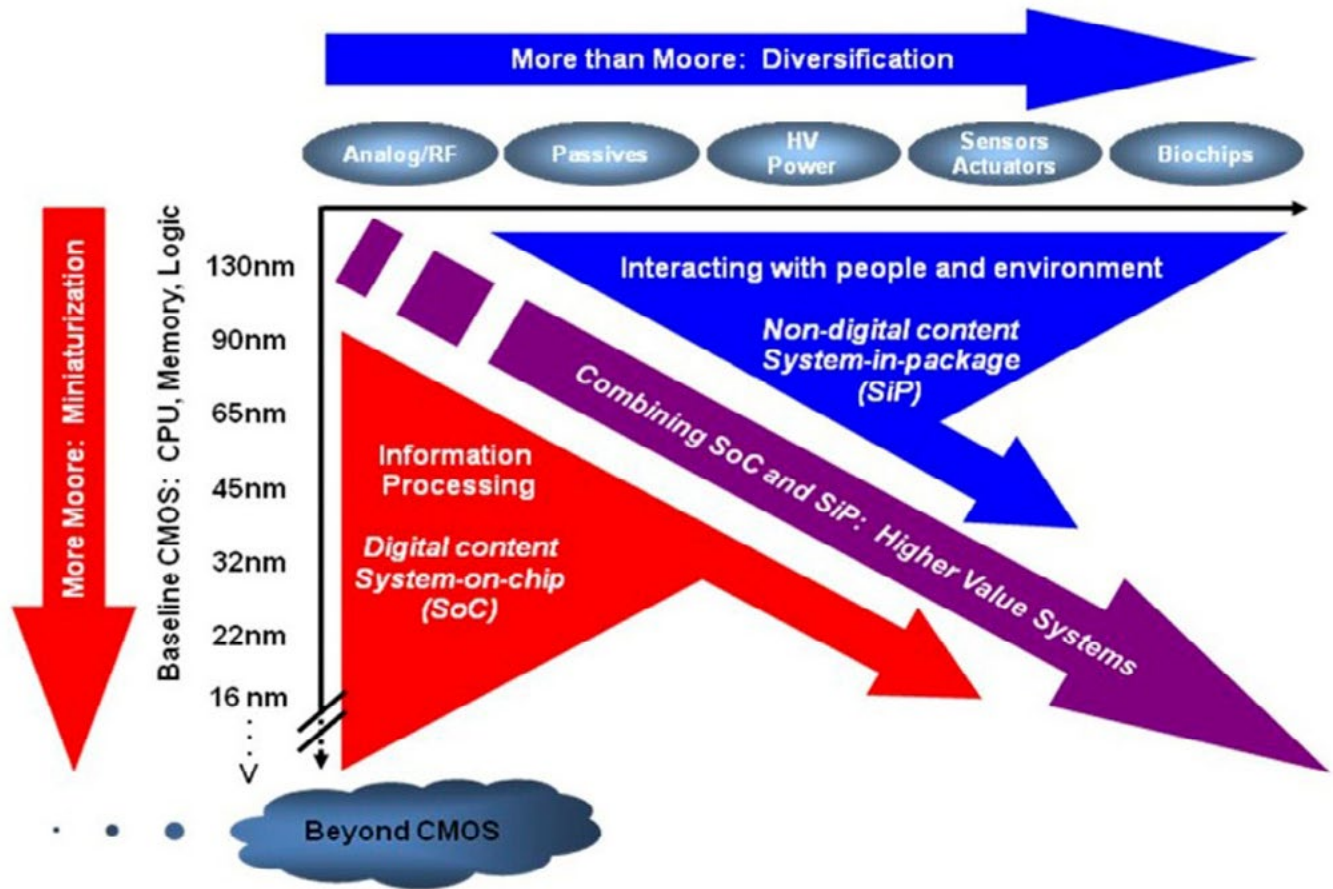


Figure 1: Dual vector relationship driving packaging evolution. (source: ITRS)

form factor in a relationship which is becoming known as “More than Moore” (Figure 1).

The horizontal vector of diversification is characterized by interaction with other people, things, and the environment, and for this to occur in a satisfactory manner the device must be capable of wireless communication. The miniaturization of function and proliferation of advanced packaging solutions which are now providing more silicon area than the area of the motherboard they sit on are offering the key to emergence and growth of a new applications opportunity: wearable electronics.

Wearable Electronics: A Need for Interaction

Wearables are a distinct category of devices, separate from mobile/portables or implants. They’ve been around for a long time in the

form of cardiometers for athletics and heart monitors for outpatient monitoring. Originally the information generated by these devices was stored onboard, if at all, and downloaded through either a cable or infrared connection to a computer.

One of the first forays into the separation of sensor and storage via a wireless connection was the tie-up introduced about 10 years ago between Apple’s iPod and an accelerometer about the size of a quarter placed in a special cavity in a Nike running shoe. The impact of the runner’s foot caused signals to be sent to the iPod and the generated data could then be uploaded to the internet via a host computer.

This early configuration has been followed by an increasing number of devices designed to send information to a nearby receiver. The most common configuration is an enhanced

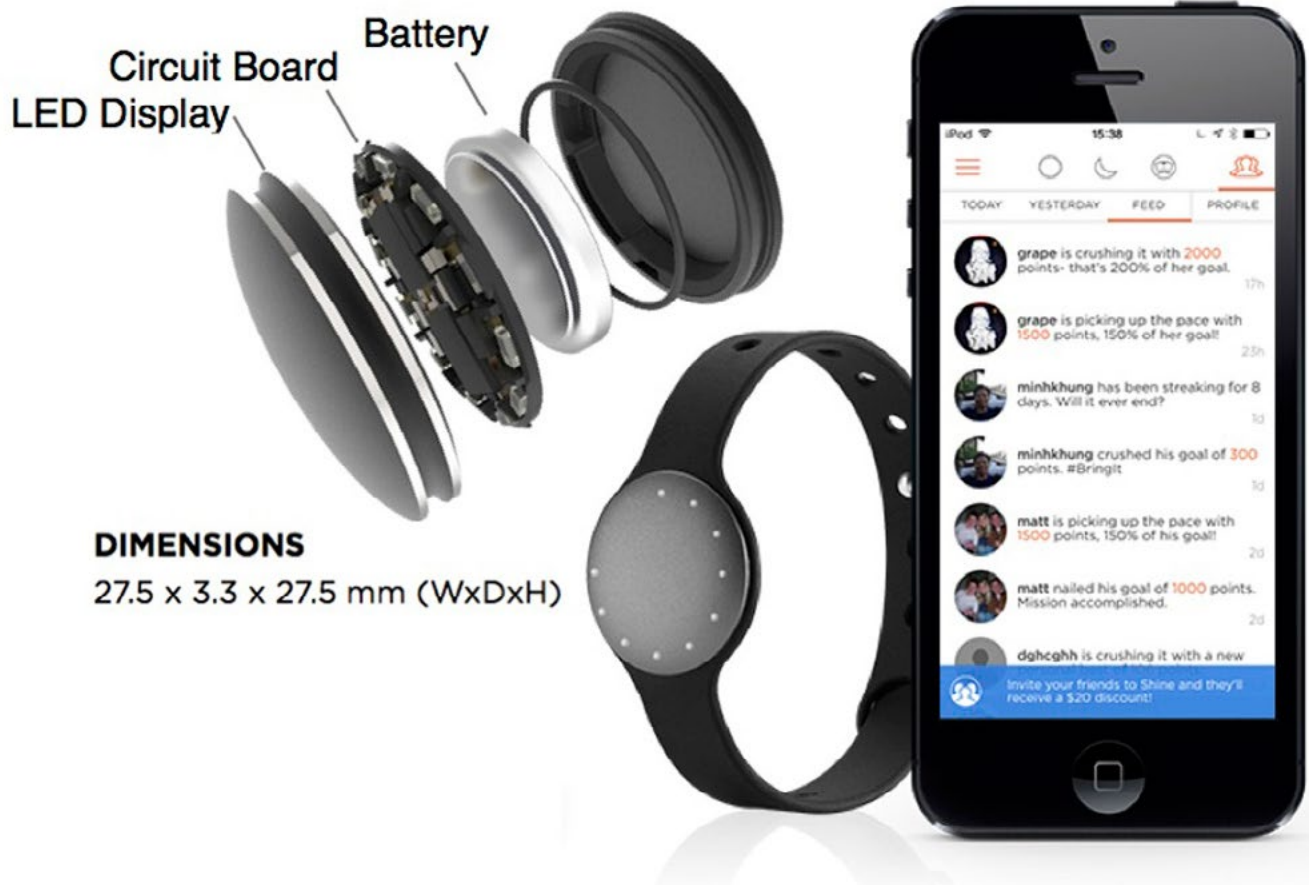


Figure 2: Fitness tracker/sleep monitor. (source: TransSiP, MisFit Wearables)

Bluetooth (BLE) connection to a smartphone as shown in Figure 2. However, the drive is on for greater range and longer battery life, and this combination not only represents the potential for completely new applications for wearables, but also is presenting the need for higher forms of integration compared to the conventional PWB/discrete component approach.

One of the major issues facing team/contact sports in the USA today is the long-term effect of concussions and sub-concussive head impacts. The impact of a soccer header is on the order of magnitude of a hard punch (there's no knock-out because the effect of the punch is magnified by the ganglia in the jaw, whereas a header utilizes the thick bone and relatively insensitive areas of the forehead/skull), and the evidence is growing that neurodegenerative diseases linked to dementia, memory loss and depression are

triggered by repetitive head trauma. The number of people playing sports with high concussion rates such as soccer, basketball, rugby, American football, and ice hockey is over 700 million worldwide, and the best way to minimize the exposure these athletes have to brain injury is to identify a concussion once it has been sustained and allow the individual proper rest to recuperate, as well as reduce exposure to repetitive low-impact (sub-concussive) events through detection and consequent modifications of technique and athletic conditioning.

The devices coming onto the market to address this need consist of an accelerometer capable of responding to multiaxis movements of the head and supporting electronics. While some systems simply trigger an alarm on the headset, more advanced designs store data for wireless transmission to a base station such as

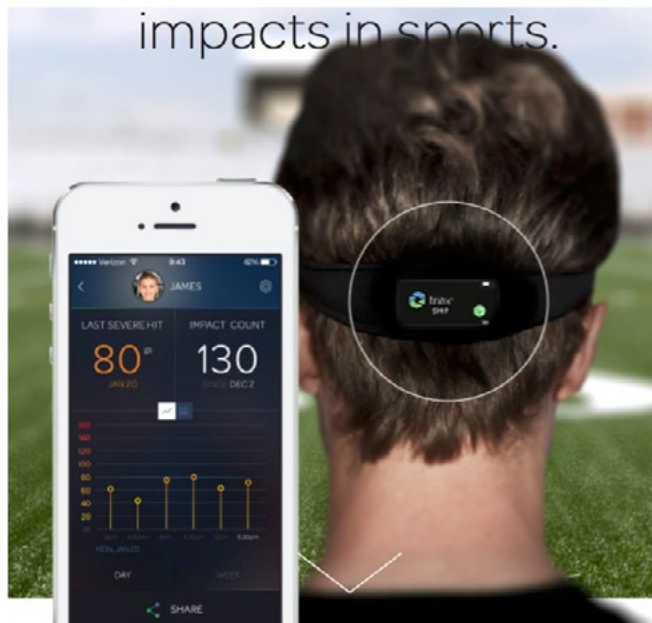


Figure 3: Sports impact detection system.
(source: Triax Technologies)



Figure 4: Apple's computer on a chip.
(source: Apple)

a smartphone. Since the athlete is wearing the sensor, size and weight are of primary concern. Most systems consist of helmets or skullcaps, while one supplier has succeeded in miniaturising the electronics to the point where everything is contained in a headband (Figure 3) and transmitted to the sidelines.

While first-generation systems are attracting a lot of attention it is clear that longer range and/or alternatives to BLE such as WiFi will enhance functionality and effectiveness, giving the coach or trainer realtime feedback on traumatic stress events. Diversification and short product introduction cycles will tend to exclude highly integrated solutions such as system-on-chip (SoC) unless a custom processor platform can support an upgradeable software defined user experience as in the case of Apple's recently introduced Apple Watch (Figure 4). In addition, an integrated packaging (chip scale, wafer level)-on-PCB approach not only tends to introduce parasitics at RF frequencies but is also limited to the specifications and performance of the individual components which make up the circuit.

New developments incorporating a novel approach to managing the electromagnetic properties of materials are set to change this paradigm.

Engineered Materials + System-in-Package = "Better than Book"

One of the bottlenecks in the design of small, interconnected devices is the antenna. Wireless connectivity is the de facto standard for data storage and transfer, with 900MHz, 1.5GHz, and 2.4GHz the most popular spectra due to the massive proliferation of ISM (industrial/scientific/medical) band devices, GPS, BLE, and the various flavors of Wi-Fi. However, wearable is a distinct category that requires new attention in integration technologies. Applying portable or mobile electronics techniques to antenna and RF design has been shown to provide suboptimal performance, primarily due to the much smaller geometries necessary for wearable transceivers.

For example, users of wearable GPS devices have probably noticed that the time to first fix (TTFF) is always long. For wearable wireless con-

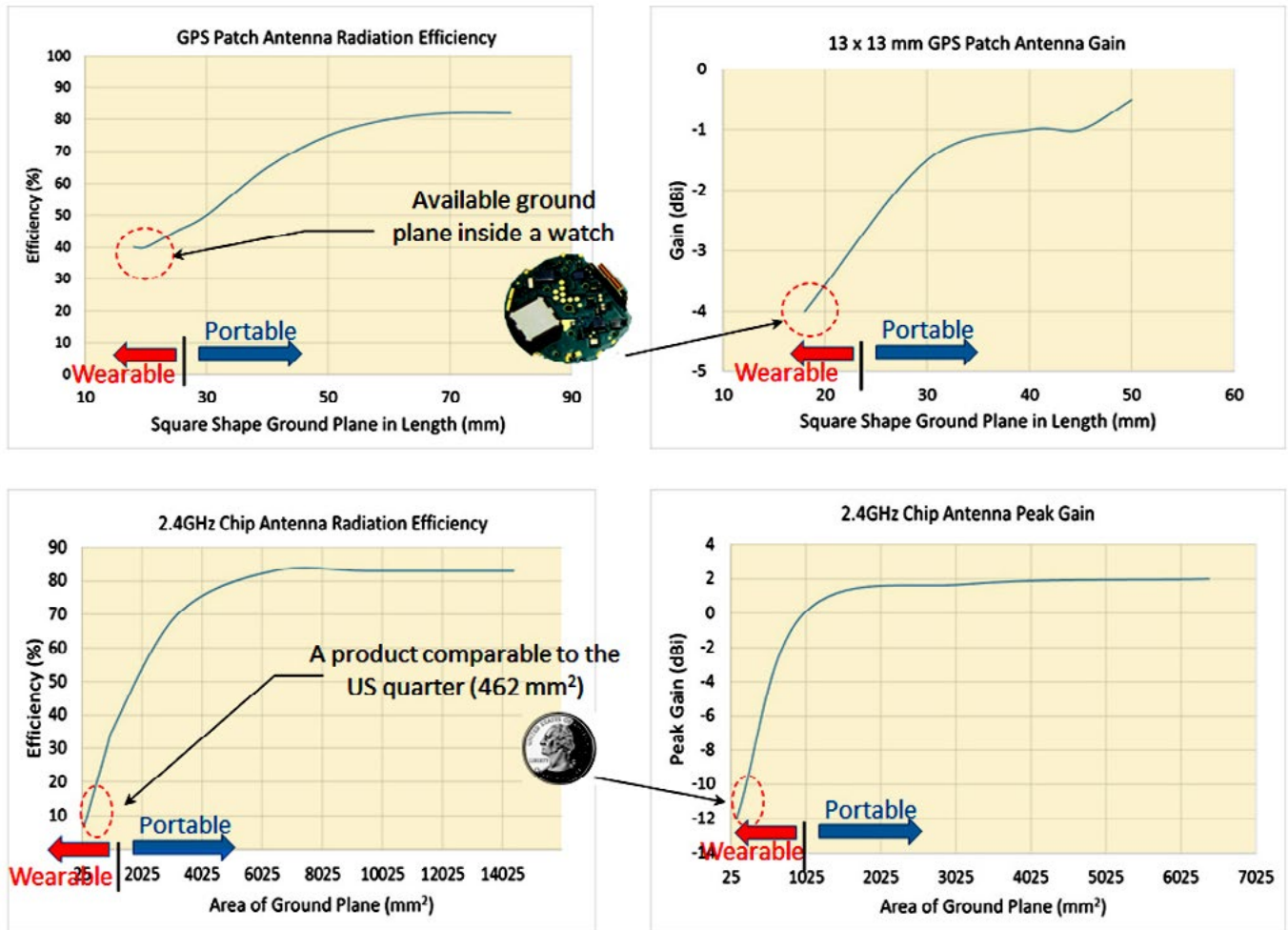


Figure 5: Comparative antenna performance vs. ground plane dimensions. (source: TransSiP)

nectivity, devices usually don't connect beyond a few meters and the connectivity becomes intermittent with increased distance and body movement. In some popular fitness trackers the range is actually only a few centimeters.

The reasons behind this have to do with antenna theory, but basically electromagnetic energy is not radiating from the source and propagating to the far-field (receiver) with enough energy to induce current and voltage in the receiver circuit, primarily because the efficiency and gain of an antenna are dependent on antenna physical dimensions and electrical characteristics for a given output power level. For wearable electronics, the physical dimensions are limited to within a form factor about the size of a quarter (24.3 mm diameter, Figure

2), and the red circles seen in Figure 5 show that, using conventional FR-4 materials and antenna design, both efficiency and gain drop way off at small sizes. This problem is much less evident at the larger dimensions possible inside mobile/portable devices such as smartphones, tablets, and laptops. But once the form factor becomes wearable and the antenna ground plane is limited to 13 x 13 mm or less, it is a different story.

A California startup is taking a novel approach. In this patent-pending process, microscopic structures are used to create "engineered materials" in a 3D embedded SiP solution incorporating coreless/anylayer technology providing electromagnetic band gaps in a wide range from a few hundred megahertz to

	FR-4	TransSiP M3iP
Ground plane size	13 x 13	13 x 13
Radiation efficiency	40%	82%
Gain	-4dBi	1.3dBi

Table 1: Comparative results: GPS patch antenna.

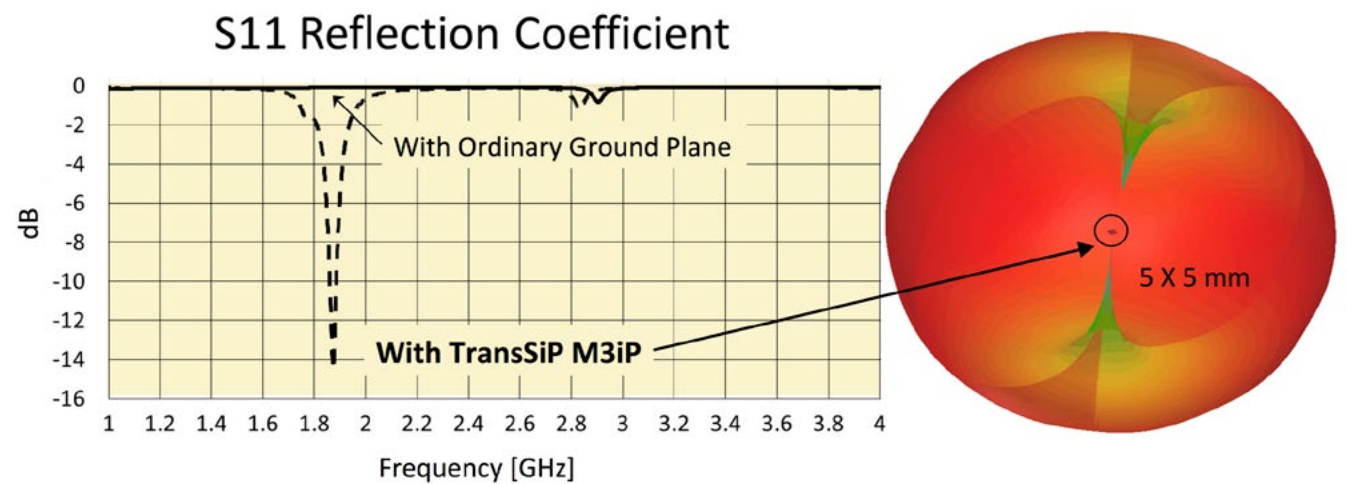


Figure 6: Radiation field and resonance for a 5 x 5 mm AiP. (source: TransSiP)

over 3GHz. This feature coupled with the well-known advantages of embedded SiP improves transceiver gain and efficiency as shown in Table 1.

These results can be further extended with modifications to the engineered materials. A 5 mm x 5 mm printed PCB antenna gave results shown in Figure 6. Without any ground plane extensions that would increase the overall footprint of the device, well-defined resonance was achieved at about 1.9GHz. This opens the door to either AiP (antenna-in-package) or antenna miniaturization in a product no larger than a U.S. quarter.

The TransSiP 3D embedded structure is shown in Figure 7. The process uses B2it technology to enable co-lamination of subassem-

blies during the embedding step, while build-up layers can be done using either B2it or the ALIVH-type variants, or lase-and-plate sequential processes.

Either way, the benefits of embedding combined with any-layer buildup technologies are seen in:

- improved routing flexibility for high speed lines with specific voltage referencing and shielding requirements
- reduced crosstalk between vias due to flexible via placement and shorter barrel length
- reduced parasitics due to lower via inductance
- improved impedance matching around via

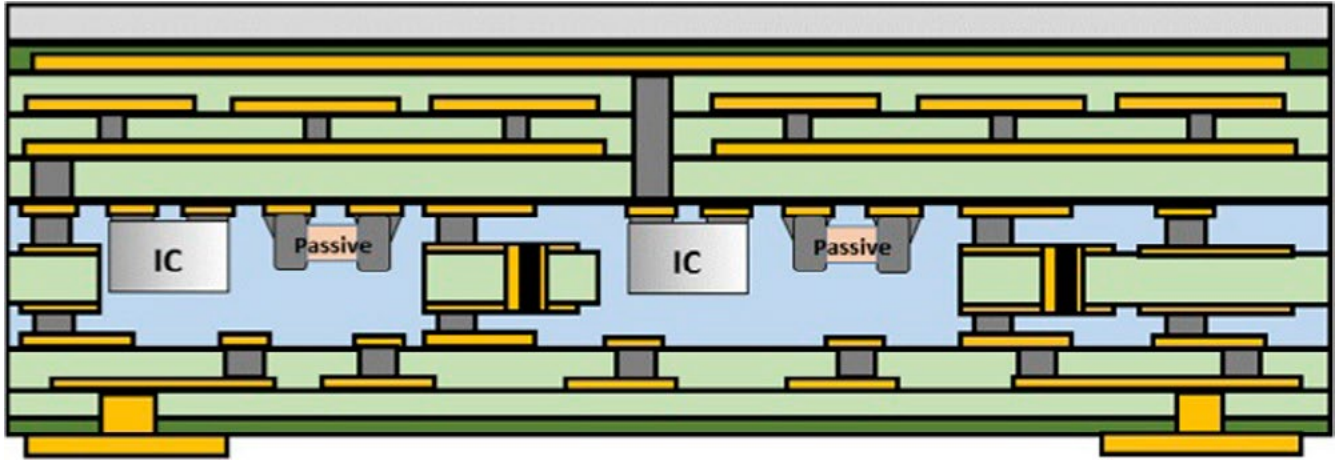


Figure 7: TransSiP 3D embedded SiP.

- lower power delivery network (PDN) self-impedance due to reduction in overall thickness of substrate
- lower loop inductance due to thinner substrate
- lower voltage drop/shorter run lengths
- thin dielectrics offer possibility for reduction/elimination of decoupling capacitors
- surface wave effect suppression due to high impedance surface
- increased small antenna efficiency with consequent increase in range and battery life
- overall smaller footprint/weight/volume for wireless radio

Conclusion

The potential of wearable electronics is proportional to the ability to provide the functionality outlined in the “More than Moore” concept—the need for interactivity with others, with things, and with the data environment. Improved efficiency and range will open up applications such as the impact sensor, or a whole host of remote monitoring systems that simply don’t exist today.

The key to greater efficiency and range is a departure from the radio and antenna technologies which up to now have worked well as portable devices have scaled from the dimensions of a small briefcase/handset to the ubiquitous

smartphone. The next step to a true, wearable device involves another order of magnitude scaling (about 30x, compared to an iPhone), and at that point conventional planar antennas as well as planar designs in general start to run out of gas. Just as the semiconductor industry is pushing the boundaries of physics in the attempt to cram more into smaller and smaller volumes, the radio transceivers which form the backbone of the wireless world must be shrunk to dimensions compatible with the devices they will be housed in. TransSiP has found a way to transcend the physical and electromagnetic limitations of conventional materials with the potential to enable the development of truly interactive wearable electronics. **PCB**



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William (Bill) Burr is owner and principal of LPC Ltd, senior consultant with BPA Consulting Ltd (UK), and currently collaborating with TransSiP, Inc. as a senior advisor. He may be contacted at w.burr@transsip.com.

Security

New Regulations Clarify U.S. Export Controls for Defense PCBs

by Fern Abrams
IPC

On July 1, 2014, the U.S. Department of State issued a final rule for Category XI (Military Electronics) of the United States Munitions List (USML). The new rule states that PCBs “specially designed” for International Traffic in Arms Regulations (ITAR) covered defense articles are controlled under USML Category XI. This is a significant win for IPC members in the U.S. who have advocated for the specific enumeration of PCBs on the USML to clarify and highlight the importance of export controls on PCBs for defense articles.

Why the Change was Needed

It is widely understood within our industry that printed boards for ITAR items are sometimes inappropriately sourced from non-ITAR facilities without necessary export licenses. It is believed that, with few exceptions, non-compliance is a result of genuine unawareness of the law, as it pertains to printed boards manufactured for ITAR-controlled defense items.

Confusion over the application of ITAR to PCBs stems from two main sources. First, because defense equipment itself is often not exported, some manufacturers falsely believe that export controls don’t apply. This is simply not true. Because one must “export” designs and other intellectual property in order to manufacture PCBs

outside the U.S., export controls do apply if the boards are destined for ITAR-controlled defense items.

Second, many manufacturers are confused by the historical regulation of PCBs as parts and components that are “specifically designed” for USML listed items. The ambiguous regulation of printed boards—on the USML under a catchall pertaining to “specifically designed” parts and components—has led to widespread confusion, especially among those responsible for sourcing printed boards who don’t understand that each PCB is uniquely designed for its end item.

Because PCBs historically were not enumerated on the USML, understanding their regulatory status required an understanding of both ITAR and the unique nature of PCBs. The previous law was clear only to those who understand both ITAR and the specially designed nature of printed boards. If a person mistakenly believes—as we have found many do—that printed boards are commercial-off-the-shelf components, then that person might believe printed boards are not covered by ITAR.

ITAR Protection of PCBs is Critical to National Security

The sourcing of PCBs for ITAR electronics from non-ITAR facilities is a threat to national security. In order to manufacture a PCB, the manufacturing facility must be given designs and other sensitive information about the workings of the

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ITAR-controlled defense article into which it will be installed.

Printed boards are essential to many defense systems. Specifically and uniquely designed for each and every one of those systems, printed boards are used to mechanically support and electrically connect electronic components. Printed board designs reveal critical information about the board as well as about the devices for which they are designed. Accordingly, clear and appropriate protection of printed board designs for USML items is needed to safeguard, from U.S. adversaries, inherently sensitive information about both PCBs and their associated U.S. weaponry and military equipment.

From the designs for printed boards to the boards themselves, significant information can be learned about the workings of the item for which the board is designed. For example, PCBs designed for IED jammers help determine radio frequency and range capability. Access to the design of these PCBs would provide an understanding of the jammer and how to circumvent it, leading to greater U.S. casualties during military engagements.

In sum, printed boards—the central nervous systems for all electronics—hold valuable and specific information about the workings of the underlying defense articles themselves. Companies with access to the designs of printed boards for defense articles thereby also have access to sensitive information about controlled technologies. This exposes these technologies to malicious intrusion by U.S. adversaries that may destroy the reliability of U.S. weaponry and other critical defense equipment. Failure to properly secure the information embedded in printed boards that are custom-designed for defense articles could result in a breach of national security, theft of critical defense-related intellectual property and allow for reverse engineering of critical defense systems.

The Need for Export Control Reform

In August 2009, the Obama administration announced a comprehensive review of the U.S.

export control regime in an effort to address longstanding concerns that the current system fails to adequately safeguard both national security and economic competitiveness.

For more than 60 years, U.S. export controls have suffered a patchwork of fixes with new requirements and cumbersome rules resulting in inefficiency, poor security and lost business.

An increasing number of global companies are purchasing products outside the U.S. because of the onerous U.S. export controls system. Others are taking actions such as ceasing to design electronics using U.S.-made products or stopping work with U.S.-based companies altogether.

U.S. regulations control the export of both defense and dual-use items (i.e., items that can be used for both commercial and military purposes). Electronics, including certain printed boards, are examples of potentially regulated exports. Controls on ITAR-covered electronics also

extend to the associated intellectual property (IP), such as chemical formulas, purchase orders containing specifications, and printed board artwork.

The administration's ambitious plans call for the current outmoded regime to be replaced with a single-tiered control list, a single agency to administer controls, a single enforcement agency, and a uniform, multiagency IT structure to streamline licensing approvals. Fully

achieving the administration's vision will entail passage of legislation by Congress, but the administration has moved aggressively to accomplish that which is within its authority, including a rewrite of USML categories.

IPC is a supporter of efforts to modernize and streamline export control regulations. The current export control system neither adequately protects national security, nor facilitates the export opportunities needed to grow the economy. Most importantly, IPC has advocated that the administration must use the opportunity provided by the reform of the nation's export control rules to clarify the frequently misunderstood regulatory treatment of printed circuit boards that underpin critical defense technologies.

“
The current export control system neither adequately protects national security, nor facilitates the export opportunities needed to grow the economy.
”

IPC's Efforts

Over the past four years, IPC conducted an aggressive and effective advocacy campaign for clearer and more explicit ITAR controls on PCBs as part of a revised USML. During that time, IPC met with key officials at the Departments of State, Commerce and Defense, filed two sets of formal comments on proposed revisions to Category XI, and testified before the U.S. House Committee on Foreign Affairs.

From the outset, IPC's position was clear: Printed board designs should remain under the jurisdiction of ITAR when the end item for which the board is designed is a USML item. PCBs must be controlled in the same manner as the defense articles for which they are designed because PCBs and their designs reveal valuable information about the workings of those defense articles. Throughout the four years, IPC sought the explicit enumeration of PCBs as the most effective and appropriate method of addressing the widespread confusion within the defense community about ITAR controls on PCBs and their designs.

On February 7, 2012, the IPC message was underscored by Mikel Williams, then president and CEO of DDi Corp and chairman of the IPC Government Relations Committee, who testified before the House Foreign Affairs Committee. Williams' testimony underscored the importance of clear and appropriate U.S. export controls on PCB designs for sensitive military technologies. The Committee on Foreign Affairs held the hearing to consider industry perspectives on export control reform, including proposals now being contemplated by the U.S. Departments of State and Commerce.

In addition to supporting the clarification of ITAR regulations for PCBs through explicit enumeration, IPC also conducted a one-year educational campaign, Follow the Law, Protect the Board initiative. The initiative sought to address continuing confusion in the defense industry about the applicability of ITAR to printed boards. At the center of the campaign was a white paper, "Applicability of U.S. Defense Trade Controls to Printed Boards," which was authored by the one of the country's leading ITAR lawyers. Delineating the applicability of ITAR to PCBs in plain language, the white paper also provided examples of the importance of protecting PCBs designed for ITAR-controlled defense items.

Revised Category XI Enumerates Control of PCBs

The specific listing of PCBs in Category XI clarifies and highlights the importance of ITAR controls on PCBs in ITAR-covered defense articles. This clarity represents a significant step in addressing the confusion in the defense industry about ITAR controls on PCBs, which should reduce inappropriate sourcing of printed boards for ITAR items from non-ITAR facilities. Additionally, any designs or digital data related to "specially designed" PCBs will be controlled as technical data.

In addition to specifically regulating, "(2) PCBs and populated circuit card assemblies for which the layout is specially designed for defense articles in this subchapter," the preamble to the rule states, "the Department has revised the controls for PCBs and patterned multichip modules, providing each with a separate subparagraph, and notes that jurisdiction of a PCB or patterned multichip module should follow the jurisdiction of the specific item for which it is designed, as opposed to the jurisdiction of the overall system into which the article one layer up from the PCB is ultimately incorporated."

Next Steps

The new rules are effective December 30, 2014. With respect to PCBs, the rule clarifies and emphasizes the existing regulatory status of PCBs for ITAR-controlled defense items, so companies should not wait until December to change internal control procedures that may not be fully compliant with ITAR.

In addition, the State Department has indicated to IPC that the rule, although final, may need some tweaks. IPC will continue to meet with the State over the next few months to determine if additional clarifying language should be added, likely in the form of a note.

For more information on IPC's efforts or to link to the final rule, visit www.ipc.org. **PCB**



Fern Abrams is director of government relations and environmental policy for IPC.



PCBs for Automobiles: What to Wear to the Party?

by **Yash Sutariya**

ALPHA CIRCUIT CORPORATION

As I was thinking of ideas for this article, a funny throwback commercial played on TV. It was a commercial for AutoTrader in which Bo and Luke Duke from “The Dukes of Hazard” were being chased in their 1969 Dodge Charger, the General Lee. However, it was set in current times, which meant the police cars chasing them were much faster than those in the original episodes. During the chase, the Duke boys identify technologies such as backup cameras, Bluetooth, and GPS that could have helped them out.

Thinking back to just 10 years ago, the list of technologies added to vehicles is quite amazing: electronic stability control, GPS, Bluetooth,

drive by wire, adaptive cruise, etc. The next wave of technologies (driverless vehicles, self-parking, anticipatory braking, etc.) makes use of those new base technologies in ways that we would only think of seeing in movies.

As a North American PCB fabricator, I find it obvious that this is a market that’s worth targeting or, at the very least, exploring for opportunities. As such, exploring this market will be the focus of this piece.

Industry Background

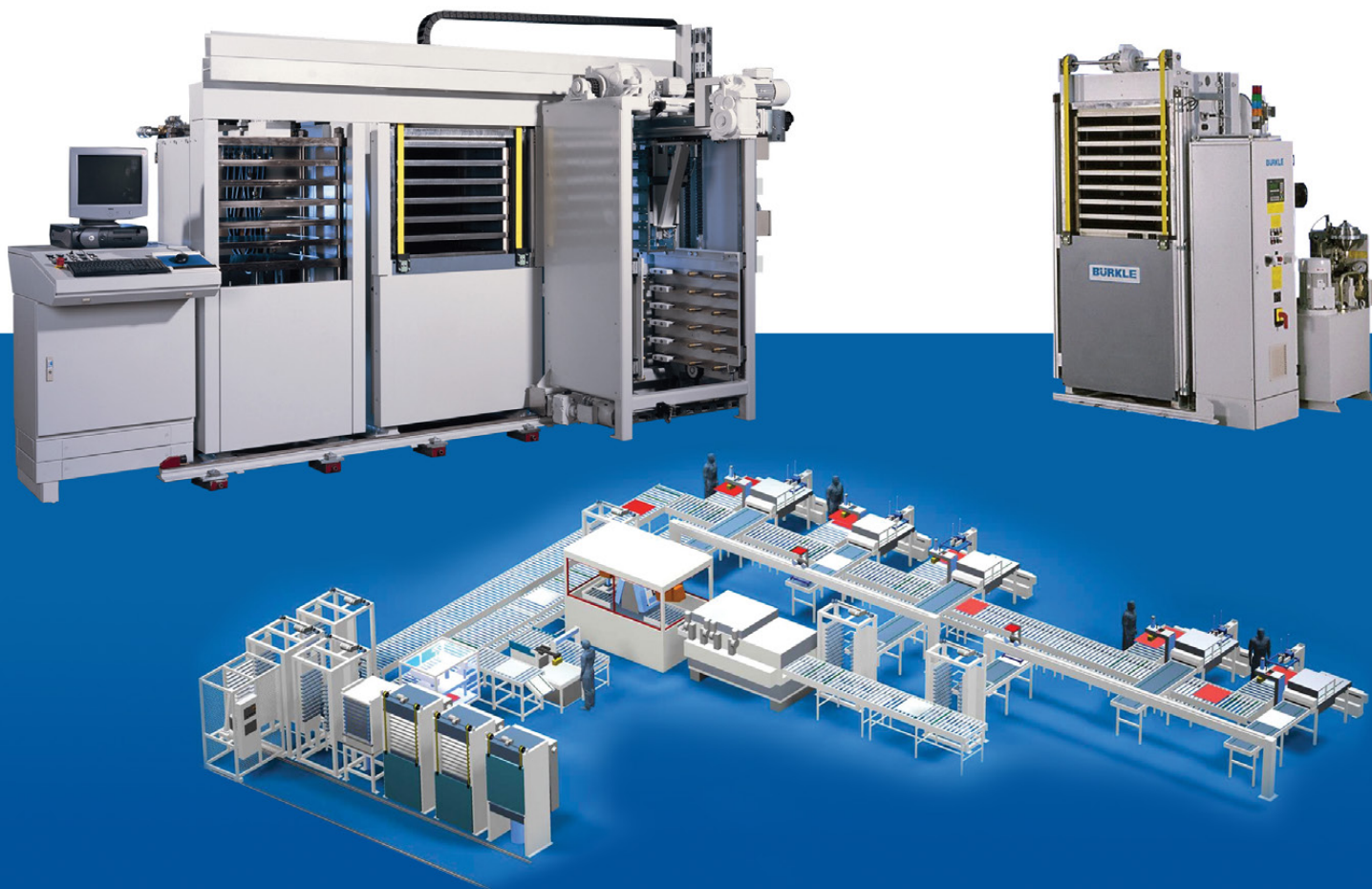
In the 1970s, the electronics content of the average automobile was close to \$100. The content began increasing in the late 1970s as a result of new government mandates regarding emissions and fuel economy, which couldn’t be accomplished with mechanical or electro-mechanical components. This push, coupled with advancements in semiconductors that allowed more output at decreasing cost, resulted in an ever-increasing amount of electronics content in subsequent years. By the early 2000s the average vehicle contained about \$1,500 worth of electronics content. Since then, some of the newer base technologies such as advanced infotainment and GPS became more commonplace, pushing electronics content to over \$2,000 by 2013.



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The culminating effect is that in a typical premium-class automobile there are 70–100 micro-processor based electronic control units running on about 100 million lines of code. To the PCB fabricators, that means the global automotive electronic market is currently in excess of \$150 billion, and is expected to grow to in excess of \$240 billion by 2020, according to more current estimates.

But how do I get Invited to the Party?

Quality

The past year has brought an abundance of headlines regarding product recalls. The most famous have been the rolling recalls from General Motors, but checking deeper into the news you can find various recalls from Ford (Ford Flex, Lincoln MKX, CMax, Focus), Toyota (Tundra), Land Rover (LR2, Evoque), Jaguar (XK, XF), Chrysler (200, Cherokee), Aston Martin (DB9, Rapide S), BMW (i3, Mini), Honda (Odyssey), and Mercedes Benz (GLK350). Not only is this only a partial list from this year, but it already includes most of the global automakers.

This is almost certainly going to put a renewed focus on supplier quality and long-term

reliability. As such, one of the base requirements to breaking into the market is having a robust quality management system (QMS). In 1994, the North American big three automakers developed a system named QS9000, which enabled their collective supply base to build and manage a single system that was recognized by the three primary customers in North America. However, by the 2000s it became clear that a more global outlook was necessary. The key factors towards determining this was that the big three were not looking too big anymore. Factories were being built in North America by foreign automakers at an increasing rate, with Honda, Toyota, and BMW leading the charge. Furthermore, these transplant OEMs often looked to have a localized supply base, prompting North American automotive parts and systems suppliers to target their business as well. Maintaining multiple quality management systems in a single factory proved to be an extremely expensive venture that was rife with opportunities for failure.

In response to this global dilemma, the major America, European, and Japanese automobile manufacturers created the International Automotive Task Force (IATF), whose primary

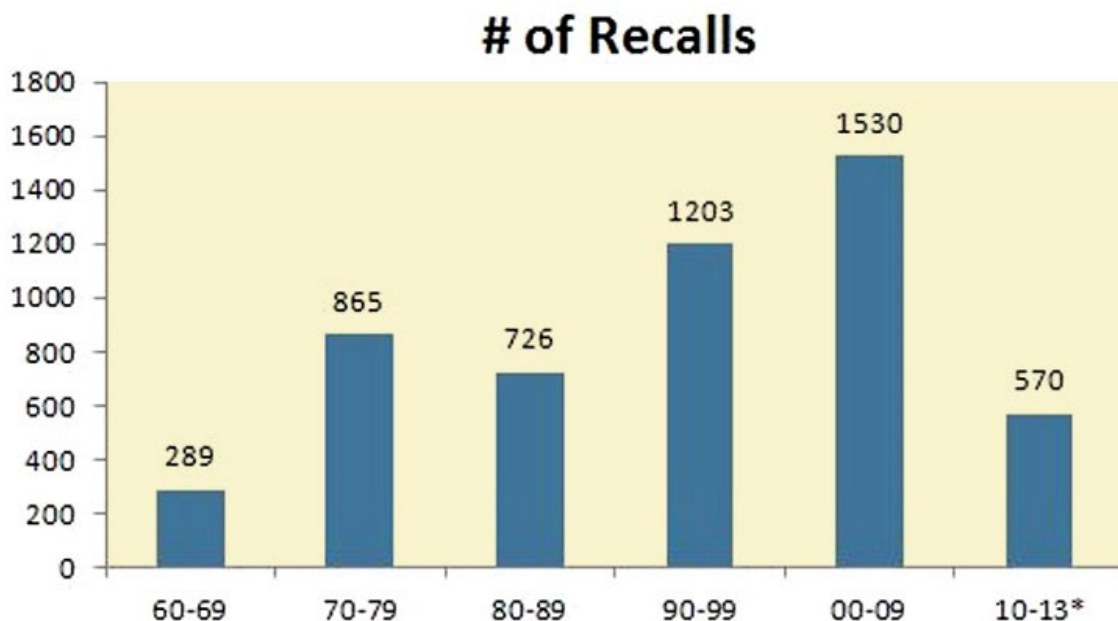
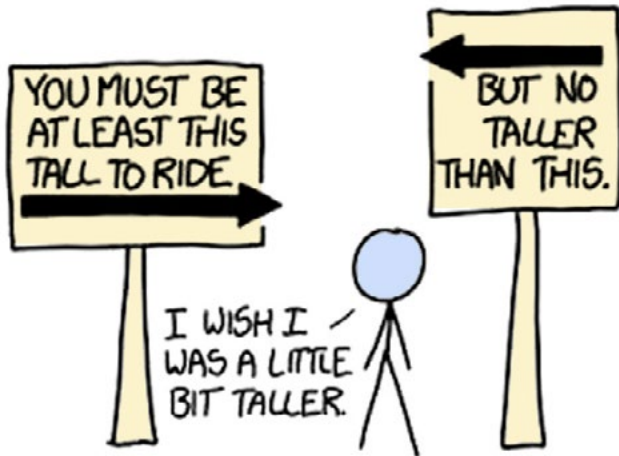


Figure 1: Vehicle recalls by decade* through September 30, 2013. (source: NHTSA)



goal was to provide quality-related products to the automotive manufacturing base. The most important product created by the IATF was the TS 16949 global automotive quality systems specification. Being recognized by all major automotive OEMs, it resulted in the obsolescence of the QS9000 standard and continues to be the de facto QMS for the automotive supply base.

Therefore, in order to begin targeting the automotive electronics market, the initial hurdle will be to create and execute a proper QMS that meets the TS 16949 criteria. Once established and executed, you would need to achieve certification from an accredited registrar. I detailed the primary steps towards creating an effective TS 16949 system in a [past article on automotive electronics](#). Not much has changed since then in case you would like to reference it as a starting point.

Capability

Let's assume you've gone through the steps of breaking down and rebuilding your QMS and are now TS 16949 certified. Now that you've gotten into the party, don't assume that someone is going to want to dance with you just for walking in through the door. You've got to accessorize in order to find a date.

The reason why accessorizing is important is because while there aren't many TS certified PCB fabricators in North America, there are hundreds of them in China that collectively supply the vast majority of PCBs used in automobiles. One driving factor is that, historically, PCBs for

the automotive market didn't really even come close to pushing the envelope for technology. These would typically be single through 6-layer PCBs made of standard FR-4. Accordingly, what you've got to do is target the segments of that market that are not only a good fit for your company, but for which your company is reciprocally a good fit.

One way to do this is to think about electronic automotive systems and their underlying technologies. Once you have a handle on what technologies those products use, you've got to build the capability for producing those technologies in your company.

We'll discuss a few as examples as we don't have enough room in this paper for a truly exhaustive list. Not to mention that at the current rate at which technology for automobiles is evolving, such a list is sure to be obsolete within a short period of time.

Technology: **collision avoidance/anticipatory braking**

Essentially, these applications use a form of near-field radar that enables the safety systems to react accordingly to external events. As those suppliers to the military market know all too well, these systems can use a wide variety of high-speed, low-loss materials. Typical suppliers are Arlon, Nelco, Rogers, and Taconic, who provide materials made of specialized FR-4, ceramic based, and PTFE/Teflon-based materials to achieve the desired properties and function.

Unfortunately, you can't just change the material type on the traveler and expect everything to turn out right. Let's take PTFE materials as an example and identify the processes that need adjustment.

- **Drilling:** Unique feeds and speeds are definitely required, and you can't just go by the datasheet. I had a wonderful experience last year in which a customer wanted to try a design but built in two different materials, one from Rogers and one from Taconic. In reading their datasheets and comparing to our standard PTFE feed and speed tables, we found that there was a wide range of chiploads. This was odd since both materials were PTFE based, implying they would drill similarly. Long story short, we end-

ed up using our standard F&S tables for the Rogers, and the Rogers datasheet F&S table for the Taconic.

• **Activation:** Typically with FR-4 materials you can just go straight to metallization (electroless or direct) and continue processing. With PTFE materials, since they are Teflon® based, you must activate the surface to enable the copper plating to stick. This can be done by using either a plasma unit or a chemical-based method. If ponying up over \$150k for a plasma unit from either March or Plasma Etch isn't in the cards, the chemical treatment method might be the way to go. Two such suppliers are Acton Technologies, Inc. (FluoroEtch) and W.L. Gore (Tetra-Etch).

I've heard of people shortcutting this process, which may work for lower level commercial customers. However, when it comes to automotive the best bet is to follow best practices. Just think how many recalls were caused by the motivation to save just a few cents on a part. No need to subject your company to that risk as OEMs are coming back to suppliers harder than ever to recoup warranty and recall costs.

Technology: Power Delivery Systems

The growing number of hybrid and fully electric vehicles are fueling a need for more advanced power delivery systems. Also, the increasing number of electronic functions is driving battery manufacturers to find new options, such as lithium ion.

From a fabricator's perspective, this means heavy copper PCBs (three or more ounces) could see an increase in demand. While double-sided heavy copper PCBs are fairly easy to do, multilayer buildups can be tricky. We'll touch on a few of the key things to focus on during manufacturing.

• **Stackup Generation:** One of the most frequent failure modes in heavy copper multilayer boards is voids within the bondsheet dielectric. Voids can subsequently cause high resistant shorts, CAF, and broken vias. One way to address this is by using as much 106 resin rich prepreg to fill the etched areas. Any leftover room in the stackup height can be made up by

using 2116 prepregs as internal pads to push the resin into every etched out feature. Typically, though, with heavy copper you are waging a battle between minimum copper requirements and maximum thickness requirements. One trick to address this is by pre-filling the etched inner layers with layer fill epoxy, thereby minimizing the need for multiple layers of prepreg. Unfortunately, neither of these is a cheap option but well worth the price when it comes to reliability of the end product.

• **Multilayer Lamination:** Most technologies allow you to throw in multiple part numbers using the same press recipe. However, heavy copper projects warrant their own recipe. Since you have a higher than normal amount of copper within the stackup, you should be using a higher temperature setpoint since that copper will act as a heatsink. Further, you should play with the rate of rise and pressure cycles to insure proper prepreg flow and etched area fill.

• **Etching:** Most heavy copper projects will have you in inner layer etch at least 3x as long as standard inner layers. It's critical that you address the strength of the dry film being used. Most standard dry film will manage up to three ounces, but things get sketchy beyond that. It's important that to run development panels to establish the true limits of your dry film; it makes no sense to save 50 cents on dry film just to end up scrapping out a \$20 inner layer core.

Technology: Infotainment/Communications

One of the newer technologies that has been a huge burden on automakers across the spectrum is infotainment/internal communications. These technologies employ the use of Bluetooth, cellular, and sometimes even WiFi. If you look at the J.D. Power initial quality surveys, you will find that many of the premium marques take a spot in the "Worst Performing" section, mainly because of their new driver interface systems. One of the most recent cases was the failures documents on the Ford Sync system. While many of these issues were due to software glitches, there has been a keen focus on hardware quality as well. These systems often

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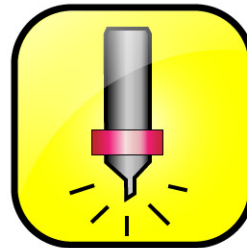
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push automakers into previously untouched technologies due to the component footprints for these capabilities. As such, in order to capture a piece of this market segment many fabricators will have to ramp up their capabilities for fine lines, higher layer counts, and microvias.

• **Drilling Microvias:** Drilling small holes is one thing to master, but drilling small blind vias is a totally different chapter in the book. Most folks assume that both an expensive and time-consuming outsource is involved, or they'll have to spend \$500k on a laser drill. However, it's important not to overlook the advancements that have been made in mechanical drilling systems. The incorporation of linear motors and scales and refined contact drilling systems enable you to drill diameters down to 0.002", with positional and Z-axis accuracy of 0.0005". This is more than adequate for most designs at less than half the cost of a laser drill. Furthermore, unlike a laser drill, when the mechanical drill isn't busy drilling blind microvias it can be commissioned to drill standard products to enhance its ROI.

• **Microvia Drill Quality:** When it comes to consumable materials in the drill room, the habit for most fabricators is to go with the cheapest possible materials since they are discarded after just a single use. However, backup

and entry quality are paramount when it comes to successful microvia creation. Using coated backup with high-quality pressed fiber will ensure reduced burring and minimal debris pull-back into the hole. It's much easier to clean a hole out if there is less debris in it to begin with. Additionally, using the proper mix of phenolic, aluminum, and coated entry for each specific application will maximize location accuracy and drill bit life.

• **Layer to Layer Registration:** For most folks, this means investing in new tooling systems that have more pins to ensure greater layer-to-layer accuracy. Depending upon the current state of your tooling, this may not be necessary. The first step would be to check the condition of what you have already. Often, huge gains can be made just by checking the straightness of your pins, quality of your bushings, and flatness of your caul and lamination plates. The next step would focus on pre-engineering. Higher-technology PCBs often incorporate the use of thin cores and mixed copper weights that result in non-uniform stackups. With a non-uniform stackup you can no longer count on all of the cores shrinking or expanding at the same rate that you can correct for in drilling. We've found tools such as X-ray drills and PerfectTest to be invaluable at providing data to continuously tighten your process and scale factors.

Automotive PCB Categories		Class	Min Temp	Peak Temp
Class A	Interior Components	A	- 40°C	+ 85°C
Class B	Under-Hood	B	- 40°C	+ 125°C
Class C	On-Engine	C	- 40°C	+ 145°C
Class D	In-Transmission	D	- 40°C	+ 155°C
Class E	In-Engine	E	- 40°C	+ 165°C

Figure 2: Automotive PCB categories and the changes in peak temperature between the five classes of automotive PCBs.

Performance

Supplying to the automotive market is not an easy path. Your work isn't even over after you establish quality systems and technical capabilities. After all this, these darned customers actually expect your boards to work for a long time and not just past final test. Even component manufacturers have been driven to increase their products' performance in thermal cycling environments. For some reason, we North American PCB fabricators get pounded on even harder. To summarize this, you would need to meet different performance criteria for each end application. Figure 2 displays one automotive supplier's requirements.

Meeting these requirements is not an easy feat, but not impossible either. It means devoting engineering and process development resources to your critical processes such as multi-layer lamination, drilling, and plating. It could also mean a change to your supply base to switch from "what's on sale this week" to more

robust raw materials and consumables such as copper clad laminate, drill bits, and copper plating chemistry.

Conclusion

The automotive electronics market is ensured to generate growth for the rest of this decade. Just because the Chinese have the lion's share of this mature market doesn't mean there is no room for a North American PCB fabricator. You just have to be more discerning and offer a value-added solution to the customer, which can take investment in education, processes, and people. Not an easy road, but one with potential riches at the end. **PCB**



Yash Sutariya is president of Alpha Circuit Corporation. For more information, or to contact Sutariya, ysutariya@alphacircuit.com.

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Thin PCBs for Smartphones:

Technology & Reliability Considerations



**by Thomas Krivec, Gerhard Schmid,
Martin Fischeneder, Gerhard Stoiber**

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Abstract

The next generation of smartphones will demand very thin multilayer boards to reduce product thickness again. This paper shows three different manufacturing approaches which can be used for very thin, any-layer build-ups. The technological approaches are compared on reliability level—the any-layer copper filled microvia technology which is to be considered as state of-the-art technology for high end phones and the ALIVH-C/G technology that is well established in Japan. A test vehicle design featuring test coupons for comprehensive reliability test series has been defined as target application for investigation. The applied test vehicle build-ups comprise an eight-layer build-up with total board thickness below 500 μm . The first test vehicle is based on an any-layer HDI build-up including copper filled stacked

microvia structures, the second test vehicle features a 1+6+1 ALIVH-C build-up comprising an outer HDI prepreg layer, while the third test vehicle is built in ALIVH-G technology featuring a full ALIVH build-up.

The influence of the applied manufacturing technology on the reliability performance of thin PCBs is evaluated based on these three test vehicle build-ups.

To cover the behavior during SMD component assembly the produced samples are subjected to reflow sensitivity testing applying a lead-free reflow profile with a peak temperature of +260°C. Failure occurrence and the observed failure modes are evaluated and compared.

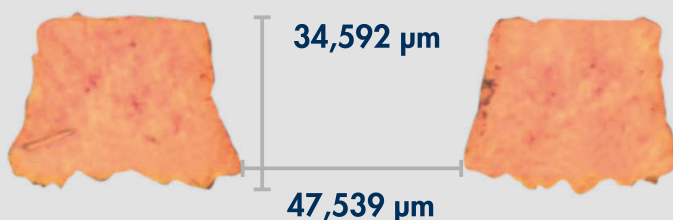
In parallel, a temperature cycling test is conducted on the test vehicles in a temperature range between -40°C and +125°C in order to evaluate the thermo mechanical reliability of the test vehicles with regard to the manufacturing technology.

In order to characterize the reliability aspects influenced by electrochemical migration phenomenon the different samples are subject-



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ed to a HAST test at +130°C with 85% humidity level.

The results obtained from reliability testing are summarized and compared within this paper. The identified relations between manufacturing technology and the reliability performance of the test vehicles are shown; strengths as well as weaknesses of the applied any-layer technologies are identified and summarized.

Introduction

IBM's introduction of the IBM Simon Personal Communicator marks the beginning of the smartphone era^[1]. Combining phone functions with the functionality of a PDA is a remarkable milestone for our communication age. However, while being very innovative, the device was not really suitable for one's waistcoat pocket. With a total weight of 510 g and a thickness of 38 mm, it was confined to in the briefcases of business executives. Since that time, the smartphone OEMs have quite clearly recognized that next to functionality the handling behavior

and the ergonomics of the smartphone device belong to the decisive criteria for the customers. Based on selected examples, Figure 1 shows how the smartphone dimensions have evolved since Simon appeared. While the basic length and width of the devices just changed with regard to functional and aesthetic trends, the reduction of the thickness of a smartphone device became a kind of race, with the OEMs as competitors. As Figure 1 shows, the thickness of a smartphone device has been reduced by a factor of almost six, with the October 2012 champion being the Finder X907 device from Chinese OEM Oppo. This Android-driven device claims to have a nominal thickness of only 6.65 mm. However, there will not be much time to enjoy the position at the cutting edge since another Chinese OEM, ZTE, already announced the introduction of a device with 6.2 mm within the next months.

In order to achieve this reduction, the smartphone designers quite neatly used all the possibilities that the always ongoing miniaturization

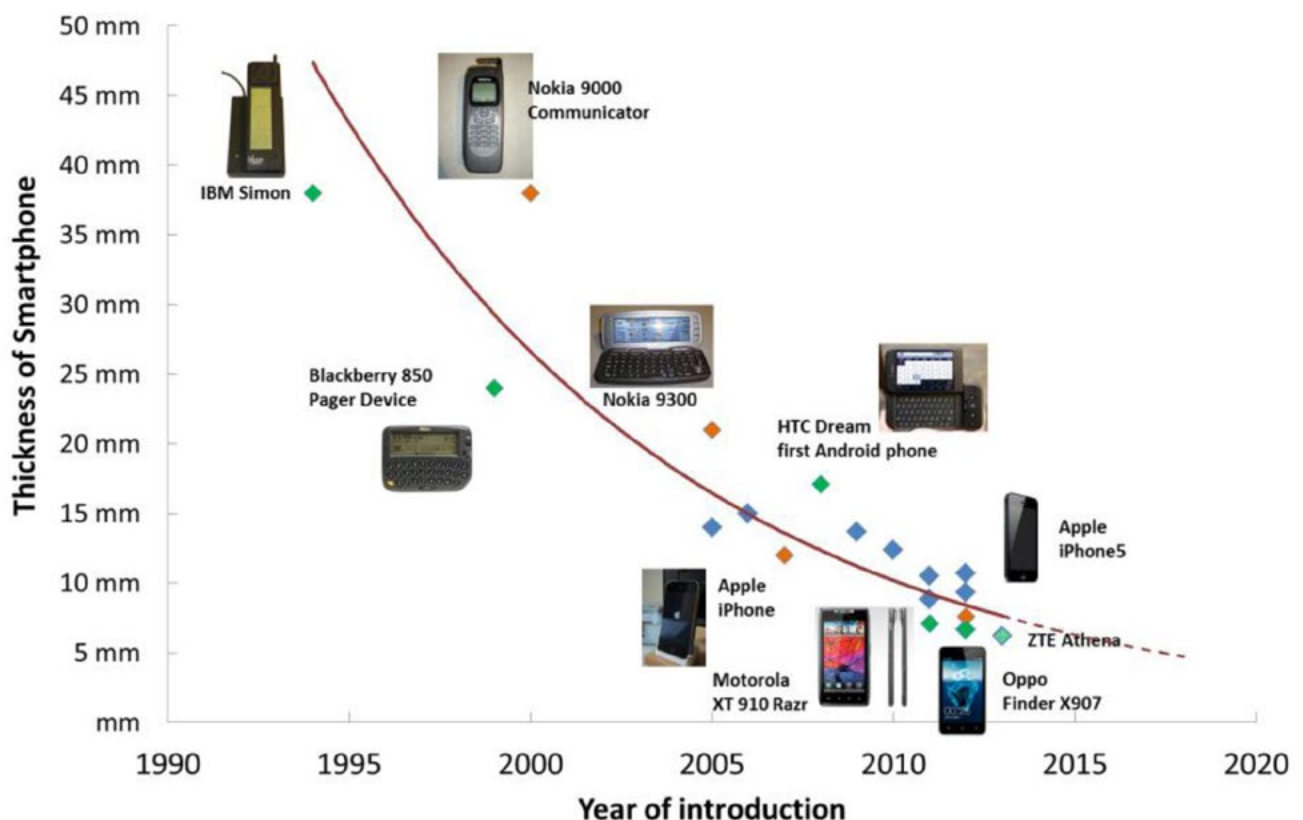


Figure 1: Thickness of smartphone devices with regard to the year of introduction.

trend in industries offered to them. It is obvious that for the producers of PCBs for smartphone devices it has been necessary to adopt for that demand and to reduce the thickness of their PCBs significantly.

The period around the introduction of the first smartphones coincides with the breakthrough of the HDI technology in PCB making^[2]. The first smartphones often featured eight-layer rigid boards, with a stack-up made of 1080 fabric style prepregs and 25 μm copper layers. While the layer count is similar for the boards of today's high-end phone, again the thickness changed significantly: from more than 1.2 mm in the year 2000 to approx. to approximately 600 μm in 2011, while the target for a rigid eight-layer board in 2013 has been set to 400 μm .

Experimental Set-up

In order to evaluate the production process and performance of very thin rigid PCBs within this study test vehicles in three different technological approaches have been built. The test vehicles then were subjected to a reliability test program comprising a MSL Level 3 reflow test, a thermo cycling test with lower temperature level of -40°C and an upper temperature level of $+125^{\circ}\text{C}$ at two cycles per hour and a highly

accelerated stress test (HAST) at a temperature level of $+130^{\circ}\text{C}$ with a humidity level of 85%.

Processing Technologies ALIVH™ and HDI/FV

To build the rigid eight-layer board with a total thickness below 500 μm , two PCB production technologies were considered. First, HDI technology combined with microvia filling was chosen in order to realize the implementation of stacked via designs (HDI/FV)^[3]. The second is the proprietary any-layer interstitial via hole (ALIVH) technology that was introduced in 1996 by Panasonic/Matsushita, and which is well established in Japan. The HDI/FV process features the traditional process flow with lamination steps, mechanical and laser drilling and subsequently establishing the contacts between the layers by electroless copper deposition and electrochemical plating. Also the filling of vias is done in an electrochemical plating process, while the ALIVH process is based on printing a conductive copper paste into pre-drilled holes of the prepreg layers to achieve the required electrical connection from one copper layer to the other. A more detailed description of the process has been given by Happy Holden in the HDI Handbook^[4]. A schematic view of the ALIVH process is shown in Figure 2.

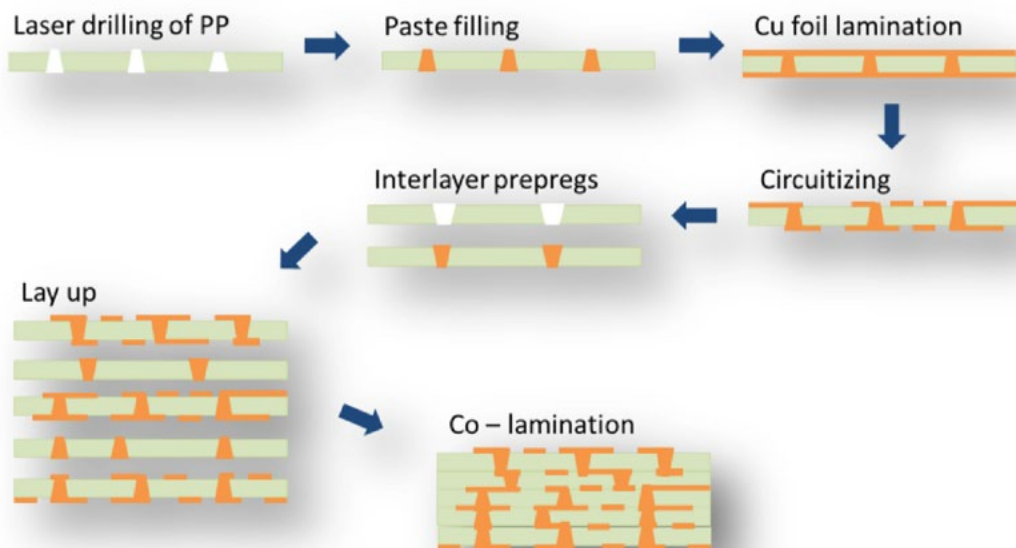


Figure 2: Schematic description of process flow at ALIVH PCB production process.

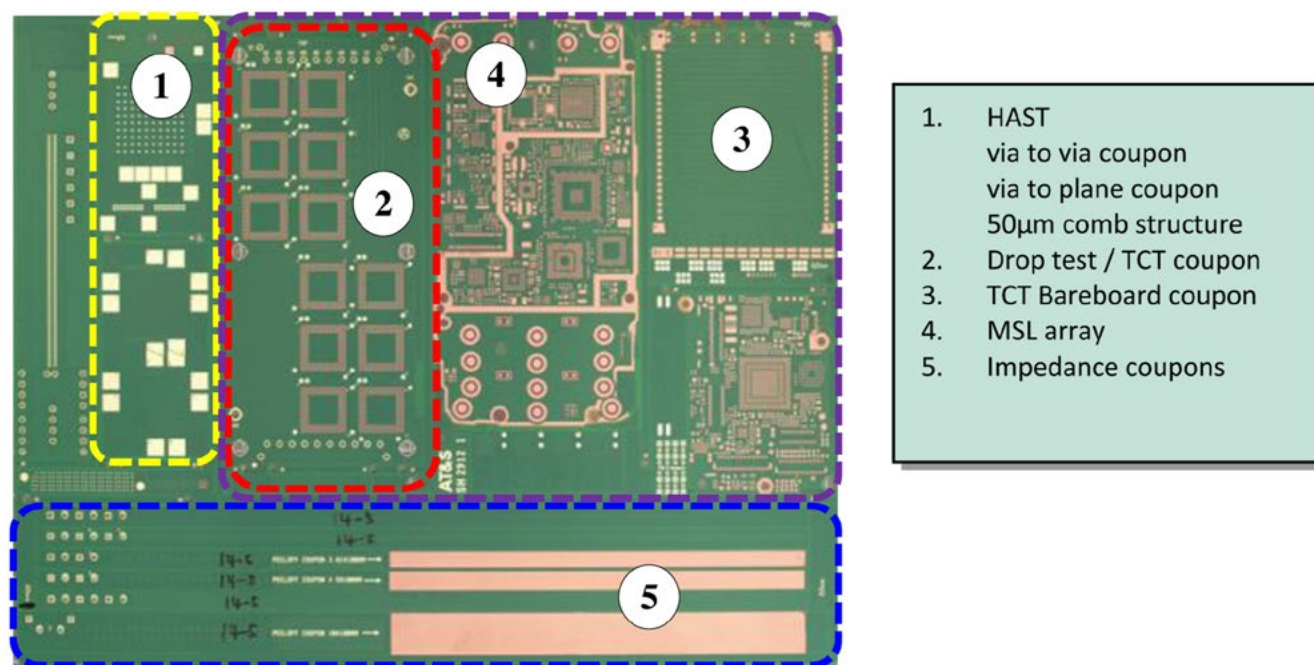


Figure 3: Test vehicle design and corresponding test coupons.

Test Vehicle	Technology	Build-up	Dielectric Material	Expected thickness [μm]
TV1	HDI/FV	3-2-3	HF FR4	471
TV2	ALIVH-C	1-A6-1	Low Flow HF FR4	459
TV3	ALIVH-G	A8	HF FR4 Low Flow HF FR4	448

Table 1: Built test vehicles and expected total board thickness.

Design and Stackup of Test Vehicles

For the targeted rigid eight-layer PCB test vehicle, a test design used regularly for reliability tests and material qualification issues at AT&S was selected. The test vehicle comprises several coupons for electrical and reliability tests with an eight-layer build-up. With regard to the defined production technologies slight modification within the design of the single part numbers had to be made, however great care was taken to assure the comparability of the HDI and ALIVH test vehicles. Figure 3 shows the built test board and the corresponding test coupons used for the further tests within the reported work.

Stackup and Applied Material

For the reported work, three different test vehicles with different build-up approaches have been defined. As Table 1 shows there is one HDI build-up, one full ALIVH build-up (ALIVH-G) and an ALIVH-C build-up where layers 2–7 are manufactured in ALIVH technology and the two outer layers are then in a subsequent process step added in HDI technology. The expected thickness column shows that thickness value for the board as it is calculated during the PCB design stage.

Since the target applications this study is based on are from the mobile devices segment all used dielectric materials have been chosen

	Low-flow FR-4	FR-4 standard	FR-4 standard
Halogen free	yes	yes	yes
Cloth style	1037	1037	1x1067
Resin content [%]	73	70	65
Thickness [μm]	40	45	50
Copper thickness [μm]	-	-	12
Dk	4.3	4.1	4.2

Table 2: Properties of applied dielectric material.

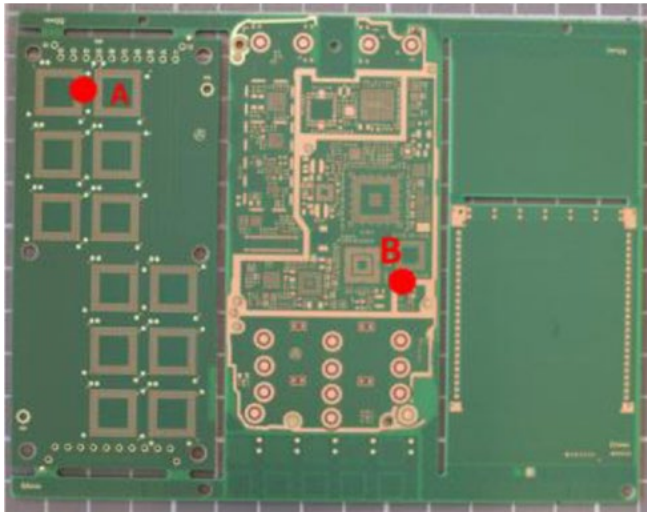


Figure 4: Positions for board thickness measurements.

from the standard materials which are well introduced in PCB mass production. It was mandatory for all selected materials to be halogen free (HF).

Relevant material and build-up properties of the applied dielectric materials are given in Table 2. For copper layers, standard 12 μm copper foil with single-sided, standard treatment has been applied.

Experimental Procedures

Board thickness measurement

The thickness of the board was measured at two positions of the board as shown in Figure 4. The measurement was done manually with a

Moisture sensitivity level	MSL3
Conditioning/drying	24 h/125°C
Pretreatment MSL3	
Temperature	60°C
Moisture duration	60%
Reflow cycles	40 h

Table 3: Preconditioning for IPC/JEDEC J-STD-020D1 MSL3acc level reflow testing.

digital micrometer gauge with a precision level of 0.001 mm at ambient conditions. The measurement was done for a random sample of 15 TVs from the production lot. While position A represents an area with lower overall copper content in the build-up, position B corresponds to an area of the built test vehicle which features a relatively high copper content in the stackup structure.

Reflow performance

The reflow testing was done in accordance with IPC/JEDEC J-STD-020D1T^[5]. Applied moisture sensitivity level was level 3. The sample size was 10 test vehicles of each test vehicle type. Conditions for preconditioning are given in Table 3.

Thermo cycle test

The thermo cycling of the samples has been done in accordance with JEDEC JESD 22-A104D^[6], Test Condition G,2,C. Parameters are given in Table 4. Testing at the bareboard

Parameter	Level
Temperature low	-40 °C
Soaking time at low	5 min
Temperature high	+125 °C
Soaking time at high	5 min
Cycles per hour	2
Total cycle count	1000

Table 4: Temperature cycling test parameter setting.

level was carried out with a designated daisy chain coupon for all three test vehicles: TV1, TV2 and TV3. Resistivity of the daisy chain structure at each sample was checked at defined checkpoints during the test duration. For the bareboard configuration in total eight coupons of each test vehicle type have been tested. The test is considered as passed if after 1000 temperature cycles the change of resistivity of the daisy chain structure is within the limits of 10%.

Additionally, four populated samples each were tested for TV2 and TV3. The populated sample was assembled with 12 CTBGA288 dummy components (Figure 6). Each of the components during the test was monitored online by an event detector device. Test is considered as passed if no failure at a monitored structure is identified.

Highly Accelerated Stress Test (HAST)

HAST testing was done in accordance with JEDEC JESD 22-A110C^[7]. The HAST test provides four process parameters: temperature, humidity level, applied bias and duration. For the current test the following parameter set was applied. For pre-treatment, the samples have been thermo cycled five times between -40°C to +125°C, then stored for 48 hours at 60°C and 60% humidity level. Last step of preconditioning for the HAST test have been five lead-free reflow cycles with +260°C peak temperature.

For the actual HAST test then the parameter set given in Table 5 has been applied.

The used test coupons provide structures for via-to-via testing (one structure per coupon), via-to-plane testing (one structure per coupon) and comb structures (one comb structure per layer) as shown in Figure 7 and Figure 8, respectively.

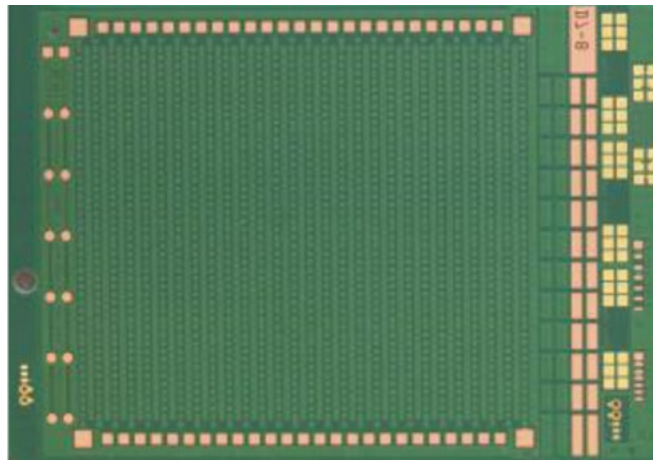


Figure 5: Bareboard daisy chain coupon for thermo cycling.

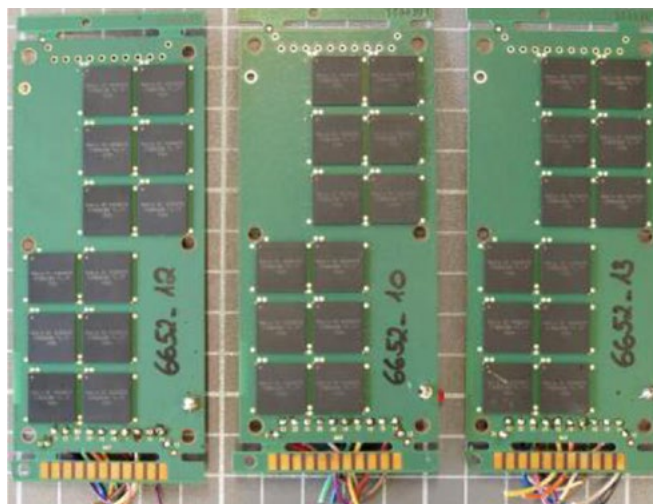


Figure 6: Assembled coupons (TV1) for thermo cycle testing.

In total, eight coupons per part number were tested. All test structures have been monitored continuously during the test period, and the results have been recorded. As failure criterion at each of the tested structures a drop of resistivity below a value of 106 ohms was considered.

Results

Test vehicles and board thickness

After pressing, the test vehicles were singularized from the panel and the final thickness was evaluated. Table 6 shows the measured thickness

Parameter	Level
Temperature	130°C
Humidity	85% r.h.
Bias	3.5 VDC
Test duration	120 hrs

Table 5: Parameter set applied for HAST testing.

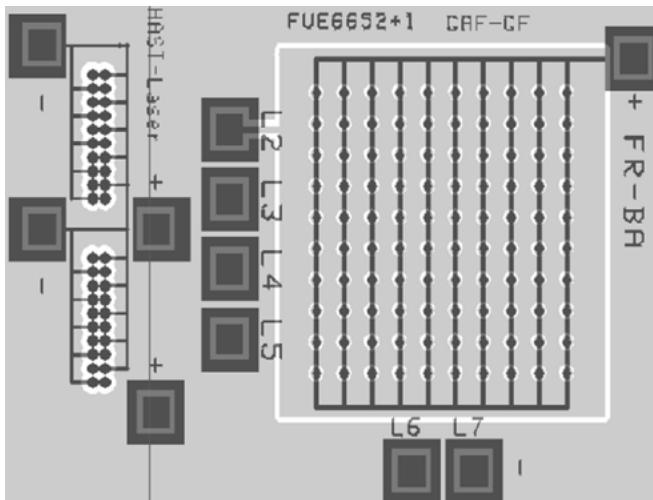


Figure 7: Via-to-via and via-to-plane test structures of HAST test coupon.

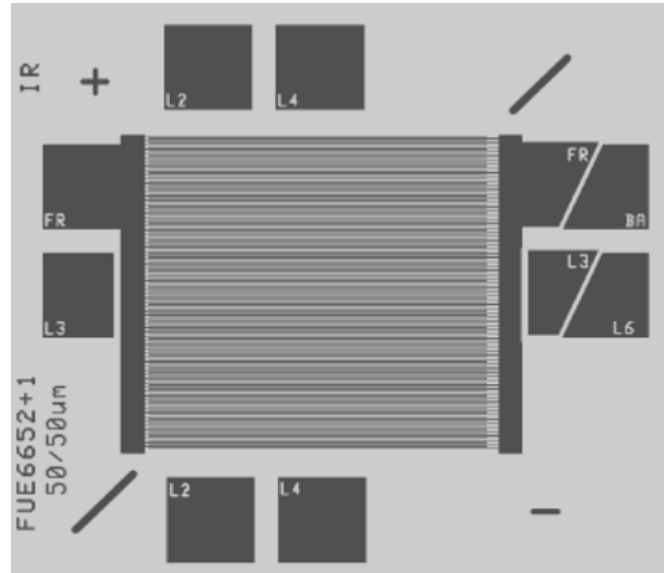


Figure 8: Comb structure, front layer of applied HAST test coupon.

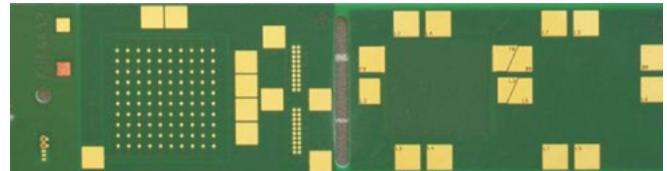


Figure 9: Thinboard HAST test coupon.

Test Vehicle	Build-ups	Thickness Pos. A mean/ σ [μm]	Thickness Pos. B mean/ σ [μm]
TV1	3+2+3	443/5.4	482/4.3
TV2	1+A6+1	481/3.3	498/4.3
TV3	A8	485/5.5	512/6.6

Table 6: Thickness values of built test boards.

values for the boards. Cross-sections of the TV1 and TV2 are given in Figure 11 and Figure 12, respectively. Table 6 shows the mean value for a random sample of 15 TVs with the thickness measured manually with micrometer gauge.

Reflow performance

The results of the reflow testing are summarized in Table 7. The results of the components show that the HDI/FV board performed signifi-

cantly better than the two ALIVH build-ups. While at the TV2 and TV3 most of the delamination failures occurred between the third and fourth reflow cycle, all TV1 samples survived a number of 15 reflow runs. An example for a typical failure that was observed at TV2 and TV3 is given in Figure 13.

However, it has to be pointed out that the big difference observed cannot be directly related to the influence of the manufacturing pro-

Test Vehicle	Number of reflow cycles survived	
	Mean Value	σ
TV1	15	—
TV2	2.4	0.8
TV3	3.4	1.2

Table 7: Results of reflow testing of thin board test vehicles.

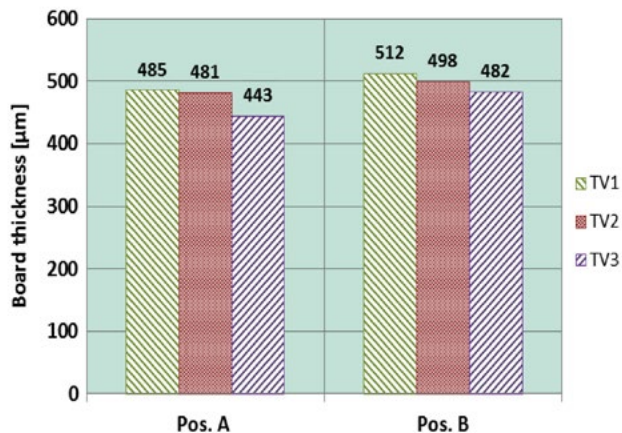


Figure 10: Mean thickness of the manufactured thin boards (TV1 to TV3).

cess. Rather, it has to be considered that the FR-4 HDI prepreg material used is a most recent generation of FR-4 material that has been optimized for reflow behavior and has a known outstanding reflow performance. Thus, it is as expected that TV3 shows the best performance in MSL testing.

If the cross-sections of the failures at TV2 and TV3 are investigated in more detail, it is visible that the delamination failures occur in both cases which feature design characteristics known to be critical for reflow testing, such as structures with full copper areas. The analyses did not show evidence for an interface failure that could be related to the applied copper surface adhesion promotion system. Instead, the cross-sections show a mixed failure mode with cohesive failure in the prepreg layer as well as adhesive failure at the interface (Figure 14). In order to identify the root cause for delamination at the current samples more work has to

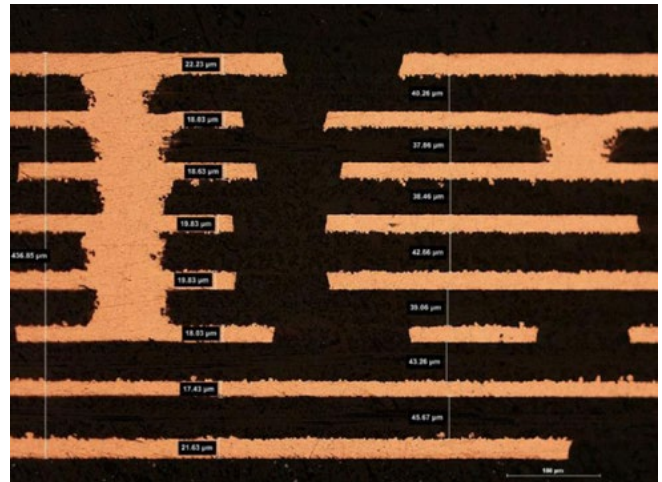


Figure 11: Cross-section of TV1 (3+2+3 HDI/FV build-up).

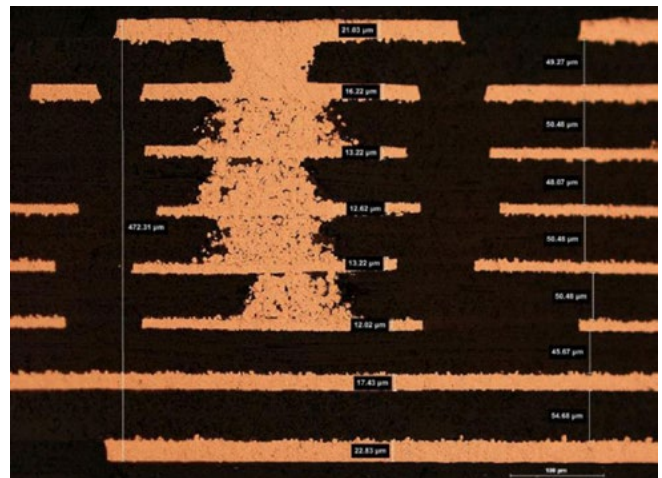


Figure 12: Cross-section of TV2 (1+A6+1 ALIVH-C build-up).

be done; however, although the performance of TV2 and TV3 in the reflow process did not reach the level required for mass production boards, it is considered as acceptable, taking into account that the samples are built within a development project without any process optimization steps.

Thermo cycling results

As described earlier, the temperature cycling was done on bareboard coupons as well as on populated ones. Neither at the bareboard samples nor at the populated ones were failures



Figure 13: Cross-section after reflow testing, with occurred delamination at TV3.

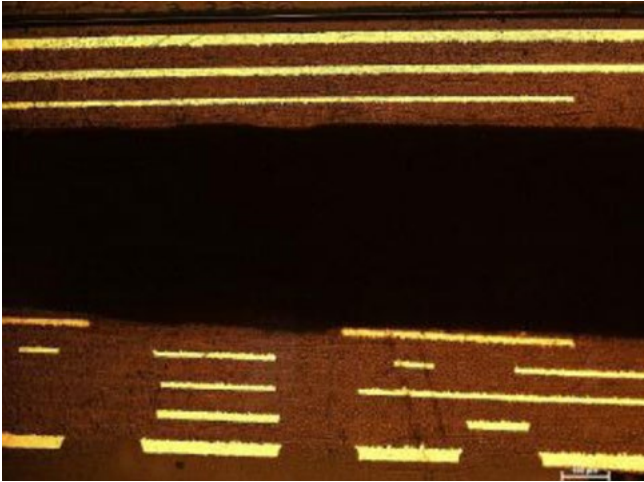


Figure 14: Detailed view on delamination area at TV3.

observed over the test time. None of the tested specimen exceeds the limit of -10% of resistivity decrease; the test is considered as passed for all part numbers.

At the thermo cycling of the populated samples also no failure was observed as shown in Table 8.

Based on the obtained results it can be considered that the thermo cycling behavior will not present the primary challenge in manufacturing thinner boards. It is commonly considered that major effect influencing the performance of boards stressed cyclic thermo load is the CTE mismatch between copper at vias and applied dielectric materials. Making the boards thinner does not make the mechanical loads on the copper plating in the plated through holes or the micro vias significantly more severe. This assumption is confirmed by the results of the current work. Additionally no influence of the manufacturing technology was observed. All test vehicles manufactured with the different any-layer technologies passed the limit of 100 cycles in bareboard as well as populated configuration.

Part number	Thermo cycle test
TV1	4/4 passed
TV2	4/4 passed

Table 8: Summary of results of thermo cycling test, board level.

	TV1	TV2	TV3
Comb L1	1/5 failed	1/5 failed	0/5 failed
Comb L2	1/5 failed	0/5 failed	0/5 failed
Comb L3	0/5 failed	1/5 failed	0/5 failed
Comb L4	0/5 failed	0/5 failed	1/5 failed
Comb L5	0/5 failed	0/5 failed	1/5 failed
Comb L6	0/5 failed	0/5 failed	1/5 failed
Comb L7	0/5 failed	0/5 failed	1/5 failed
Comb L8	1/5 failed	1/5 failed	2/5 failed
V-2-P	2/10 failed	2/10 failed	3/10 failed
V-2-V	0/10 failed	0/10 failed	0/10 failed

Table 9: Summary of result of HAST testing for thin board test vehicles.

Results HAST Test

In contrast to the thermo-cycling the electrochemical migration behavior seems to be a more critical issue for very thin boards. The subsequent Table 9 shows a summary of the results obtained from HAST testing of the investigated samples.

In general the table shows that several failures have been recognized. At the current study the samples with an HDI outer layer—TV1 with the full HDI built up and TV2 with the ALIVH-C built up showed at better HAST performance than TV3.

For the HAST test the via-to-via (V2V) structure can be regarded as the least critical case of the three cases evaluated. As expected there was no failure observed at these structures.

In contrast to the V2V case, for the via-to-plane structure (V2P) at all test vehicles failures were observed. The majority of the failures occur at early stage of the test which might be a sign of residues or impurities due to non-optimized manufacturing conditions. Cross-section analyses of the failed samples did not show evidence of failure due to dendrite growth. All observed dendritic structures can be considered as small compared to the corresponding dielectric gap. However, as it is also shown subsequently for the comb structures, the samples show clear signs of electrochemical migration of copper into the dielectric material. Together with the observed small dendrites this is considered to be a major cause for the observed failures.

Concerning the comb structure the results are similar to the results obtained for the V2P structures. Again TV1 and TV2 show better results than TV1. For all samples the majority of the failures are located in the outer layer comb structures, literally in layer 1 and layer 8. Figure

15 shows a detailed plot of the monitored resistivity versus test duration for the comb structure on one outer layer (layer 8).

As for the V2P structures, the evaluation of cross-sections of the failed coupons did not show evidence of excess filament growth or related electrochemical migration effects which could be identified as root cause for the failure in the HAST test. In fact the comb structures showed significant signs of copper migration at the failed samples. Figure 16 shows an example for a failed structure at TV3 in a darkfield view; Figure 17 shows a darkfield/UV image of a failed comb structure of TV2.

Both figures show clearly the migration front at the copper traces with negative potential. However, it is also visible that the migration front has not reached the neighboring conductor at the time of failure. So again it is considered that failures at the comb structure are a combined phenomenon where the migration effects together with dendritic growth or

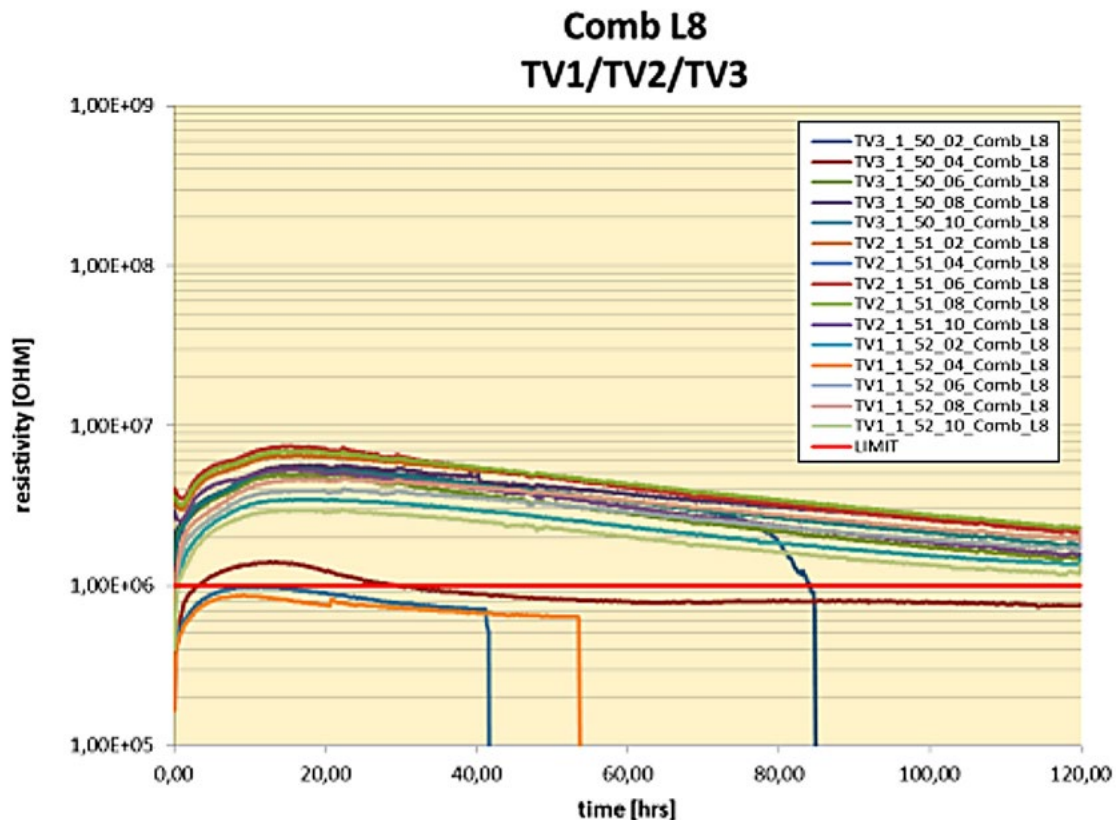


Figure 15: Resistivity for comb structure on outer layer (L8) vs. storage time in HAST test.

impurities such as copper residues finally result in a drop of the resistivity.

In general, based on the experiences available at AT&S related to electrochemical migration phenomenon such as dendritic growth, the obtained results are considered as non-critical for all three part numbers, since during manufacturing of the evaluated TVs in the first step, no specific manufacturing provisions to improve CAF/HAST behavior have been applied. Available experiences show that with special provisions—as regularly applied in mass produc-

tion—a significant improvement of the electrochemical migration behavior can be achieved.

Conclusion

The smartphone market is constantly driving producers of PCBs to reduce board thickness. For an eight-layer board in a modern mobile phone, an any-layer design is considered as almost mandatory, while the thickness target is currently at 600 μm for this kind of stack-up, and it dropped to 400 μm for a rigid eight-layer board in 2013.

Current research has shown that with the currently available materials and manufacturing processes, it is possible to build rigid any-layer PCBs featuring a build-up of eight layers with a maximum thickness of less than 500 μm .

To implement these boards, different manufacturing approaches were successfully applied: a high-end HDI process combined with via-filling step, and the ALIVH technology. Additionally, it was shown that the combination of pure ALIVH with outer layer HDI, the so called ALIVH-C process, could be successfully applied. Board thicknesses between 443 and 512 μm were manufactured. AT&S has almost 20 years of experience in HDI, and began licensing ALIVH technology in 2011. Thus, ALIVH technology in particular promises still additional potential for improvements in manufacturing of thin boards.

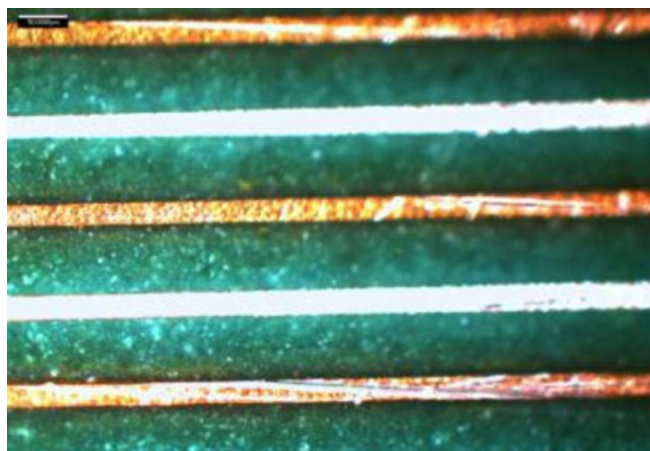


Figure 16: Microscopic darkfield illustration of comb structure on TV3 Layer 1, solder mask layer removed by grinding.

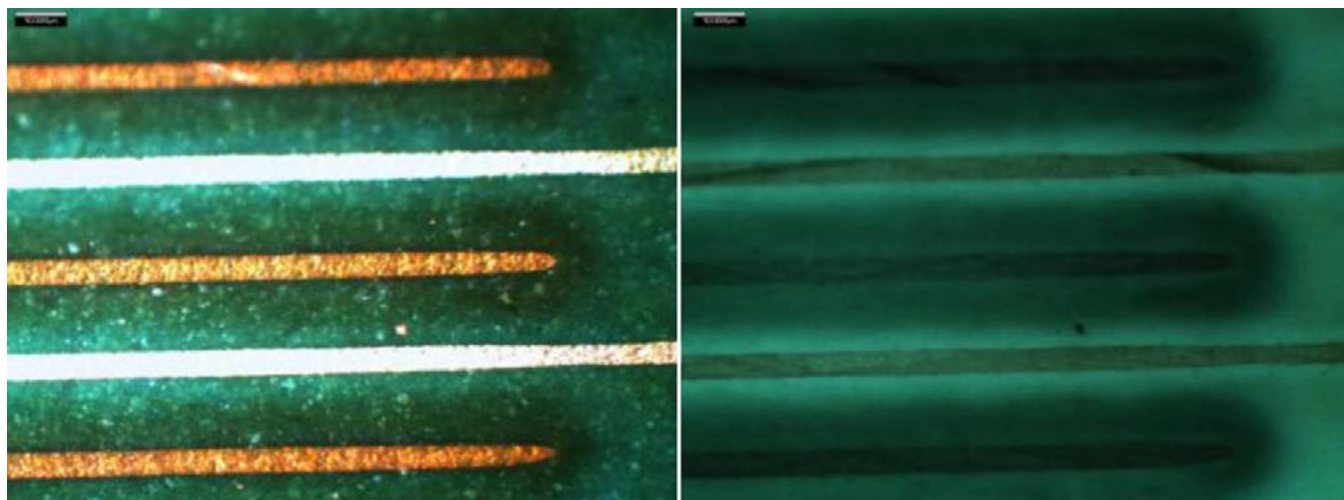


Figure 17: Microscopic illustration of comb structure on TV2 layer 8, solder mask layer removed by grinding, left view darkfield, right view with UV lamp.

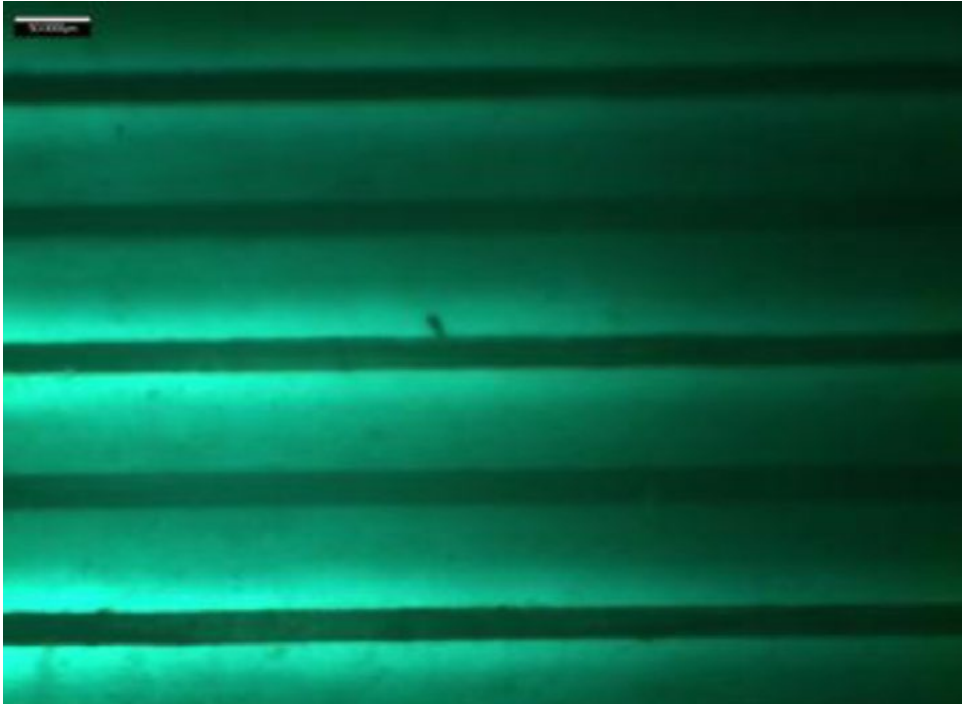


Figure 18: Identified copper dendrite on TV2 layer 8, solder mask partially removed by grinding, UV lamp applied.

The reliability behavior of the samples built during this study is overall considered as acceptable. Currently the material situation for the HDI process can be considered as advantageous compared to the materials situation for the ALIVH process. While this is specifically true for the reflow sensitivity behavior the observed difference in performance of the three produced test vehicles was lower for the electrochemical migration in the HAST test. Finally the temperature cycling of the parts did not cause any failure during this study.

It can be concluded that all observed technologies are generally feasible for building reliable thin boards. Further work will have to focus on potential to meet functional requirements, such as the electrical performance and the economic questions that are corresponding to the manufacturing of these very thin boards. **PCB**

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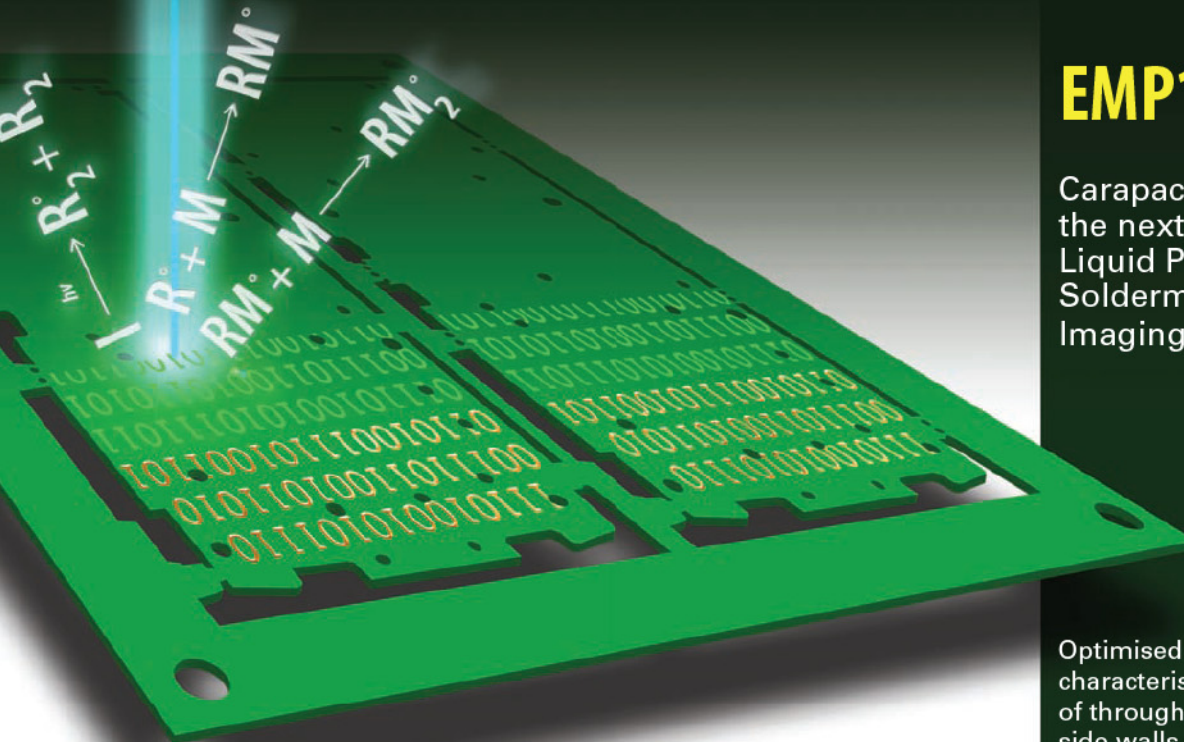
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This paper originally published in the IPC APEX EXPO 2013 Conference Proceedings, under the title, Reliability Performance of Very Thin Printed Circuit Boards with regard to Different Any-layer Manufacturing Technologies. Some images were omitted.

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THE SMART GRID OPPORTUNITY

by Bill Burr
BPA

Abstract

The growing demand for electrical power coupled with aging infrastructure is placing considerable strain on the electrical power grid. In addition, migration of electric power generation to the periphery of the grid is presenting new challenges for load balancing and synchronization. The continuing need for greater efficiency in electric power utilization and control also means that control systems are in the process of migrating towards individual loads. As a result, greater intelligence is required throughout the grid, from point of power generation to point of power consumption. This combination of power and intelligence is presenting both challenges and opportunities to the electronics designer: challenges because small, cost-effective intelligent power management modules need to combine digital logic with mains power, and opportunities because new and innovative board level technologies will be required to meet this challenge.

What is the Smart Grid?

The electric utility industry is transforming from a unidirectional commodity business where power flows one way from producer to consumer toward a services-oriented business in which customers are both producers and consumers. In addition, economic imperatives, ecological concerns, and an aging infrastructure demand improvements in generation and transmission efficiency, as centralized load balancing in the current grid requires standby capacity which represents additional capital and operational costs. This new configuration involves active demand side management in addition to the supply side management formerly done through passive metering systems. Consumers will be making choices as to how, when, and from whom they purchase electricity or provide demand reductions, and whether to become producers themselves. The addition of IT intelligence to the power generation and transmission network necessary to make this all happen has given rise to the term smart grid.

While much of the activity connected with the smart grid concept is concerned with inte-

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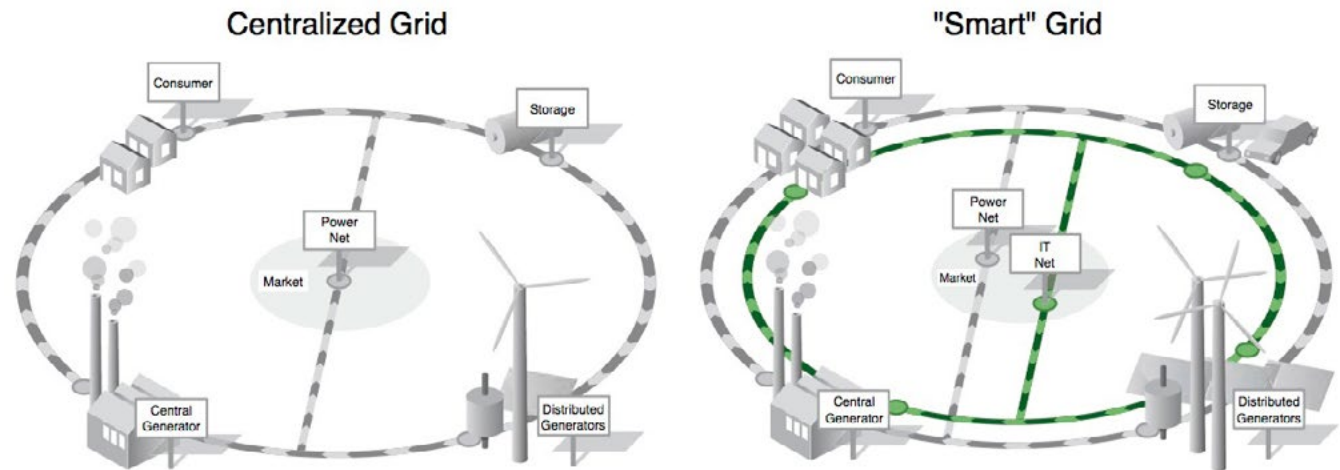


Figure 1: Power grid evolution. (source: Smartgrids Austria)

gration of distributed power generation into the grid and load balancing through the introduction of parallel IT infrastructure as shown in Figure 1, the introduction of intelligence out on the periphery (i.e., at point of consumption) and distributed generation basically involves the creation of active crosspoints. These have to be capable of controlling power either in the form of supply or demand, thereby providing improved stabilization of the network from the periphery inward.

For example, a point-of-use power management system has to communicate with other crosspoints, sense the local load, and provide additional demand side management through direct load control of devices such as hot water heaters, air conditioners, thermostats, and other appliances, as well as to reduce the overheads involved in switching electrical utilities providers (electrical service providers, or ESPs) where retail choice exists. Distributed intelligence in the form of smart meters (also known as remote terminal units or RTUs) also enable ESPs to reduce operating costs and enhance their responsiveness with such capabilities as outage detection and remote connect/disconnect functionality. Smart meters make it easier for ESPs to offer net metering and feed-in tariffs for customers who own generation such as rooftop solar, where policies exist to promote the adoption of such systems.

Sensors along the transmission and distribution system allow grid operators to know the

condition of the grid at any given location, and advanced meters and load control devices as well as appliances that can respond to signals from the grid-based on load conditions require current sensing and control.

Therefore, at the edges of the grid, demand side management will be in the form of a power control computer with autonomous communication capabilities either via wireless or broadband-over-powerline. This means that control logic will meet mains voltages through metering/consumption monitoring and load regulation. These applications confront the designer with problems which usually are partitioned into separate subsystems: digital logic, communications, and mains voltage (240VAC)/medium current (20–90A) sensing/switching.

The Opportunity

To be effective, the smart grid needs to involve every point of generation/load. And on the load side it has to approach consumer electronics price points to bring it within reach of the greatest number of users. Although timing of the rollout of smart grid infrastructure will vary from region to region depending on saturation and the regulatory environment, BPA expects worldwide shipments of smart meters will peak in 2018 at some 125 million units annually, declining to 110 million by 2022, as shown in Figure 2.

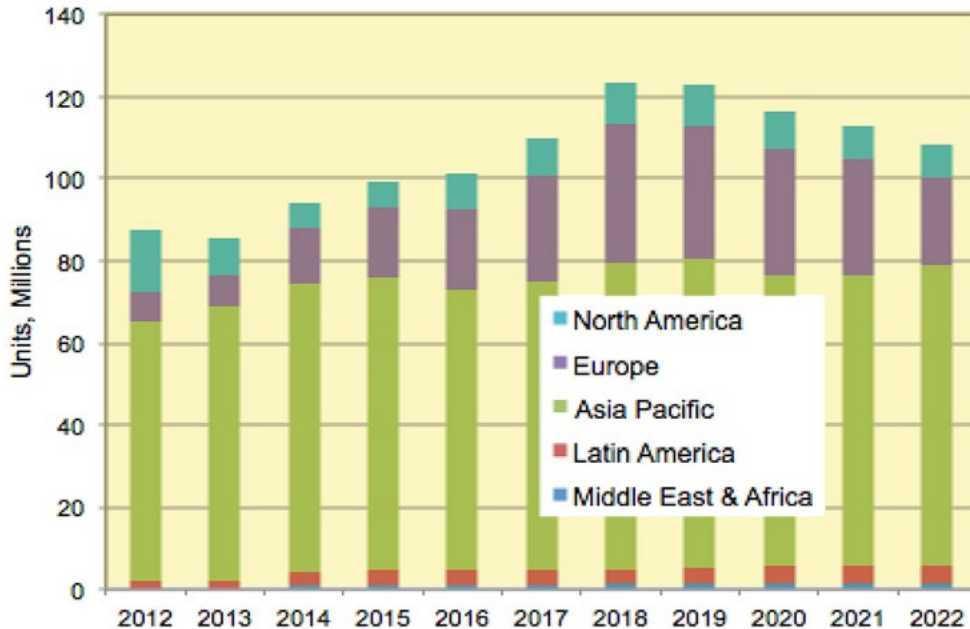


Figure 2: RTU worldwide build-out in millions of units. (source: BPA Consulting, Telefonica)

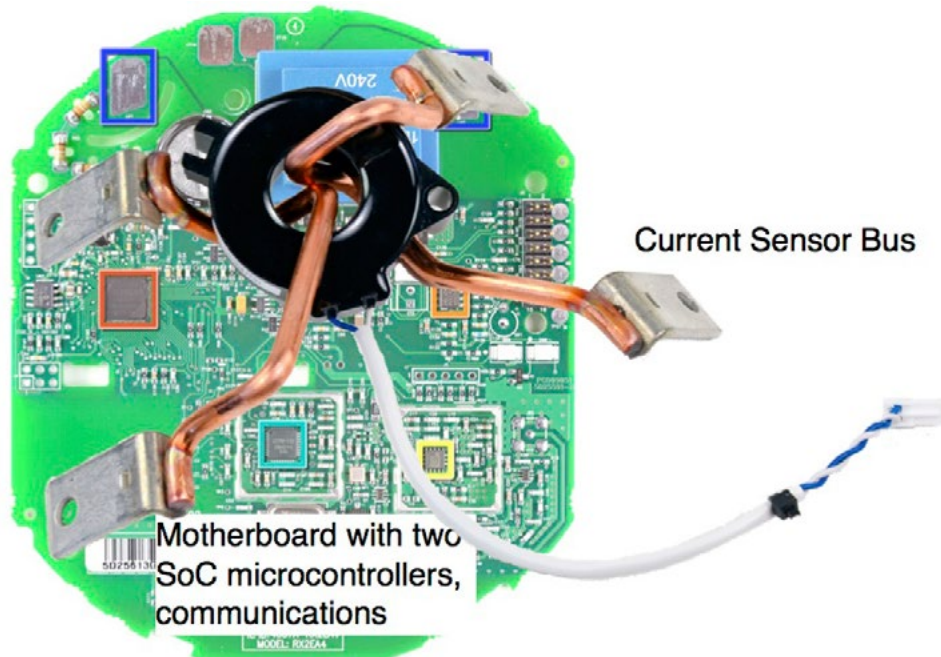


Figure 3: First generation smart meter. (source: BPA composite, iFixit)

The Challenge

AC power management involves three basic functions: current sensing/ measurement, phase detection/synchronisation, and switching. While load sensing has been an electromechanical process for decades in the form of the

trusty electric meters found in every older installation, the need for communications as well as demand-side load control represents a new challenge. Current designs have basically retained the heavy shunt/sensor hardware while adding communications and control logic (Figure 3).

In addition to the added complexity in BOM (bill of materials) these represent, providing the current sensing function involves assembly of a number of discrete elements, adding both cost and physical bulk. Therefore designers are looking for alternatives within a more highly integrated system. Although printed wiring offers an alternative in the same way as circuit boards replaced discrete wiring in the 1950s, the problem is that the mains load current must transit the assembly requiring a much larger conductor cross-section than is standard with printed circuit processes.

The MiB Solution

The need for communications as well as demand-side load control represents the combination of intelligence and power provided by metal in the board (MiB) printed circuit technology.

The solutions that are emerging offer the potential for replacement of hardware and components formerly used to manage heat and power, and range from simply providing a metal base

in the board for heat dissipation to sophisticated solutions combining thermal and power management with high-density interconnect and formability. As a term, metal in the board is coming into general use, because these solutions are not metal core or metal base; they are metal in the board.

The manufacturing technologies and capabilities of MiB range from simple three layer buildups commonly known as Al-based or insulated metal substrate to complex assemblies using a variety of techniques to provide low thermal and electrical resistance pathways in the board. In every case, the MiB component is providing additional functionality—thermal and/or power management. In addition to load sensing, the other primary challenge for the RTU is load switching. New generations of power semiconductors are emerging in response to the need for intelligent power management across an expanding range of applications, from automotive through renewable energy harvesting, appliances, solid state lighting, and RF power.

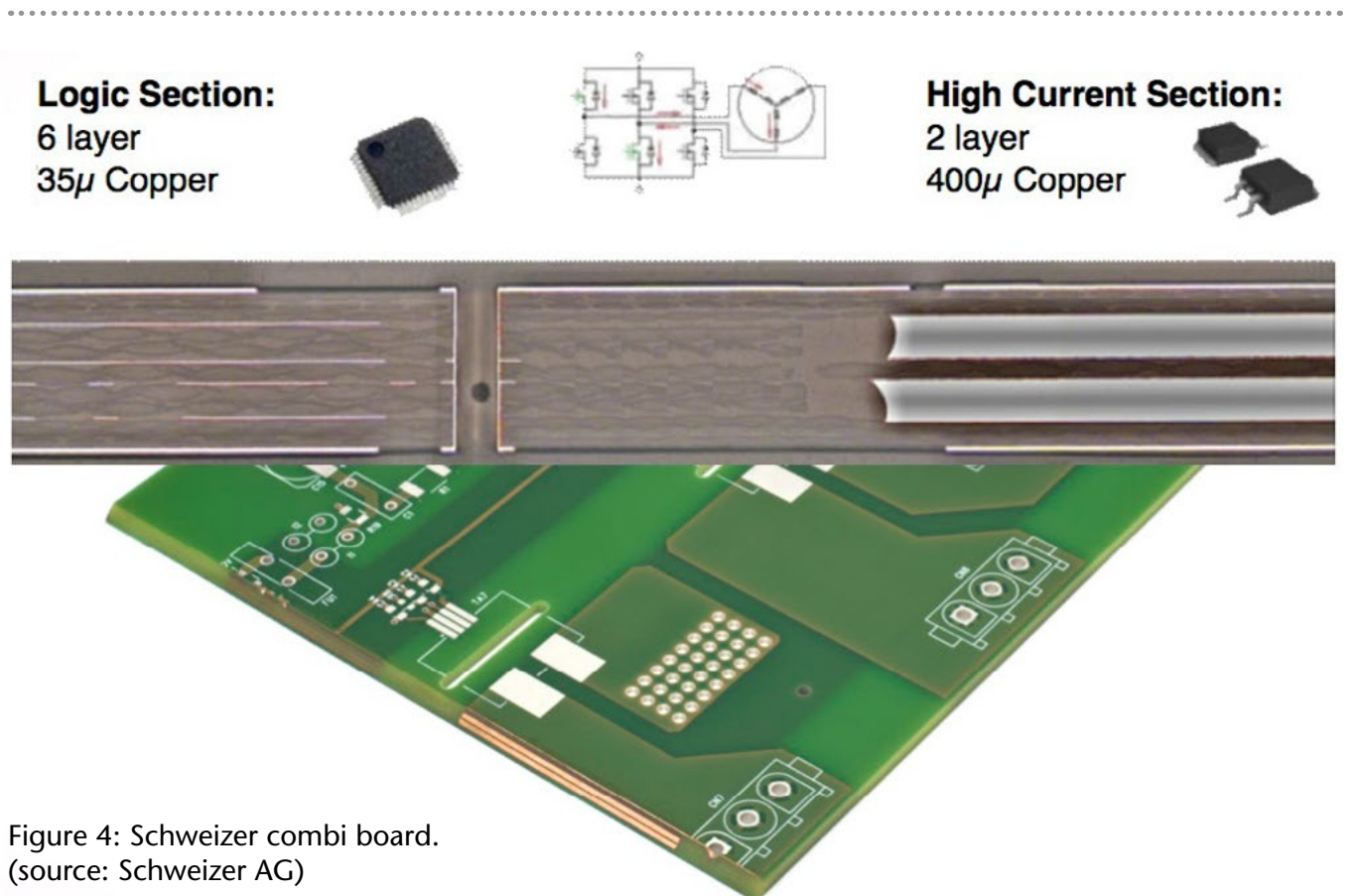


Figure 4: Schweizer combi board.
(source: Schweizer AG)

All of these applications share the same objective—the efficient and economical management of power. Heavy, bulky electromechanical relays are being replaced by IGBT or MOSFET switches, and these same devices are also used for power control through pulse width modulation of IGBT or MOSFET power stages.

The problems faced by peripheral RTUs in smart grid systems are identical to those involving digital power—the need to carry and control loads up through 24KVA. The MiB types generating the most interest are the thick copper multilayer and discrete wire types and their variants, providing current management capabilities well in excess of the ranges needed for domestic appliances and utilities such as air conditioning and hot water heating.

One of these, Schweizer's combi board, is shown in Figure 4. This structure combines thick and thin copper on the same layer, addressing the limitation of conventional thick copper MiB types where all the copper on either external or internal layers is the same thickness. The result

is a “selective” technology, where heavy copper is used only where needed. Therefore, in addition to the cost benefits of selectivity, the combi board enables integration of logic/control and current sensing into the same board.

This level of integration is also achievable with discrete wire technologies. Häusermann's HSMtec® and Jumatech's WireLaid® provide the ability to embed 0.5 mm thick copper strips (profiles) and copper wires within the board as shown in Figure 5.

The profiles and wires which make up the MiB components in a discrete wire board are bonded to tracks etched on innerlayer cores, basically forming a sandwich consisting of the etched track and the bonded elements. This patented process ensures a consistent bond line between the track and the wire/profile which is essential for uniform heat spreading and consistent conductor cross-sectional area. It also simplifies the layout task and/or conversion from conventional designs, as placement of the high current MiB components: The wires and profiles

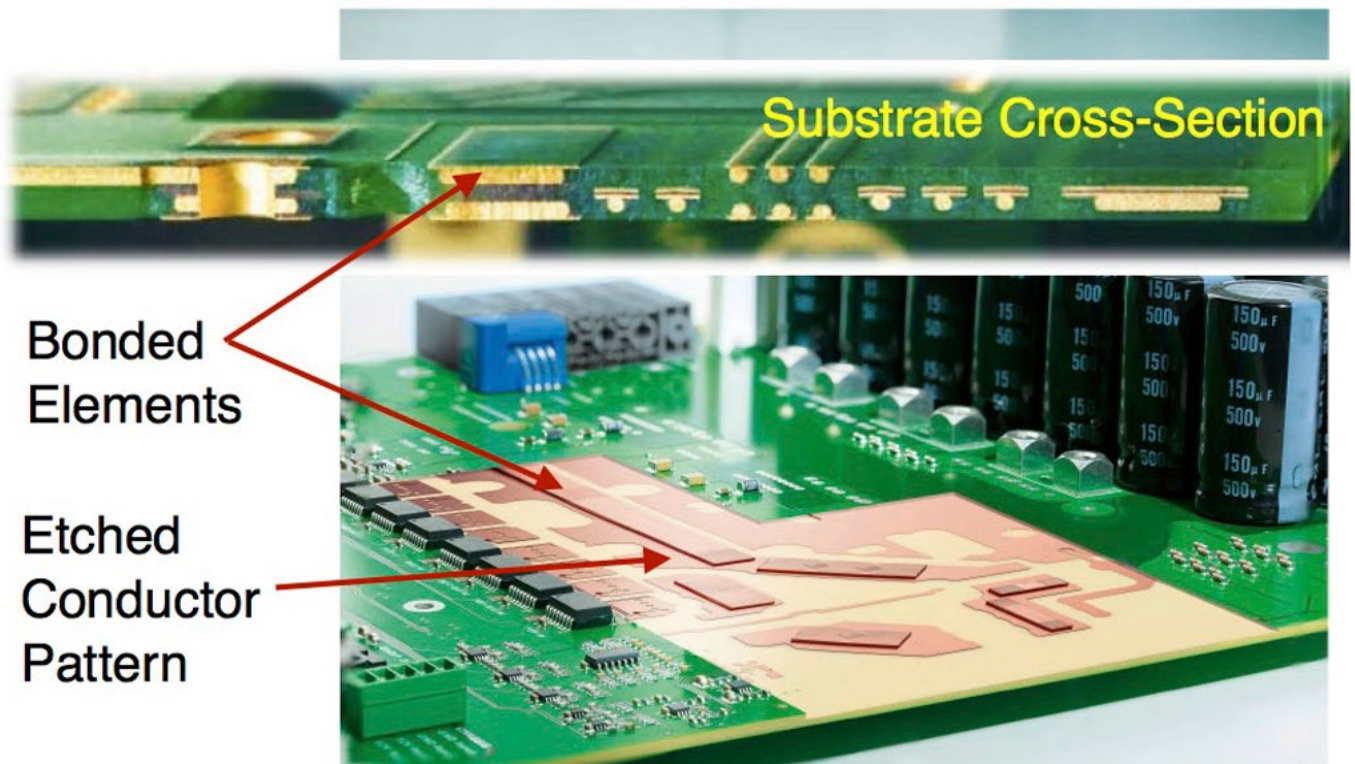


Figure 5: HSMtec layout. (source: Häusermann GmbH)

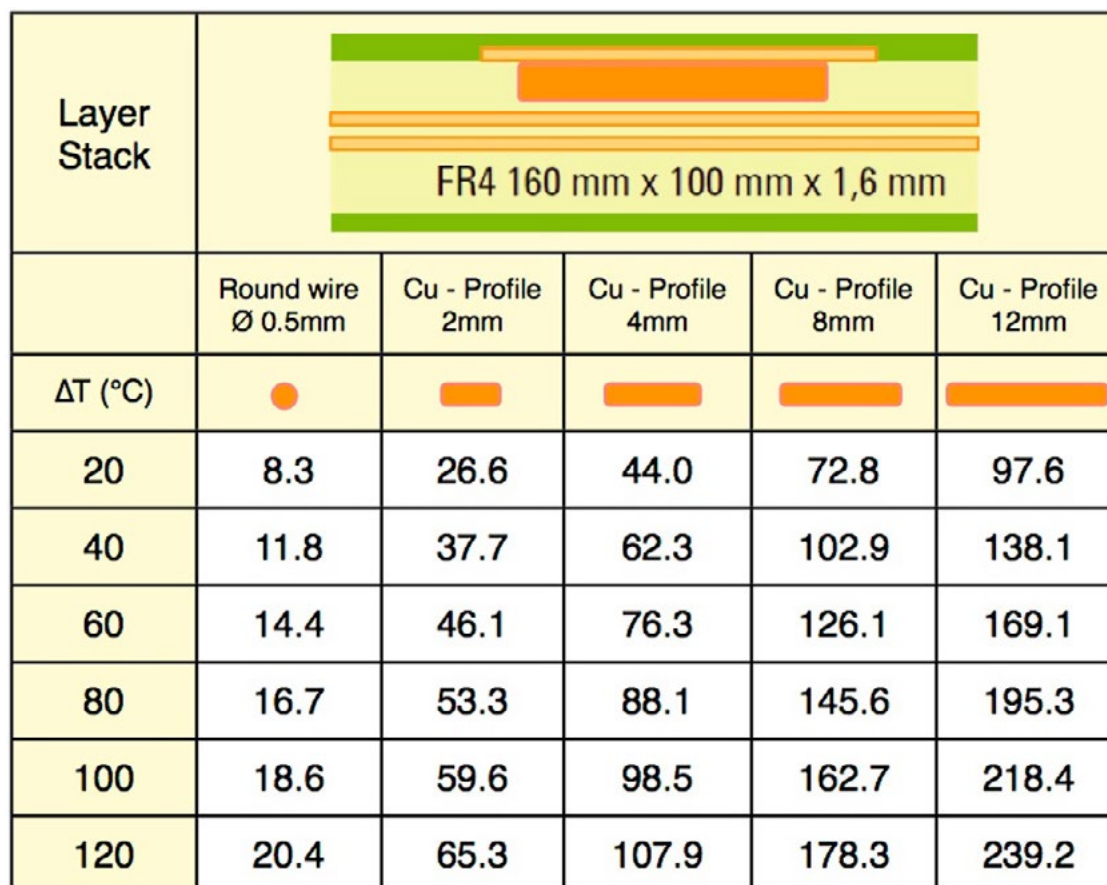


Figure 6: Temperature rise vs. current for four-layer stackup. (source: Häusermann GmbH)

will be done on what are essentially enlarged tracks on an inner or outer layer.

This arrangement provides a great deal of flexibility in stackup configuration. Profiles/wires are bonded to a routing track, and thermal dissipation planes can be located on the same layer or on a facing layer co-axial with the MiB track. Ampacity data based on actual thermographic observations of different layout configurations as shown in Figure 6 shows the suitability of discrete wire types for medium power applications with nominal currents of 5 to 150A (40°C temp rise). Depending on the individual requirements for temperature rise and thermal management strategies this value can easily run to over 400 Amps.

The current carrying capability, heat-spreading characteristics, and design versatility of these MiB types are directly applicable to the challenges of functionality and cost presented by smart grid RTUs.

Conclusion

Smart grid RTUs are a rapidly growing opportunity with the need for a combination of digital communications and control of mains power at consumer electronics price points. Conventional solutions involving discrete AWG6 wire, busbars, and electromechanical relays will not meet the cost, reliability, and performance needs of distributed intelligent systems. The solutions offered by MiB technologies provide the flexibility and integration necessary for the marriage of intelligence and power necessary to realize the potentials inherent in the smart grid concept. **PCB**



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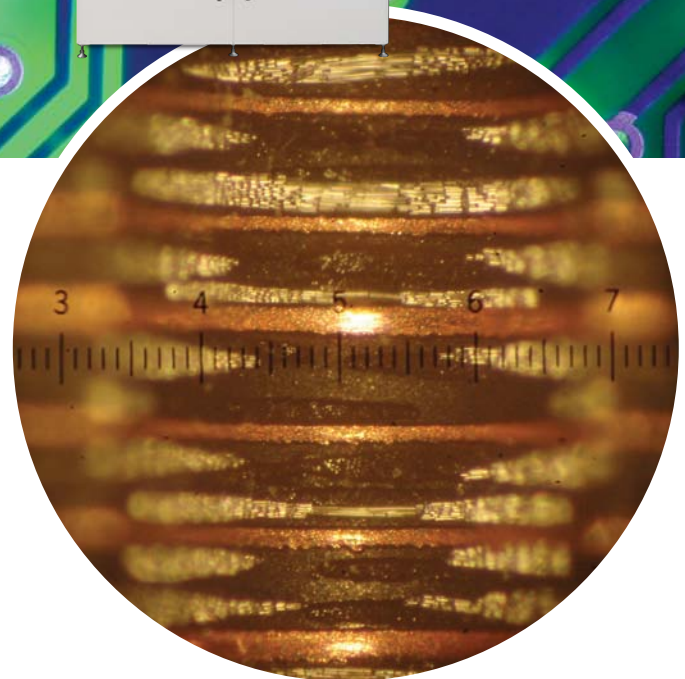
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A joint conversion project has successfully tailored the dielectric properties of Isola's high-performance I-Tera MT laminate material to match the properties of an incumbent product.

Techno Service Installs Ucamco Imager

With this new three-head imager, Techno Service strengthens its commitment to its customers, offering top-quality PCBs at a competitive price.

Advanced Circuits Completes Isola's Certification Program

ACI was audited by Isola's technical services team to validate ACI-Tempe's manufacturing operations against the standards established in the IPC-A-600 Acceptability of Printed Boards and the IPC-6012 Qualification and Performance Specification for Rigid Printed Boards.

Xcerra Delivers Strong Q4; PCB Test Systems Gain Share

Xcerra Corporation has announced financial results for its fourth fiscal quarter ended July 31, 2014. Net sales for the quarter were \$124,327,000, compared to the prior quarter net sales of \$105,424,000. GAAP net income for the quarter was \$13,514,000, or \$0.27 per diluted share.

GCT Posts 36% Growth in 1H; Welcomes Nierada

GCT GmbH in Weingarten reported an on-year net sales increase of 36% in the first half of 2014, which is 17% above their own target fig-

ures; GCT appoints Markus Nierada as production manager for the diamond coating department.

Technic Launches Technology Support Hub

Technic is pleased to announce the official opening of the Technology Support Hub portal on our three global web sites in North America, Europe and Asia. With the Technic TSH, registered users will be able to access disparate and extensive resources designed to make our products easier to use and to enable our customers to design better process solutions.

Isola Now Meets ESA's Base Material Standard

Karl Stollenwerk, European president, commented, "We were pleased to confirm our ability to comply with the new requirement. The high-reliability sectors, including aerospace, are important segments of our business, and we are committed to a process of continuous improvement to satisfy, or exceed, the ever-increasing demands of our customer base."

Intercept Strengthens Canadian Representation with Kaltron

"Kaltron is delighted to offer Intercept's PCB, Hybrid IC, and RF software solutions to our customers in Canada. They complement very well our existing portfolio of design services, components, and modules," said Tom Martin, president of Kaltron.

Xcerra's Pricing of Public Offering of Common Stock

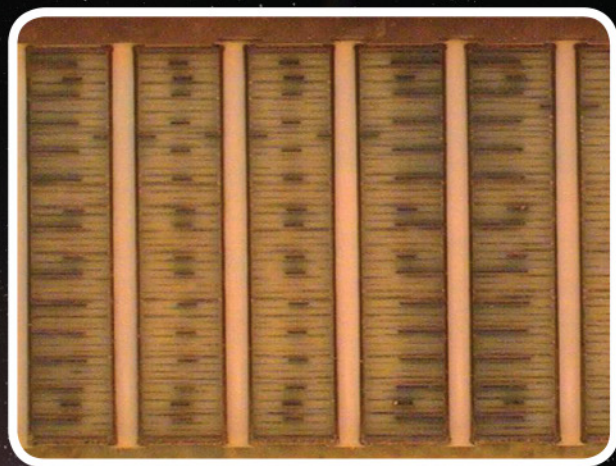
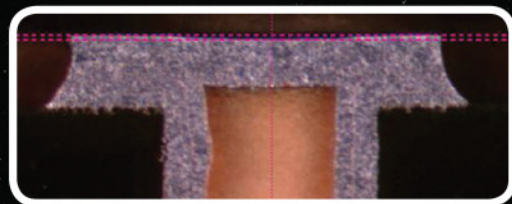
Xcerra Corporation announced the pricing of an underwritten public offering of 4,682,927 shares of its common stock at \$10.25 per share. Xcerra has also granted to the underwriters a 30-day option to purchase up to an aggregate of 702,439 additional shares of common stock to cover over-allotments, if any.

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Oxide Alternatives to Enhance LPI Adhesion to Copper

by Michael Carano

OMG ELECTRONIC CHEMICALS

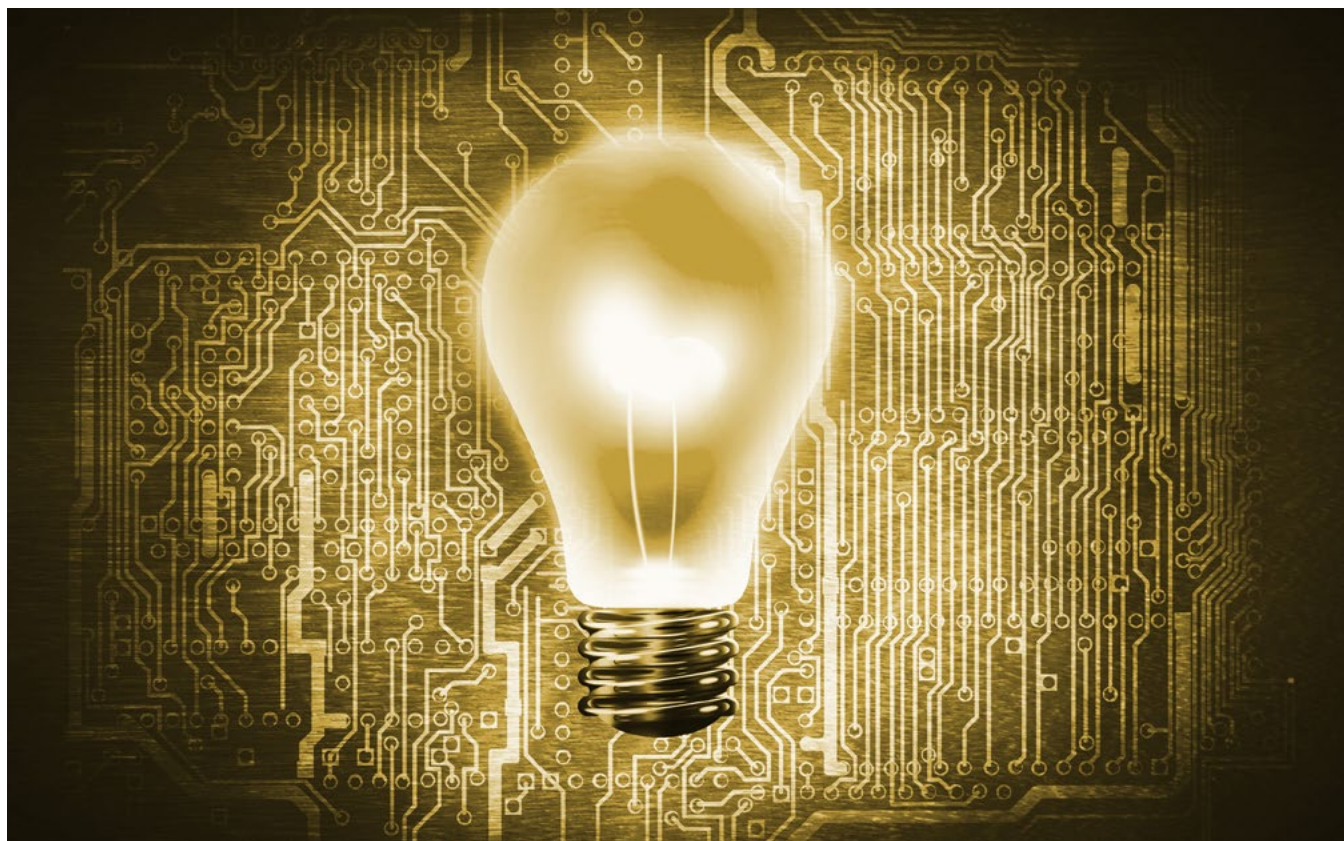
Introduction

The printed wiring board industry has experienced issues with liquid photoimageable solder masks under various conditions. LPI breakdown or lifting near the copper-mask interface typifies a common defect seen when fabricators institute electroless-nickel immersion gold (ENIG) as a final finish. The aggressive nature of the ENIG process is a particular nuisance for some aqueous based LPIs. Simply scrubbing the copper surface prior to soldermask application is often not an effective adhesion promotion mechanism for LPI and ENIG. (Please note that not all LPIs exhibit this problem.) A number of factors contribute to mask adhesion issues in-

cluding acrylate content of the LPI, degree of cross-linking, mask thickness, and adhesion strength of the mask to the surface. Regardless, surface topography plays a unique role in enhancing the adhesion of the LPI. Before exploring surface topography further, it is important to understand outside influences such as ENIG and its effect on adhesion.

Influence of Plating Processes on LPI Adhesion

The electroless-nickel immersion gold plating process places significant stress on the liquid soldermask's adhesion to the circuit board surface. Generally, there are several things the



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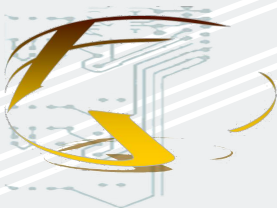
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fabricator can do to ensure proper solder mask adhesion. Of course, proper surface prep is one of them. However, these other critical success factors are important (and will be presented in a future column):

- thoroughly pre-cleaning of the substrate
- ink layer thickness
- complete pre-drying of the LPISM
- exposure energy

- correct adjustment of the developing parameters
- control of the corresponding final curing conditions

Surface Prep of Copper Prior to Soldermask

In Figure 1, the surface copper of the PWB was prepared with aluminum oxide. Even though the surface roughness appears sufficient, the fabricator experienced issues with LPI breakdown after ENIG. Figure 2 shows the mask peeling from the surface due to marginal adhesion. Most likely, even with less than adequate surface preparation, most surface finishes would not have had such an adverse effect as ENIG.

While the above case is extreme, it nonetheless illustrates that marginal mask adhesion leads to yield loss for fabricators.

Surface preparation must be optimized to improve mask adhesion. One solution is to eliminate scrubbing (either pumice, AlOx) and utilize the oxide alternative (organo-metallic) adhesion promotion system. The surface topography that is achieved on plated copper outerlayers with this process is shown in Figure 3.

The topography represented in Figure 3 is remarkable simply because the copper surface is electrodeposited copper (from acid copper electroplating process). The electrodeposited

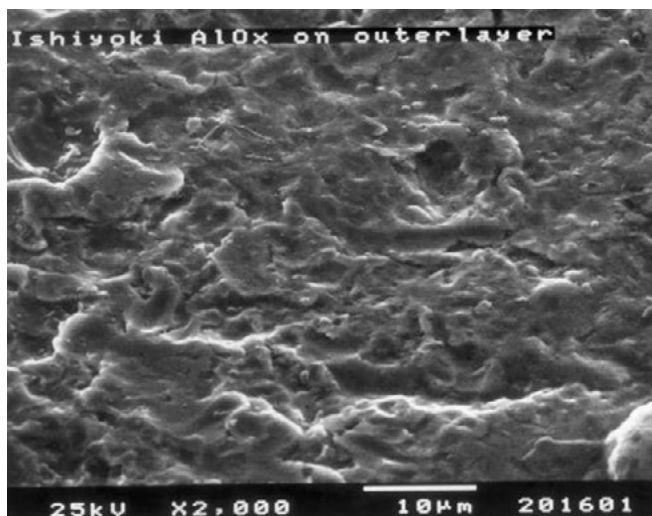


Figure 1: Copper surface outerlayer prepared with aluminum oxide prior to LPI.

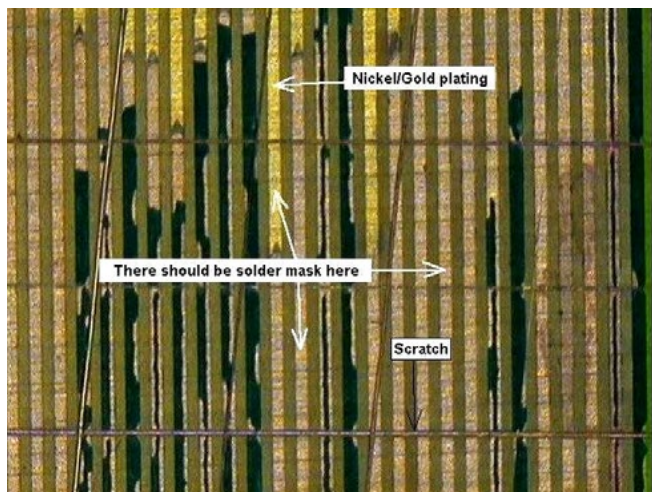


Figure 2: Severe peeling of LPI after ENIG. The above panel treated with aluminum oxide (Figure 1). Mask lifting noted after processing through ENIG.

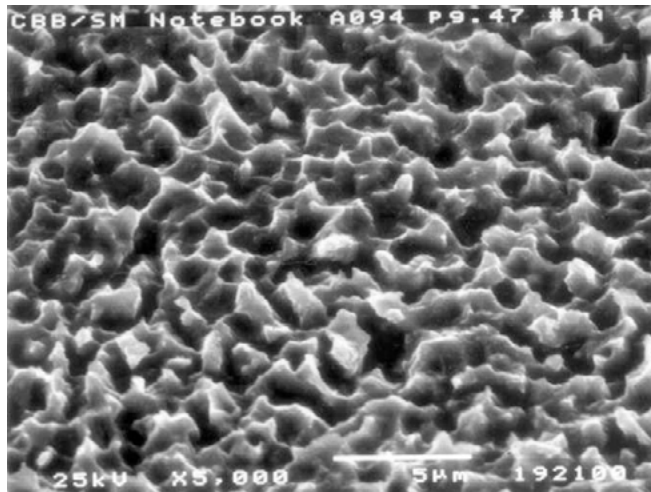


Figure 3: Oxide alternative process as an adhesion promoter for soldermask.

Process	Rp-v	Rms rough	Ave rough	Median Ht	Mean Ht
Oxide alternative	3.52 um	0.54 um	0.438 um	1.44 um	1.48 um
Scrubbed surface	2.9 um	0.298 um	0.235 um	1.44 um	1.43 um

Table 1.

copper is typically a fine-grained amorphous deposit (due to the use of organic grain refiners and brighteners) and is more resistant to etch attack as opposed to the foil (lamine) copper represented by a columnar grain structure.

Certainly it is advantageous to use a soldermask that has good adhesion properties as well as resistance to final finish plating solutions such and ENIG and immersion tin.

In Table 1, one can see the surface roughness profile as measured with profilometry. The data supports the assertion that oxide alternative process technology provides an overall surface roughness that is an improvement over conventional means.

Possible Objections to Using Oxide Alternatives

With so many different solderable finishes in use today, it is critical that the soldermask

adhere to the surface regardless the final finish process used. It is also true that with a number of different firms marketing soldermasks, not all LPI's are created equal with respect to adhesion. So it is even more critical to ensure that the surface of the copper offers an effective roughness profile. However, there are concerns that excessive roughening may lead to unexposed soldermask residues that are not able to be effectively removed in the development process. A second concern is that due to the action of the oxide alternative, there is an organic layer co-deposited on the copper surface. Thus, the non-coated soldermask features (pads and vias) show the effect of the organo-metallic coating. This coating is beneficial in that it enhances the bonding of the soldermask to the surface. The objection may be that the organic coating is light to dark brown in color. Not to worry, as the coating is easily removed in an acidic chemical step as is used during the final finish plating process. Even if the coating is left intact, there is no evidence that the coating adversely affects the final finish plating process.

With respect to concerns of soldermask residues remaining embedded into the roughened copper surface thereby interfering with plating processes, this is not an issue. The key, like all chemical and mechanical processes for PCB fabrication, is process control to ensure that you don't have trouble in your tank. **PCB**



Figure 4: No peeling of LPI after ENIG. The panel was treated with oxide alternative chemistry (Figure 3).



Michael Carano is with OMG Electronic Chemicals, a developer and provider of processes and materials for the electronics industry supply chain. To read past columns, or to contact the author, [click here](#).

PCB007 Market News Highlights



LED Industrial Lighting Market: CAGR of 29.64% by 2018

According to the report, the need for energy-efficient lighting solutions is one of the key drivers in the market. Increased concern over the depletion of non-renewable sources of power and the need to minimize power consumption are driving the demand for LEDs in industrial facilities.

Report: Smart Glass and Flexible Display Industry

The analysis shows that the total flexible display market is projected to reach the market revenue worth \$3.89 billion by 2020. The value of smart glass market was worth \$1581.4 million in 2013, and is expected to reach \$5814 million by 2020, at an estimated CAGR of 20% from 2014–2020.

Near-field Comms Market to Reach \$20.01B by 2019

The global market for NFC, in terms of revenue, was valued at US \$1.07 billion in 2012 and is estimated to grow at a CAGR of 43.7% during the forecast period from 2013–2019.

China Leads 2013 Smartphone Market: 700M Users

With active smartphone users exceeding 700 million by the end of 2013, China has now become the largest smartphone market in the world. Demand for smartphones in China is expected to cross 400 million units in 2014 with more than half of the units being contributed by local vendors.

\$8 Billion Market for Wearable Electronics by 2018

The global wearable electronics market is expected to cross \$8 billion in 2018, growing at a healthy CAGR of 17.7% from 2013 to 2018.

European Semiconductor Sales Up 14.9% in July

Sales of semiconductors in July 2014 amounted to US \$3.273 billion in Europe, an increase of 14.9%

compared to the same month in 2013, the European Semiconductor Industry Association (ESIA) announced on the basis of the latest WSTS sales reports.

Homeland Security Market to Reach \$364B in 2020

Initiatives undertaken by various governments across the world are driving the market for homeland security products. Some of these government initiatives include Sisfron program undertaken by Brazil, TECS Mod program undertaken by the U.S., and Project Cytoon undertaken by South Africa, among others.

Facial Recognition Market to Reach \$6.50B in 2018

The global facial recognition market is estimated to grow from \$1.92 billion in 2013 to \$6.50 billion in 2018. This represents a CAGR of 27.7% from 2013–2018. In the current scenario, government and utilities are expected to be the largest adaptor for face recognition technology.

27% of U.S. Households Use a Connected Health Device

Research from Parks Associates shows more than 32 million U.S. consumers will actively track their personal health and fitness online or via mobile by 2016. If Apple's watch incorporates breakthrough wellness and fitness tracking functions and supports innovative partnerships with health industry incumbents, the market adoption could be much higher in the next few years.

Solar PV Power in Japan; Market Outlook to 2025

The report provides an in-depth analysis on global renewable power market and global solar PV market with forecasts up to 2025. The report analyzes the power market scenario in Japan (includes conventional thermal, hydro, and renewable energy sources) and provides future outlook with forecasts up to 2025.

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Best Practices 101: Part 3

by Steve Williams

STEVE WILLIAMS CONSULTING LLC

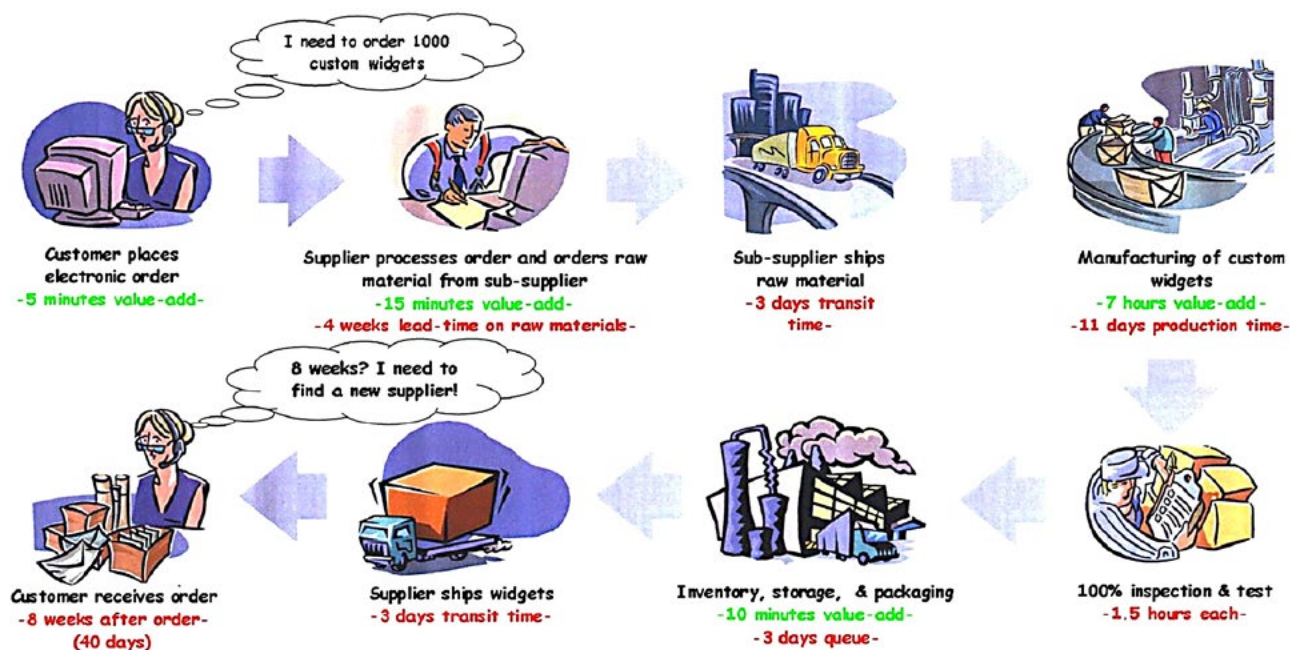


As we deep dive into the four critical steps of value stream mapping, (VSM), by now you should have a good understanding of just how powerful some of these tools and techniques can be. And the best part? It is not rocket science; it's just common sense!

Step 1: Identify the Proper Process

This step cannot be stressed enough because it is often overlooked by many companies new to Lean. Fresh out of training, the VSM team often runs out and starts mapping the first process they see. While VSM, if anything, is better than nothing, efforts should be focused on the critical processes having the greatest impact on the product.

Let's look at a typical supply chain transaction from the point of a customer order through delivery of the product. Figure 1 example shows a macro view of the supply chain cycle to illustrate how VSM works. This high-level view would be one way to drive Lean down through the supply chain to sub-suppliers. Of course, discrete processes within each supplier would need to be value stream mapped to enable reductions in their respective lead times. This product depicts a process with an eight-week lead time, which, after value stream mapping the process, reveals that there are only seven hours of value-added time on this product. As unbelievable as these results sound, most organizations experience a similar disparity in their processes. The



Time from PO placement to delivery: 8 weeks Non-value added time: 39 days Value-added time: 7 hours

Figure 1: Supply chain cycle.

Can you imagine CAM to etch in 5 minutes?

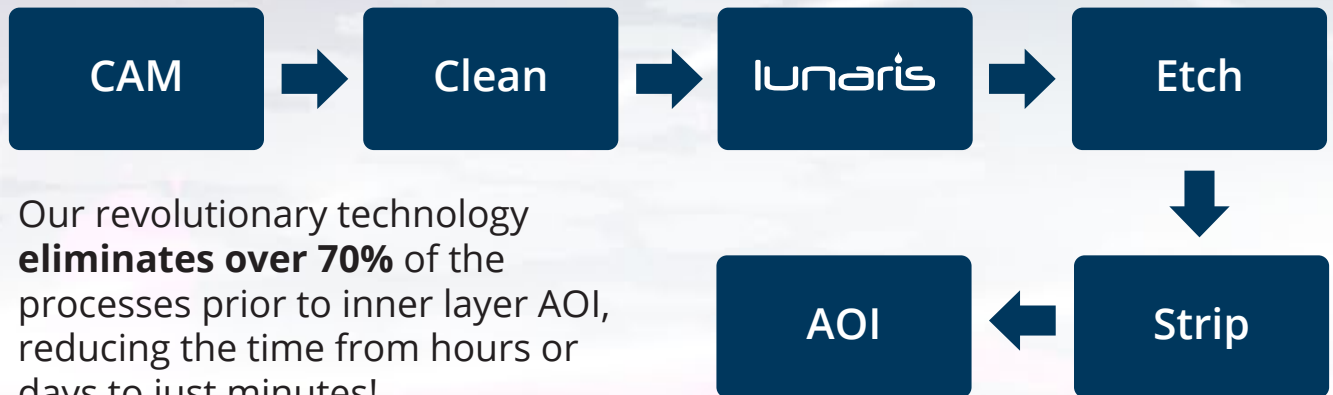
Meet Lunarix, the first fully digital inner layer printer based on inkjet technology.



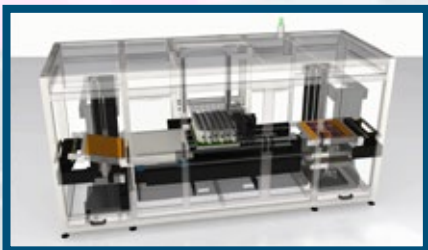
Inner layer production methods haven't changed much in over forty years. The basic process has remained the same: use lots of interdependent equipment and chemistry to completely cover a panel with photo resist. Then, use some more interdependent equipment and chemistry to remove most of it!

This is a timely, wasteful and costly process.
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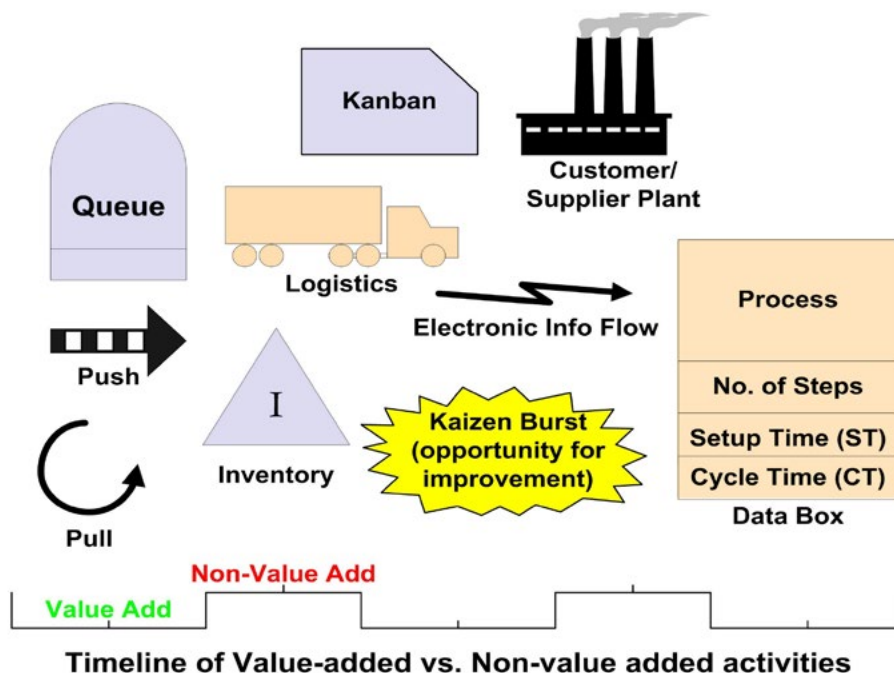


Figure 2: Value stream map symbols.

key takeaway of this scenario is that the excessive lead time has created enough customer dissatisfaction that the business is in jeopardy.

Step 2: Create a Current State Value Stream Map

Now let's turn this diagram into a current state value stream map. The original working session for developing a VSM is very manual, and as I mentioned earlier, is best done on a white board or with Post-it Notes. As the name implies, the goal is to find out how the processing is currently operating today, not how the SOP says things should be or how it was designed to be. The goal is to capture reality onto a piece of paper—the current state. Use a stopwatch for the time studies and determine the actual times where practical. While the VSM will eventually be finalized with software, the initial map should be created with Post-it Notes because there will be frequent changes as the team goes through this process. Once the process has been defined, the Post-it Notes map can be digitized with flowcharting software. Value stream maps use a variety of unique symbols that are not used in traditional flowcharts and diagrams, as shown in Figure 2. Word and Ex-

cel can be used for flowcharting, but for ease of use, professional flowcharting software like Visio should be used.

Step 3: Create a Future State Value Stream Map

Once the current state of the process has been established, which by the way, is usually the second "Ah-ha!" moment for the company, the next step is to picture the desired state of the process—the future state. This is the point where waste identified in the current state is targeted for elimination. Find the areas of waste and problem areas and try to eliminate them by looking for low-effort, high-benefit types of activities. Examples of these include:

1. Reducing unnecessary inventory
2. Pulling materials through visual controls
3. Using 5S to make materials and tools available at the point-of-use
4. Eliminating unnecessary step
5. Cross training personnel
6. Standardizing work
7. Reducing setup time
8. Balancing the work flow (Takt time analysis).

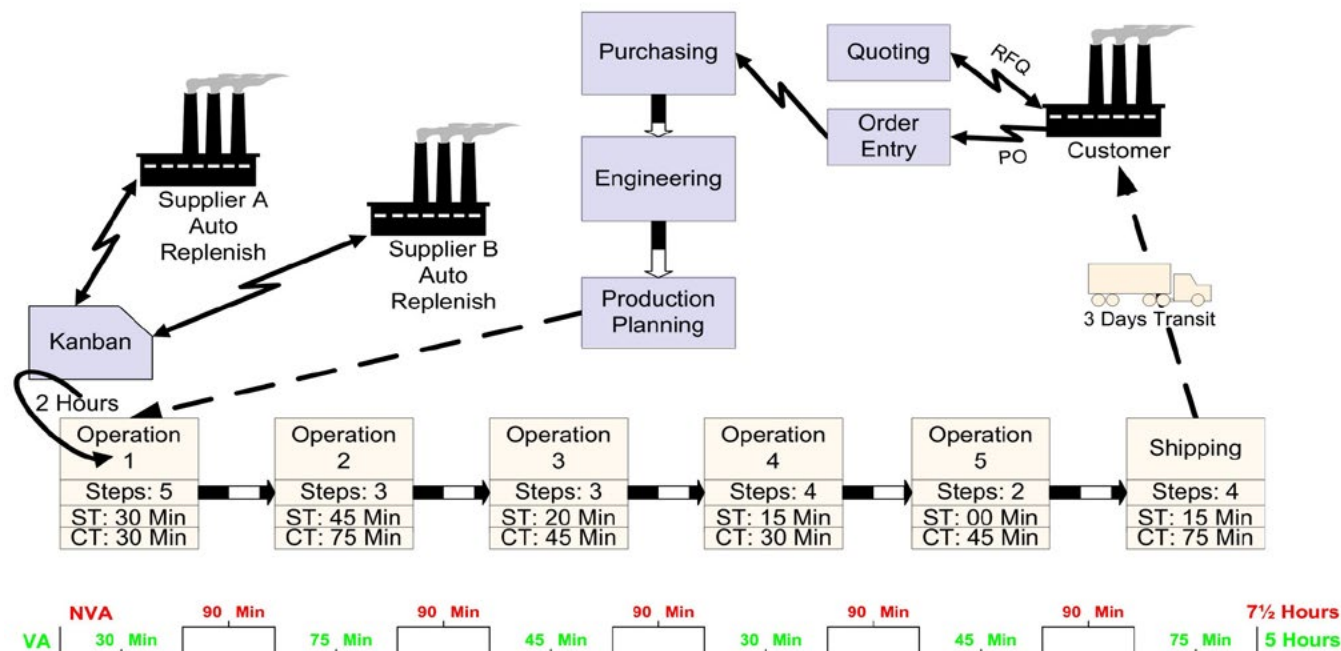


Figure 3: Future state value stream map.

Step 4: Create and Execute an Action Plan

An action plan is the method for transforming the process from its current state to the future state. The action plan for this process resulted in dramatic improvement, ultimately reducing the lead time to the customer from eight weeks to five days. This was accomplished in a number of ways, beginning with the implementation of a Kanban system at the raw material sub-supplier. Waste was minimized in the manufacturing process in three ways:

1. Elimination of inspection by placing quality responsibility at the source
2. Removing queue time by changing the flow from a push, to a pull process, and
3. Reducing the number of steps in each process.

All the results can be found in Figure 4. As the cycle repeats, further improvement could be achieved by implementing a Kanban system at the other end of the process—delivery of product to the customer.

	Current State	Future State
Total LT	8 Weeks	5 Days
MFG Time	17 Days	12 1/2 Hours
NVA	16 Days	7 1/2 Hours
VA	7 Hours	5 Hours

Figure 4: Waste reduction results.

This action plan was accomplished by using a combination of the best practices methodology that will be presented in my November column, Best Practices 101: Part 4. **PCB**



Steve Williams is the president of Steve Williams Consulting LLC and the former strategic sourcing manager for Plexus Corp. He is the author of the books, [Quality 101 Handbook](#) and [Survival Is Not Mandatory: 10 Things Every CEO Should Know About Lean](#). To read past columns, or to contact Williams, [click here](#).

Dry Film Photoresist Adhesion Tests

by Karl Dietz

KARL DIETZ CONSULTING LLC

Laminate construction, chemical composition of the copper foil surface and its topography, resist composition, lamination conditions, and hold times all affect dry film photoresist adhesion, conformation, and, ultimately PWB yields. This area has been studied extensively over the years.

A number of resist adhesion test methods have been employed to test different surfaces and process conditions with regard to dry film adhesion. The constant in such studies is a given dry film resist that is tested on different copper surfaces and under different process conditions. Conversely, one can keep the laminate construction and copper foil preparation as well as lamination conditions and hold times the same, while testing the adhesion characteristics of different films.

There are several failure modes, or sources of yield losses, if the copper surface is not properly prepared. Failure may be due to insufficient or excessive adhesion (Figure 1):

1. Failure to achieve good adhesion in a print-and-etch process will cause etchant attack under the resist and ultimately an "open" defect.

2. Failure to achieve good adhesion in a plating process will cause tin/lead underplating, ultimately leading to shorting defects ("shorts").

3. Failure to achieve good release of unexposed resist during development can cause etch retardation in a print-and-etch process, ultimately leading to shorts.

4. Failure to achieve good release of unexposed resist during development in a plating process can cause poor adhesion of the plated copper to the copper base (copper-copper peelers).

5. Failure to achieve good release of exposed resist in a print-and-etch process on innerlayers can inhibit the formation of copper oxide multilayer bonder (or alternative bonders) on such a copper surface.

6. Failure to achieve good release of exposed resist in a plating process can cause etch retardation.

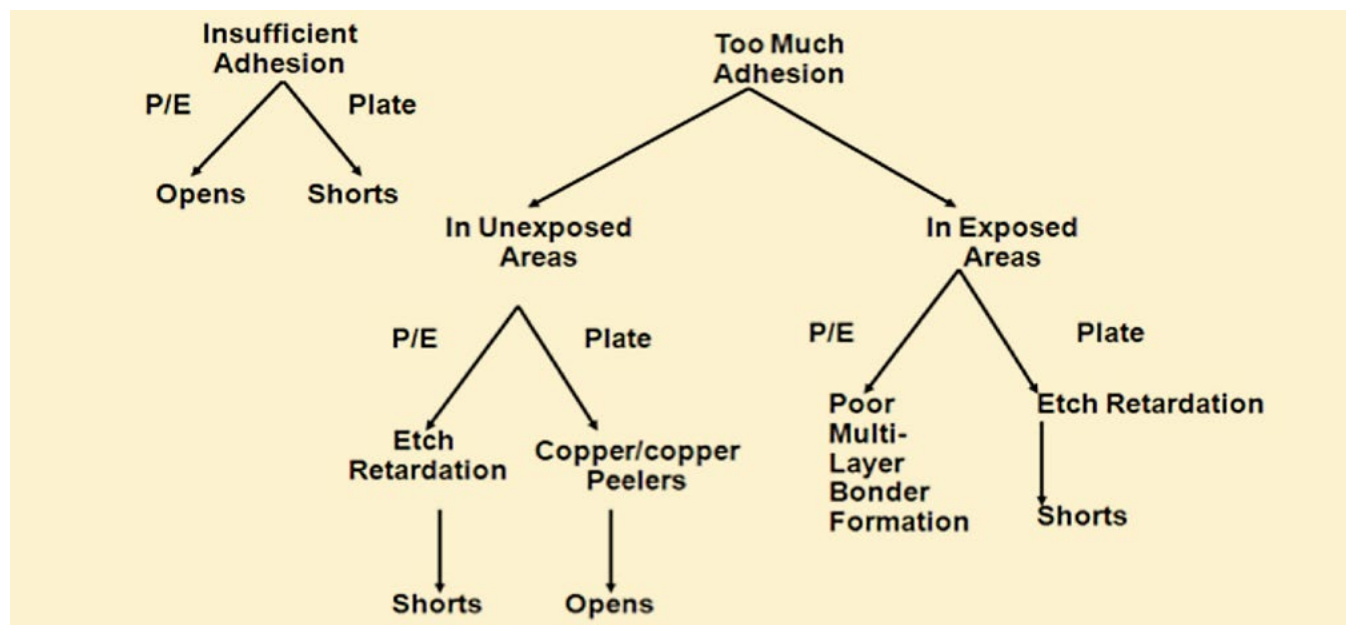


Figure 1: Failure modes due to insufficient or excessive adhesion.

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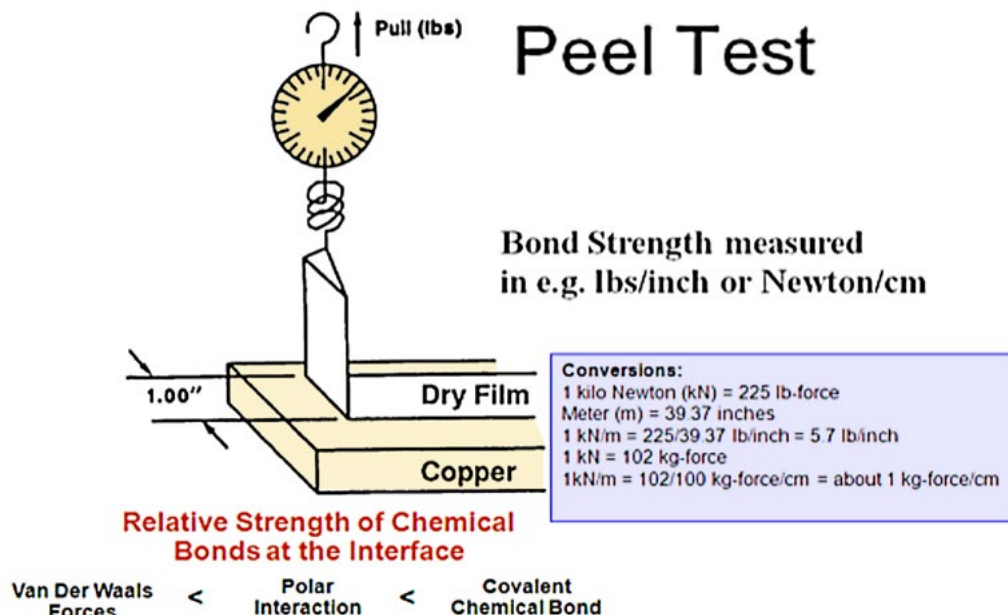


Figure 2: Concept of adhesion test by peel test.

Figure 2 introduces the concept of a peel test that measures dry film adhesion on copper. In reality, such a 90-degree pull test (e.g., with an Instron instrument) does not work with dry film, because the film will show cohesive failure before adhesive failure. This test arrangement is, however, used to test copper adhesion to the underlying dielectric.

Overview of Adhesion Tests

The effect of copper surface differences on dry film adhesion can be evaluated by the following criteria:

- Instant adhesion
- Resolution after development, as judged by
 - Minimum isolated line remaining (surviving development)
 - Minimum line/space resolution
- Survival of small resist features (e.g., dots) through development or development and etching
- Degree of resist lifting in pattern plating
- Yield (print & etch; AOI data)

Instant Adhesion

The instant adhesion test is a pull (peel off) test performed at different time intervals after resist lamination (0, 15, 30, 60 minutes, and 24 hours).

An adhesive tape is pressed against the laminated resist, the tape is pulled off, and the area-percent of the resist remaining on the copper surface is reported. There is no pre-scoring or cross-hatching of the resist before applying the adhesive test, as it is practiced in other standard adhesion tests (e.g., in the paint industry). Adhesion immediately after lamination tends to be lower than adhesion measured later, whereby in most cases the measured adhesion levels off after about 15 minutes of hold time after lamination.

Resolution after Development

Resolution after development can be judged by the smallest lines and spaces resolved, and the smallest, isolated line “held.” A multiple pitch pattern with 20–200 micron lines and spaces, isolated and nested (paired) lines, in a print & etch version and the corresponding pattern plate version, can serve as a test vehicle.

Survival of Small Resist Features Through Development or Development and Etching

A related test, introduced by Asahi, measures resist adhesion under actual wet processing conditions, through development or through development and etching. The resist is laminated, exposed, and developed to form a dot pattern of different diameter dot sizes. The test board is

then processed (e.g., through development and etching) and the resist adhesion is judged by the number of smallest dots that survive.

Degree of Resist Lifting in Pattern Plating

Degree of resist lifting can be measured by inspecting pattern plated boards after copper plating, but before resist stripping, with a high power microscope. The color of the lifted resist is a lighter blue than the darker blue observed in the region where the resist is in close contact with the copper surface. The width of the observed color change under the lifted resist can be recorded in microns. One observes that the degree of lifting on a given board varies with the dimension of the resist feature, not the size of the adjacent copper area. Therefore one measures lifting on the edge of a well defined large rectangular resist area. Three measurements from each of six test boards can be averaged.

Yield

Print & etch yields as determined by AOI can be used to correlate open defect frequency with poor resist adhesion. Defects called out by the AOI are visually inspected, verified, recorded as opens, shorts, space and line width violations, and downloaded to a PC. Yield analysis software then allows one to eliminate certain types of defects from the calculation that are not of direct interest to the study. For example, "repeat defects" which have to be associated with the imaging step (e.g., phototool flaw, trapped dirt, etc.) are irrelevant to a resist adhesion study and dilute defects pertinent to surface characteristics. Likewise, "short" defects in a print & etch study don't speak to poor film adhesion and conformation issues; however, "opens" do.

The study in Reference 1 describes yield determination in detail, as follows: The test vehicle was a single pitch, 75 micron (3 mil) line and space pattern with one-up repeat patterns of nested pair conductors, alternating in direction. The one-ups consist of a 2 x 2 inch (5 x 5 cm) pattern, repeated in an 8 x 10 array which covers a 16 x 20-inch (approx. 40 x 50 cm) total area with 36,000 inches (0.6 miles or 1km) of circuitry. Two test patterns were used, which were mirror images of each other: one for the panel front side and one for the back side. Five

boards were processed for each test condition.

When a test pattern is used, there arises some difficulty in defining yield. With real boards (at least a one-up real board), it is simple. A real board either has no defects, and is good, or contains one or more defects, and is therefore bad. The yield fraction is the number of good boards divided by the total number of boards made.

Because a test pattern is not a real board, defining yield becomes more complex. First, the test pattern may contain conductor length equivalent to that of 5–10 real boards. Our test pattern does not contain all of the features present on a real board, and it contains conductors and spacing finer than most real boards today. The best one can do is to measure the total defect count, divide by the total conductor lineage to find defects per unit length, then calculate the average number of defects per panel for a hypothetical real panel by multiplying defects per unit length (from the test vehicle) times the conductor length of the real panel. Finally, one can then estimate a yield from average defects per hypothetical panel. In our case, raw yield data are reported in DEMIs (defects per million inches of circuitry; 1 million inches equal about 16 miles or 25 km). The test pattern has 36,000 inches (0.6 miles or 1 km) of circuitry on each side. The space length is half the length of the lines. For reference, a typical high density 75 micron line & space production panel might have 5,000 inches (125 m) of circuitry. **PCB**

References

1. The Effects of Copper Foil Type and Surface Preparation on Fine Line Image Transfer in Primary Imaging of Printed Wiring Boards, B. L. Adams-Melvin, D. R. McGregor, and K. H. Dietz, Proceedings, P.C, World Convention VII, Basel, Switzerland, May 21–24, 1996.



Karl Dietz is president of Karl Dietz Consulting LLC. He offers consulting services and tutorials in the field of circuit board & substrate fabrication technology. To view past columns or to reach Dietz, [click here](#). Dietz may also be reached by phone at (001) 919-870-6230.

Mil/Aero007 News Highlights



Microtek Earns DLA Laboratory Suitability Status

The company's Linthicum Heights, Maryland facility has received Laboratory Suitability Status approval from the DoD DLA for MIL-I-46058, MIL-PRF-55110, MIL-PRF-31032, and MIL-PRF-50884. With this approval, the lab can now perform all applicable Group A, Group B, Group C conformance and reliability testing as well as full qualification testing for these specifications.

Invotec Gets Support for "Sharing in Growth" Program

The company is delighted to announce it has been approved by the government-backed Sharing in Growth (SiG) program. SiG is designed to enhance the competitive capabilities of selected companies within the UK aerospace supply chain, helping them to tackle barriers to growth, boost exports, and create more than 5,000 jobs within the UK's high-value manufacturing sector.

Amitron Named Truck-Lite's "2014 Supplier of the Year"

Truck-Lite Co. LLC has recognized Amitron Corporation by awarding their "2014 Supplier of the Year" to the Illinois PCB manufacturer. In a letter to Amitron, Truck-Lite's Vice President of Worldwide Purchasing Martin Schroeder stated that the award was for Amitron's "exceptional performance in the last 12 months in the areas of quality, delivery, technology and commercial competitiveness."

All Flex Achieves Re-cert to AS9100C, ISO 9001:2008

All Flex, a manufacturer of flexible printed circuits and heaters, announces re-certification to AS9100C and ISO 9001:2008.

Capital Electro-Circuits Reaffirms Commitment to Quality

Capital Electro-Circuits Inc in Gaithersburg, Maryland, is pleased to announce the successful completion of its ISO 9001:2008 re-certification. President Bharat Sitapara said, "This is a continuation of our ongoing commitment to maintain our ex-

cellent quality and to improve our quality wherever it is needed."

i3 Nets Contract to Supply Substrates for Military Use

i3 Electronics Inc. has announced that an industry leading aerospace and defense firm has awarded the company an order for the supply of advanced substrates for a military application. The order will run through the remainder of 2014.

Cicor Sees Positive 1H Amid Challenges in AMS Division

The Advanced Microelectronics & Substrates (AMS) Division experienced a difficult start into 2014, which resulted in a decline in sales due to the still challenging market environment in the Eurozone's aerospace, defense, and nuclear energy sectors, as well as the loss of sales in relation to the manufacture of an end-of-life product.

Military Radar Market to See CAGR of 2.9% 2013-2019

Driven by continuous growing threats from both the internal and external sources, global market for military radar was valued at US \$6,900 million in 2012 and is expected to reach US \$8,440 million by 2019, growing at a CAGR of 2.9% during the forecast period from 2013-2019.

Aerospace Industry's Sensor Market at \$2.44B in 2020

New analysis from Frost & Sullivan, "Analysis of Sensor Market in the Global Aerospace Industry," finds that the market earned revenues of \$1.24 billion in 2013 and estimates this to reach \$2.44 billion in 2020.

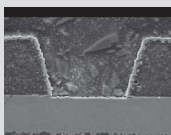
U.S. GDP to Grow 3% by 2016; Defense Spending Rises

UCLA Anderson Forecast's third quarterly report of 2014 indicates that the real Gross Domestic Product for the United States will grow at approximately 3% over the next two years, following a decline of 2.1% in the first quarter of this year and a rebound of 4.2% growth in the second.

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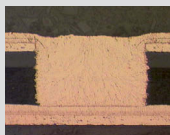


EDTA-free Electroless Copper

Formaldehyde-free Electroless Copper

Cyanide and Nickel-free Electroless Copper

Panel / Pattern Plating

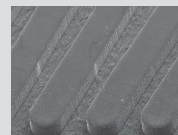


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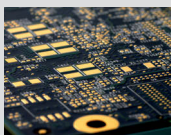


Bonding Enhancement with Reduction in Copper Waste and Chemistry Consumption

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Final Finishing



Cyanide-free Immersion Gold

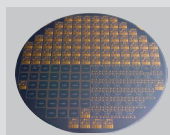
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ATOTECH

What is 4-Wire Kelvin?

by **Todd Kolmodin**

GARDIEN SERVICES USA

I've been asked many times, "What is 4-Wire Kelvin?" So, this month I will explain the 4-Wire Kelvin Test and how it can help uncover defects that normally would go undetected in standard electrical test methodology.

Most of us have used an ohmmeter to measure voltage, resistance and current. The typical meter has two wires; you probe the two terminals, trace ends or put the leads in line with the circuit for measuring current. A standard ohmmeter is shown in Figure 1 below.

However, with this type of measurement, the resistance of the leads and contact are added to the measurement. In Figure 2 you can see that the two leads with 0.5 ohms of resistance are added to resistance of the resistor being measure and providing a final result of 2.0 ohms, where the expected reading would be 1.0 ohms.

4-Wire Kelvin

4-Wire Kelvin testing is a methodology where high resolution measurements are taken to determine finite changes in resistance. These finite changes in resistance can then be used to locate plating defects or variations in plating thickness. The Kelvin test is highly accurate

because of a four terminal system that negates all current sources, lead and contact resistances. This allows for the finite measurements to only be measured on the PCB circuitry. Typically these measurements are in the milliohm range. Figure 3 shows the typical Kelvin circuit.

Now the question, "What can Kelvin detect?" In the PCB industry, the main focus of the Kelvin test is to identify plating defects in the drilled holes. The higher the aspect ratio of the drilled hole the higher risk of defect. The

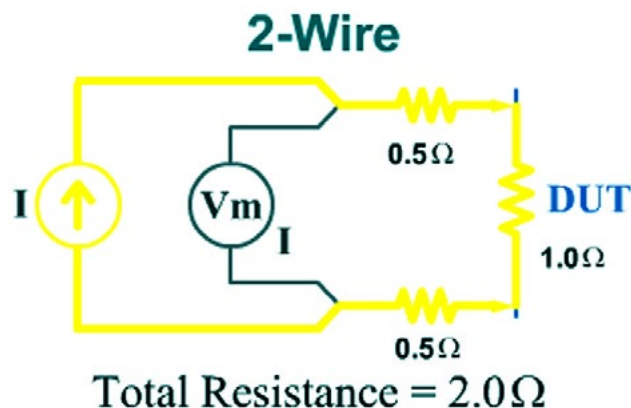


Figure 2: Two leads with 0.5 ohms resistance.

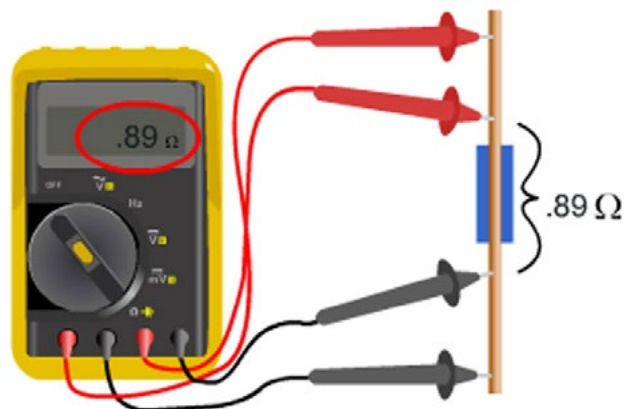


Figure 1: A standard ohmmeter.

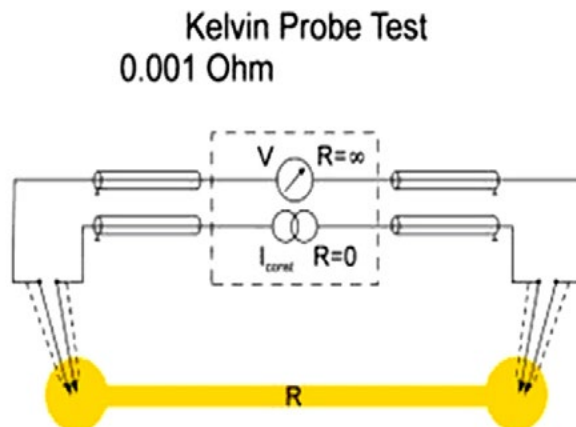


Figure 3: A typical Kelvin circuit.



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New Studies this Summer

2013–2014 Analysis & Forecast for the PCB Industry in North America

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World PCB Production Report for the Year 2013

\$475 (IPC member)
\$950 (nonmember)

On-Shoring in the North American Electronics Industry: 2014 Update on Trends and the Impact on Companies

\$225 (IPC member)
\$450 (nonmember)

Where in the World? A Regional Strategy Roadmap for Electronics Manufacturers

\$675 (IPC member)
\$900 (nonmember)

IPC's Best-Selling Study

Study of Quality Benchmarks for the EMS Industry — 2014

This annual study, published in July 2014, reports current PCB assembly quality data from companies worldwide, including:

- First-pass and final-inspection yields by various types of tests and inspection methods
- Internal yields of key processes
- Defect rates (DPMO)
- Cost of poor quality
- Customer returns
- Customer satisfaction
- Supplier performance
- Certifications

The findings are segmented by company size tier, region and type of production, enabling assembly companies to compare their performance to similar types of companies. Averages are reported for all metrics, as well as median values and 25th and 75th percentile data.

This practical reference guide is IPC's best-selling study. It is available in IPC's online store at www.ipc.org/EMS-benchmark-2014. Single-user prices are \$675 (IPC member) and \$1,350 (nonmember). Site and global licenses are also available.

More Information www.ipc.org/market-research-reports

defects shown in Figure 4 are typically what you will detect using 4-Wire Kelvin. Using standard electrical test with continuity thresholds at 10 ohms (IPC Class 3), these defects will go undetected as the change in resistance introduced by these defects will not cause enough change to fault at the 10 Ohm range. However, using the Kelvin test these changes in resistance will be detected as the changes although may be only 100–300 milliohms the high resolution measurement will fail.

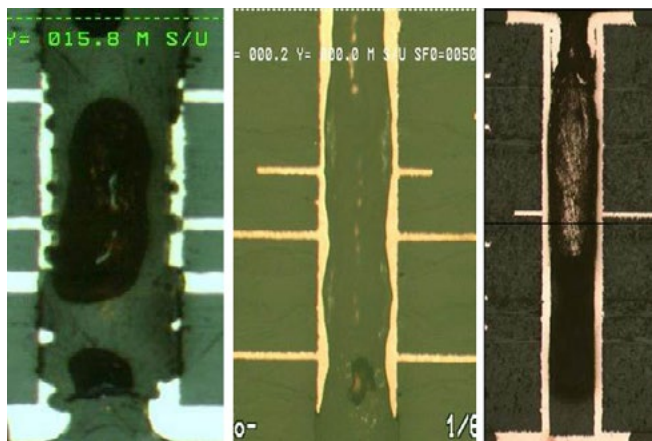


Figure 4: Typical defects detected using 4-Wire Kelvin.

4-Wire Kelvin can also detect voids in circular nets, typically power and ground (Figure 5).

A Few Good Questions

What is the best way to program for Kelvin Test...

...when looking for barrel integrity?

It is best to probe the barrel directly from one side to the other side. The barrel would have to be free of unwanted material such as solder mask. The connection to the annular ring/hole is imperative, the slightest variation with throw off the measurement system. When generating your programs it is best to ensure both sides of the barrel are tested in an overlapping fashion.

...when looking for specific net resistance?

It is important to test all pads open in the mask. This will allow for more accurate readings on each individual section of the network under test. Do not use end of node to end of node testing. The networks may be too long, causing unwanted variations in the readings.

Keep in mind that depending on the equipment used the size of the pad plays a significant

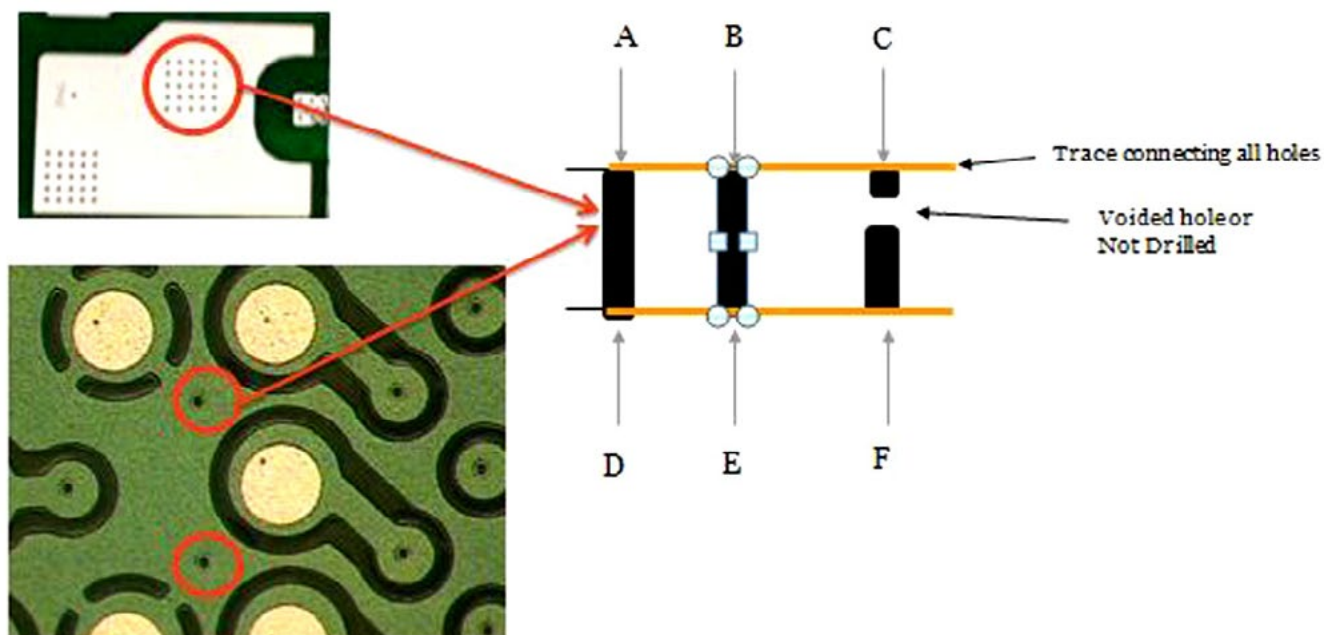


Figure 5: Voids in circular nets.

role due to the contact area of the two probes onto the pad. If only one probe hits the pad the test will be jeopardized.

Other areas of consideration when using 4-Wire Kelvin:

- Kelvin test should be done prior to solder-mask as an in-process QA step. It should not be performed as an FA process as the final board will not provide optimal or accurate results due mask on via holes
- Due to excess copper travel, the use of Kelvin for buried microvias is at the vendors discretion. The copper may add too much resistance to the master values and therefore allow possible defects to go undetected
- Kelvin testing for possible microvia copper issues should be done at the sub-part level
- For optimum test results, the barrels must

be probed directly from side to side. It is best to test each hole twice using an overlapping pattern

I hope this helps explain 4-Wire Kelvin and its uses in today's manufacturing marketplace. OEMs are requiring more and more from their suppliers and 4-Wire Kelvin test is just one of the expanded requirements. **PCB**



Todd Kolmodin is the vice president of quality for Gardien Services USA, and an expert in electrical test and reliability issues. To read past columns, or to contact Todd Kolmodin, [click here](#).

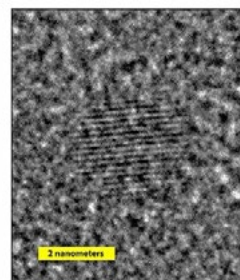
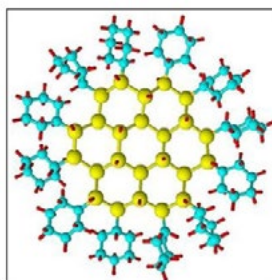
Nanotech Gets Big Push from Graphene

New research published in the journal *Advanced Functional Materials* suggests that graphene-treated nanowires could soon replace current touch-screen technology, significantly reducing production costs and allowing for more affordable, flexible displays.

The majority of today's touch-screen devices, such as tablets and smartphones, are made using indium tin oxide (ITO), which is both expensive and inflexible. Researchers from the University of Surrey and AMBER, the materials science centre based at Trinity College Dublin have now demonstrated how graphene-treated nanowires can be used to produce flexible touch screens at a fraction of the current cost.

Using a simple, scalable, and inexpensive method the researchers produced hybrid electrodes, the building blocks of touch-screen technology, from silver nanowires and graphene.

Dr. Alan Dalton said, "The growing market in devices such as wearable technology and bendable smart displays



poses a challenge to manufacturers. They want to offer consumers flexible, touch-screen technology but at an affordable and realistic price. At the moment, this market is severely limited in the materials to hand, which are both very expensive to make and designed for rigid, flat devices."

Lead author Dr. Izabela Jurewicz commented, "Our work has cut the amount of expensive nanowires required to build such touch screens by more than fifty times, as well as simplifying the production process using graphene, a material that can conduct electricity and interpret touch commands whilst still being transparent."

Co-author Professor Jonathan Coleman added, "This is a real alternative to ITO displays and could replace existing touch-screen technologies in electronic devices. Even though this material is cheaper and easier to produce, it does not compromise on performance. We are working with industrial partners on future devices and it is clear that the benefits will soon be felt by manufacturers and consumers alike."

The research benefitted from funding and collaboration with M-SOLV, a touch-screen manufacturer.

TOP TEN

PCB007
News

PCB007 News Highlights This Month

① **IPC: Slump in PCB Sales and Orders is Typical for July**

"July is typically a slow month for the PCB industry and this year is no exception," said Sharon Starr, IPC's director of market research. "The PCB book-to-bill ratio has been hovering around 1.00 since February, which explains the flat year-to-date sales growth we are seeing," she added.

② **Molex Dongguan China Earns FDA Registration**

Molex Incorporated announced that the Molex Dongguan, China facility is now registered with the U.S. FDA as a compliant manufacturer of Class I medical devices. Part of an ongoing process improvement plan by the Molex printed circuit products group, registration confirms the Dongguan China site's adherence with FDA inspections, tracking, and traceability criteria.

③ **Global PCB Market to Increase to \$74.3B in 2018**

IndustryARC forecasts the global PCB manufacturing market to increase its market size from around \$62.3 billion in 2013 to around \$74.31 billion in 2018, growing at a CAGR of 3.6%.

④ **Murrietta, eSurface Ink Technology Licensing Agreement**

The executed technology license agreement between the two companies provides Murrietta the right to manufacture PCBs using eSurface's patented technology, receive implementation and marketing support from eSurface, and to be acknowledged as an eSurface authorized facility.

5 i3 to Provide Variety of Services with New Contract

i3 Electronics Inc. has signed a multi-year agreement with an industry leading high-performance Computing firm for the supply of high-performance electronic assemblies. i3 will manufacture the PCBs and provide assembly, integration, and test services.

6 Precision Circuits West Unveils Line of Aluminum PCBs

These aluminum PCBs (also called metal core PCBs) are five to ten times as thermally conductive as conventional epoxy-glass, at one-tenth of the thickness resulting in thermal transfer far more efficient than a conventional rigid PCB.

7 Intercept Strengthens Canadian Representation with Kaltron

"Kaltron is delighted to offer Intercept's PCB, Hybrid IC, and RF software solutions to our customers in Canada. They complement very well our existing portfolio of design services, components, and modules," said Tom Martin, president of Kaltron.

8 Multitest Leads the Way in 0.3 mm-pitch PCBs

Multitest can manufacture PCBs with 40+ layers at 0.35 mm in a single lamination process without the use of laser drilled, "stacked," blind vias.

9 Ibiden Receives Multilayer PCB Manufacturing Tech Patent

The patent is mainly for a method of manufacturing a multi-layer printed wiring board including forming a core substrate, forming a first interlayer insulation layer over the core substrate, and forming a first filled via in the first interlayer insulation layer.

10 AT&S Among Top Performers in Resource Efficiency

The Lean & Green jury highlighted particularly the data transparency and the culture of open communication within the company. AT&S is committed to a green strategy and sustainability is a major goal for all employees.

For the latest PCB news and information, visit: PCB007.com



EVENTS

For the IPC Calendar of Events, [click here](#).

For the SMTA Calendar of Events, [click here](#).

For the INEMI Calendar of Events, [click here](#).

For the complete PCB007 Calendar of Events, [click here](#).

NEPCON Vietnam 2014

October 9–11, 2014
Ho Chi Minh, Vietnam

Austin CTEA Expo & Tech Forum

October 14, 2014
Austin, Texas, USA

Long Island SMTA Expo and Technical Forum

October 15, 2014
Islandia, New York, USA

Connecticut Expo & Tech Forum

October 21, 2014
Waterbury, Connecticut, USA

Intermountain (Utah) Expo & Tech Forum

October 23, 2014
Salt Lake City, Utah, USA

Industrial Automation Conference 2014

October 23–24, 2014
London, UK

LA/Orange County Expo & Tech Forum

November 6, 2014
Long Beach, California, USA

International Wafer-Level Packaging Conference

November 11–13, 2014
San Jose, California, USA

TSensors Summit 2014 – San Diego

November 12–13, 2014
La Jolla, California, USA

Wearable Sensors and Electronics 2014

November 12–13, 2014
Santa Clara, California, USA

ELECTRONICA 2014

November 11–14, 2014
Messe Munchen, Germany

Graphene LIVE! 2014

November 19–20, 2014
Santa Clara, California, USA



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PCB007 Presents

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Coming Soon to The PCB Magazine:

November:
Medical Applications
for PCBs

December:
Outlook for 2015