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February 2015

an I-Connect007 publication

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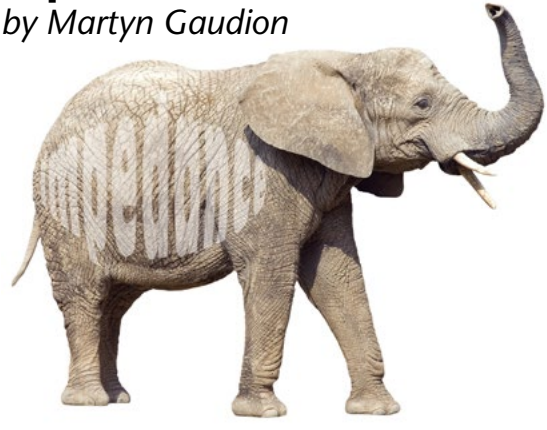
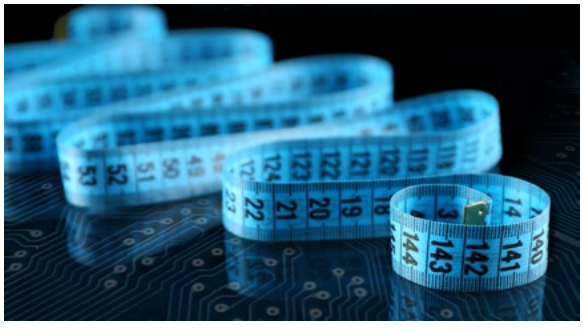
February 2015

This Issue: HIGH-SPEED DESIGN

FEATURED CONTENT

A decade ago, most PCB designers didn't have to worry about the challenges associated with higher speeds. But now, many electronic products feature high-speed PCBs, and designs are getting faster all the time. This month, we focus on high-speed design techniques, with articles from our contributors Kirk Fabbri, Barry Olney, Istvan Novak, Martyn Gaudion, John Coonrod, and Bob Tarzwell and Dan Beaulieu.





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Df @ 10 GHz	0.0028 - 0.0036	0.0028, 0.0031 & 0.0034	0.0031*	0.0030*	0.0017
CTE Z-axis (50 to 260°C)	2.90%	2.80%	2.80%	2.90%	2.90%
T-260 & T-288	>60	>60	>60	>60	>60
Halogen free	No	No	No	Yes	No
VLP-2 (2 micron Rz copper)	Available	Available	Available	Standard	Standard
Stable Dk & Df over the temperature range	-55°C to +125°C	-55°C to +125°C	-55°C to +125°C	-55°C to +125°C	-40°C to +140°C
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IPC Updates CID, and DFX Takes Off

by Andy Shaughnessy
I-CONNECT007

It's almost time for IPC APEX EXPO 2015, and I, for one, am happy to be returning to the San Diego Convention Center. Is there a nicer city in America than San Diego? Yes, it's a tad expensive, but it's worth it; there are worse places to spend a week. Nothing against Las Vegas, but San Diego beats Sin City in every category, with the exception of hotel rooms per square mile.

The Design Forum kicks off the show on the morning of Feb. 23, with a variety of new classes and speakers. This marks the first Design Forum since the death of Dieter Bergman. It'll be bittersweet, but I'm sure everyone will be sharing stories about Dieter. (Everyone is invited to join the tribute to Dieter on Wednesday, Feb. 25, at 6:30 pm in Ballroom 6F in the convention center. Share your memories of Dieter, or some of his best off-color jokes, or your favorite "Dieterisms." The $25 admission goes to a scholarship fund in Dieter's name.)

After a networking breakfast, PCB design engineer Carl Schattke of Tesla Motors will give the keynote speech. Have you ever met anyone who designed boards for electric cars? That should draw a pretty good crowd. Then IPC Master Trainer Rainer Taube of Taube Electronic GmbH will discuss IPC-7070 component mounting issues. Tom Hausherr of PCB Libraries will wrap up the morning, focusing on IPC-7351C, requirements for surface mount design and land pattern standard.

After lunch, the Professional Development design classes begin. Stephen V. Chavez, a PCB designer with UTC Aerospace Systems who has spent a lot of time working abroad, will offer tips for communicating and working with multicultural design teams. From what I've heard,

this will be a really interesting talk. The day wraps up with the newly retired (but will he ever really retire?) Rick Hartley discussing ways to achieve success by controlling cost and quality. And isn't cost and quality what it's all about?

IPC Design Programs Update

You may have heard that the IPC Certified Interconnect Designer program (CID and the CID+ advanced course) has been updated. Course content has been fine-tuned periodically since the program was introduced 20 years ago, but the 2015 edition is a completely refreshed program. CID and CID+ tutorials and exam take place Feb. 20-22 at the convention center.

I spoke with Anne Marie Mulvihill, director of education programs at IPC, and asked her about the technical offerings for PCB designers.

"If I look tired at the show, it's because I've proofed the new edition about 87 times," she laughed. "This material isn't easier; it's just easier to digest, and organized to synch up CID to CID+ for better flow of information. Designers who are already certified won't require recertification to this 2015 edition, but they should consider reviewing the new study guides, just to stay current with best practices."

She pointed out how designers can use the CID study guide to show their bosses and teammates what they've been studying, and what their job entails.

"Nobody puts baby in the corner, but designers still wind up there. Designers are not getting the respect they deserve, and new hires need formal training," Anne Marie said. "So, let your boss see this study guide. Make a 10-minute appointment to show your boss just a sample of what you're doing, or schedule time at your next department meeting for a brief presentation to your whole team. Communication can really pay off."

"Nobody puts baby in the corner, but designers still wind up there. Designers are not getting the respect they deserve, and new hires need formal training," Anne Marie said. "So, let your boss see this study guide.

For certified designers who want to take their professional development to the next level, she recommends DFX - Design For Excellence: DFM, DFA, DFT, and more. This full-day DFX course takes place Sunday, Feb. 22 at IPC APEX EXPO in San Diego.

"The DFX course debuted in late 2013, and it's been a door-buster ever since. It provides all teams a better understanding of all phases of the product lifecycle. Not just design, but manufacturing, all the way through to test phase," she added. "And if you can't get to San Diego, we're bringing the DFX course to a theater near you! We're holding DFX courses in Texas in May, Chicago in June, Minneapolis in October, and Raleigh in December."

The DFX class can be provided on-demand for interested companies or Designers Council chapters.

The second component of the IPC DFX program is an industry guideline in development now, and scheduled for publication this fall. Anne Marie expressed special thanks to the core members of the DFX Document Committee for their work developing this course: Don Dupriest of Lockheed Martin, Karen McConnell of Northrup Grumman, Dale Lee of Plexus, and Cheryl Tulkoff of DfR Solutions. Cheryl and Dale are the instructors for the DFX course.

For more information on IPC courses in 2015, click here. For a list of IPC-licensed training centers click here.

See you at APEX and the Design Forum.

PCBDESIGN

Andy Shaughnessy is managing editor of *The PCB Design Magazine.* He has been covering PCB design for 15 years. He can be reached by clicking here.

Effective Characteristic Impedance

by Kirk Fabbri
KSPT ENGINEERING CONSULTING

In a typical interconnect, there lie multiple places where capacitance plays a factor in the signal integrity. This includes the driver and receiver output/input capacitance, as well as the packages, vias, and the transmission lines. Failing to optimize these parameters can often lead to unwanted reflections, excessive radiated and or conducted emissions, and sometimes failure of components and systems.[1]

Reflections can occur anytime there is an impedance mismatch on the line. Sources of mismatches are plentiful and include trace width changes, vias, stubs, reference plane changes, and even the so-called fiber weave effect. In this case, a trace can encounter a different dielectric constant depending on whether it is routed over glass or the epoxy resin in the dielectric material.[3]

In this investigation, it is the capacitive contribution of the different components that are of interest, and how they affect the characteristic impedance the driver sees. For the following examples, the HyperLynx Termination Wizard is used for investigating these effects. It works on a variety of termination schemes including series, parallel, Thevinin, AC, and combinations of those topologies.

Figure 1 shows a simple point-to-point system in HyperLynx 9.0 LineSim. Included is a driver (flash signal I/O pin) and a simple LVCMOS input connected by a one-inch, 50-ohm transmission line.

Running the termination wizard on this net reveals the following results shown in Figure 2. The wizard shows that the driver impedance is 52.7 ohms (based on the IBIS model pull-up/pull-down curves and the 50-ohm load line), the driver transition time is 855ps, the characteristic impedance of the transmission line is 50 ohms, and the effective impedance is 46.5

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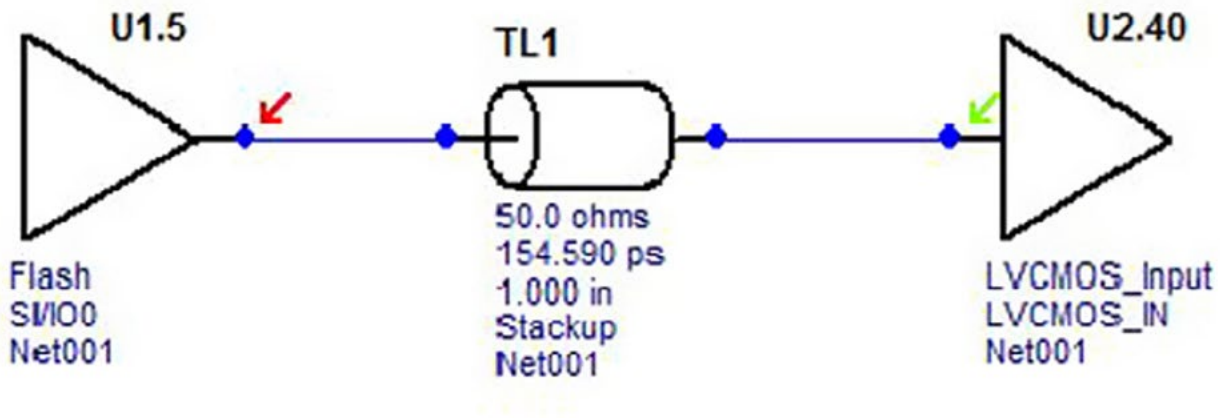

Figure 1: The schematic diagram for a simple circuit consisting of a driver (U1.5) and receiver (U2.40) connected by a one-inch, 50-ohm transmission line.

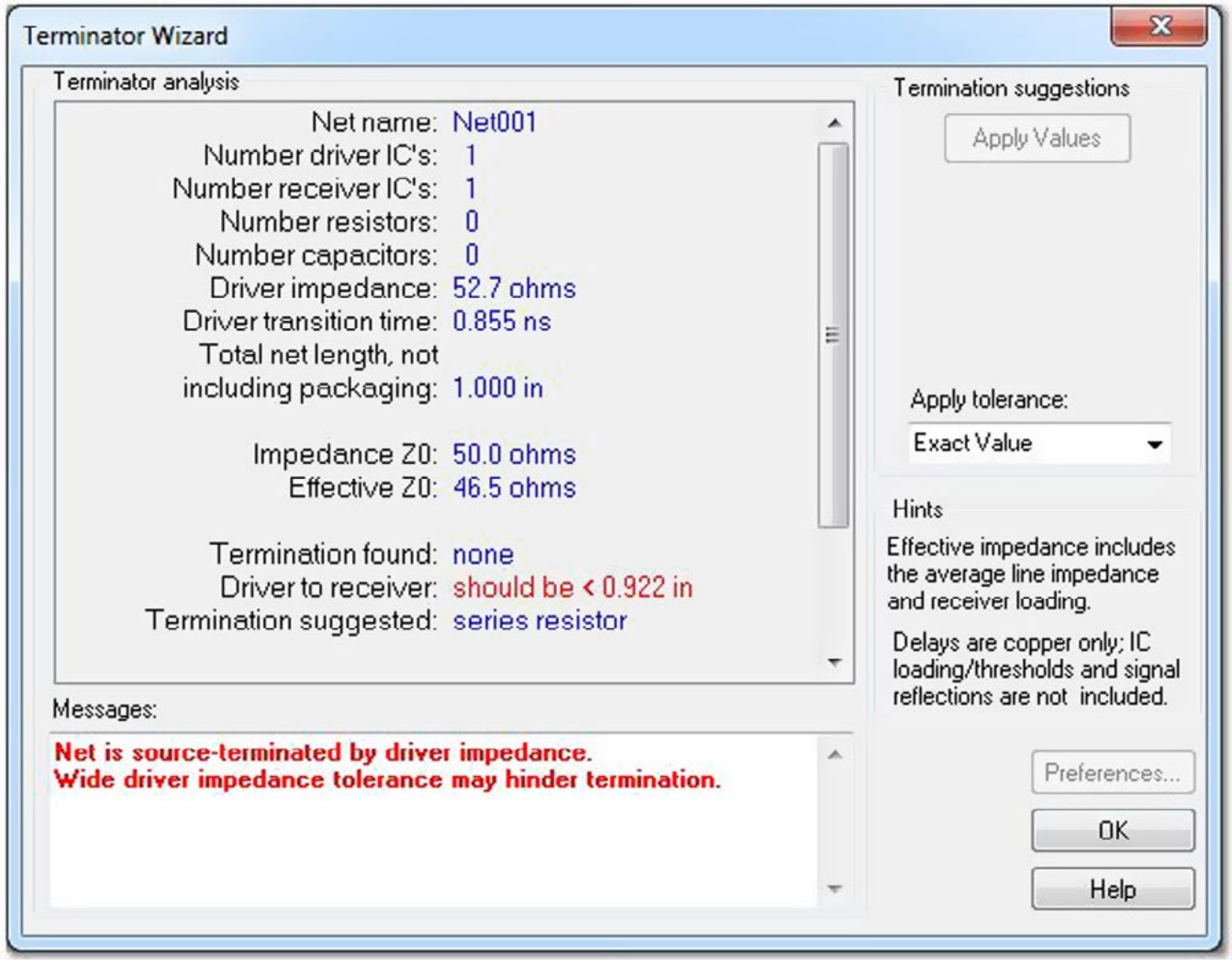

Figure 2: Termination wizard results for the simple schematic shown in Figure 1.

ohms. The effective impedance (effective Z0) is explained in the LineSim user guide as a value calculated by the field solver to indicate how much the capacitance of the load IC decreases the impedance the driver sees.[2] As shown later, the effective Z0 calculation is highly dependent on several key parameters.

To understand the effective Z0 parameter, the IBIS model of the receiver is investigated. For those who aren't familiar with the IBIS format; IBIS is used to show the buffer's behavior without compromising the manufactures proprietary information. An IBIS model describes the transistor pull-up/pull-down curves, the ESD diode clamp curves, the drivers' transition characteristics, pin parasitic information, and package model parameters among others. Figure 3 is an excerpt from the receiver's IBIS model showing the package parameters for the IC.[4] Figure 4 shows both the pin RLC parameters and the value C_comp under the appropriate buffer model.

Capacitive Effects on Effective Characteristic Impedance

Most interesting are the package/pin parasitic capacitance and the parameter C_comp in the receiver model. It is important to note the pin RLC parameters for this model were added for demonstration purposes and do not truly represent the buffer characteristics.

In this case, the addition of the package capacitance (0.605pF), the pin capacitance (2pF), and input capacitance (0.5pF) make up the total input load capacitance. According to the wizard, it is this capacitive load that effectively lowers the characteristic impedance that the driver sees down to 46.5 ohms. In this case the driver impedance (52.7 ohms) is already higher than the characteristic impedance, so no additional termination is recommended.

For demonstration purposes, the pin capacitance is changed to something significantly higher (10pF for this example). Running the wizard for this case indicates that the effective Z0 is now 39.4 ohms, as shown in Figure 5.

Now the pin capacitance is set to 0pF to analyze C_comp's contribution to the results. After running the wizard on this scenario, the results show the effective Z0 to be 43.9 ohms, indicating that C_comp also has an impact on the impedance the driver sees.

```
[Package]
| variable      typ           min           max
R_pkg           85.000m       45.0500m      0.1039
L_pkg           3.7700nH      3.4000nH      4.1550nH
C_pkg           0.6050pF      0.5440pF      0.6650pF
```

Figure 3: Receivers RLC package parameters for the IC. IBIS includes the minimum, typical, and maximum values for all parameters.

```
38          VDD_IO          POWER
39          PCLK_OP         PRU08slew_ESD
40          LVCMOS_IN       PRU08slew              0.1        1.5nH      2pF

C_comp      0.5000pF          0.5000pF              0.5000pF
|
```

Figure 4: Pin RLC parameters for pin 40 (RGBA0) and the values for C_comp. The pin RLC data was added to the model for demonstration purposes. C_comp is the input capacitance for the buffer when specified as an input and the output capacitance when specified as an output.

EFFECTIVE CHARACTERISTIC IMPEDANCE *continues*

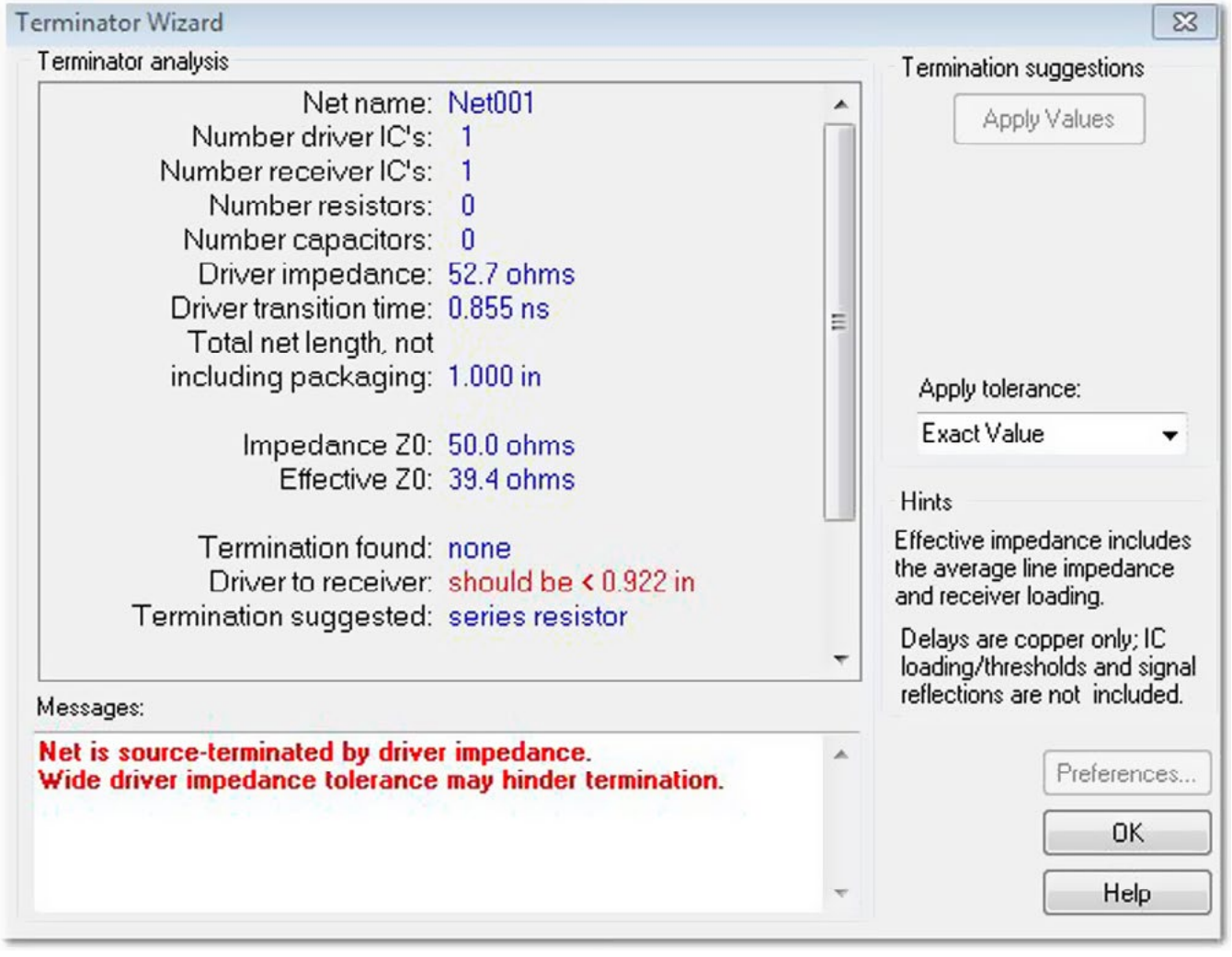

Figure 5: The wizard results after changing the capacitance parameter of the pin to 10pF. Notice how the effective Z0 is considerably lower than previously shown.

Transmission Line's Effect on Effective Characteristic Impedance

The length of the transmission line also had an effect on the results of the wizard. Recall from Figure 1-1 that the driver and receiver are connected by a 1 inch 50 ohm transmission line. Figure 6 below shows the transmission line parameters calculated by the field solver where the inductance (L) and capacitance (C) are the results of the entire one-inch of transmission line.

Depending on which source is referenced, publications differ on when the interconnect is considered to be a lumped or distributive system.[1] This distributive property is based on the drivers transition rate as compared to the delay of the interconnect. The field solver appears to using a 1/6th rule as based on the experiment outlined next.

For this experiment, the length of the transmission line is shortened to see where the wizard starts to ignore its effect on the effective Z0 parameter. The receiver IBIS model is set back to its original configuration with C_comp being equal to 0.5pF and the pin RLC parameters set to equal those shown in Figure 4. Recall from Figure 2 that the effective Z0 was equal to 46.5 ohms by this configuration.

Now the transmission line is shortened to 0.5 inches to see the effect on the wizard. Figure 7 shows the results after shortening the trans-

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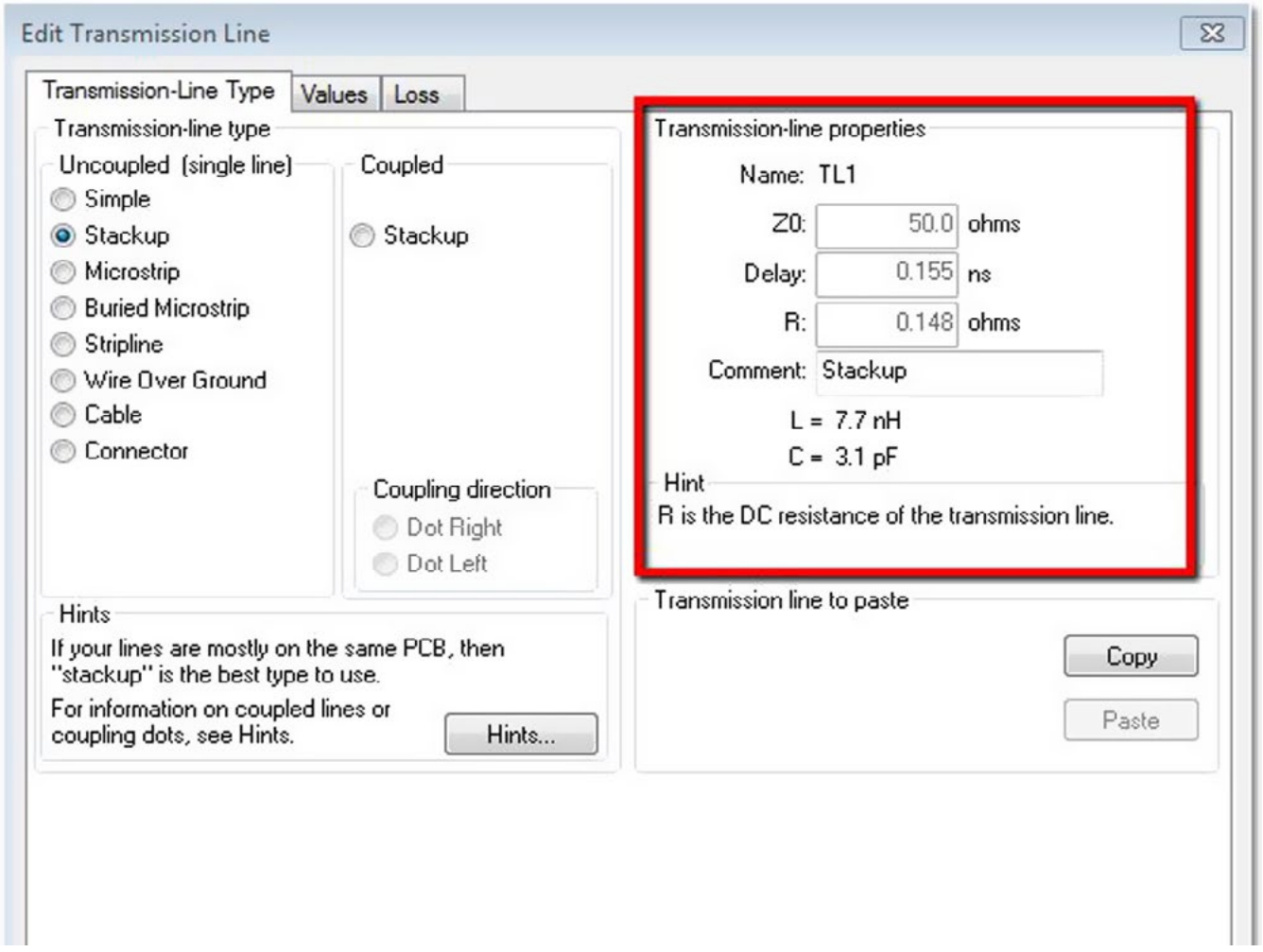

Figure 6: The important parameters for the 50 ohm transmission line.

mission line to 0.5 inches. Notice now that the effective Z0 is equal to the transmission line Z0 parameter of the system—50 ohms. From this it is reasonable to conclude that the simulator no longer considers this to be a distributive system since the length of the interconnect is shorter than some factor when compared to the driver transition time.

1/6th Rule

Now the interconnect length is changed to be 1/6th of the driver transition time, which according to the wizard is 855ps. This transition time would equate to an interconnect delay of approximately 142.5ps. Using the original transmission line delay factor of 155ps/inch, the line length is calculated to be approximately 0.919 inches. After running this simulation, the wizard indicates that the field solver still considers the system lumped, and therefore, not considering the interconnect length in the effective Z0 calculations. If the interconnect length is set just slightly longer than this 1/6th factor (e.g., 0.925 inches), the simulator switches over to a distributive system and the effective Z0 parameter decreases to 48.1 ohms from 50 ohms (lumped system calculation).

Also notice that 48.1 ohms is calculated for a transmission line length of 0.925 inches, which is slightly larger than for the one-inch line (46.5 ohms). Since the line length is slightly less, the total distributed capacitance is also less, thus the driver's loading is decreased, mak-

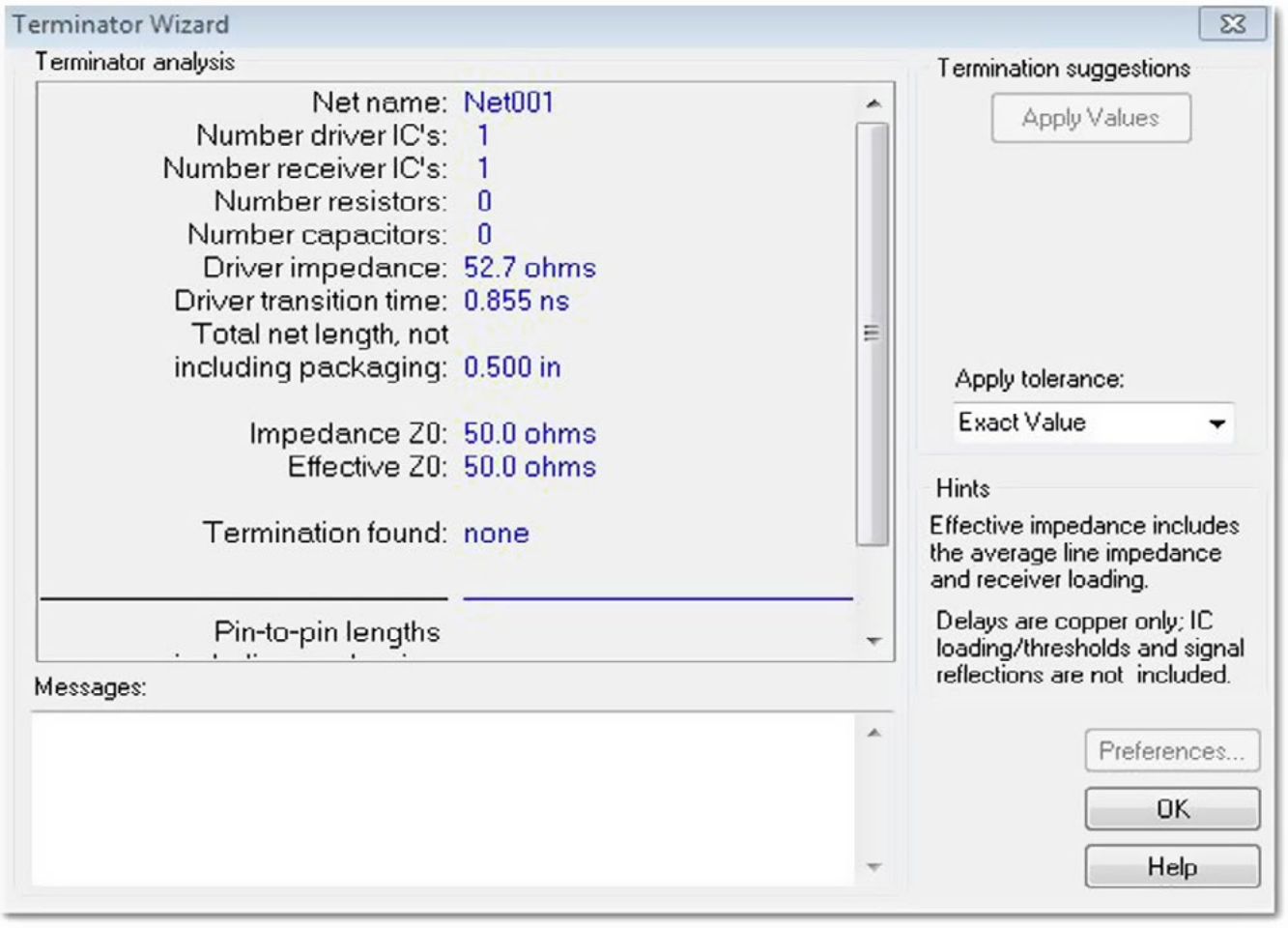

Figure 7: Results of the wizard after the transmission line length is shortened to 0.5 inches. Notice the effective Z0 is equal to the impedance Z0 parameter of the system—50 ohms.

ing the effective Z0 increase (recall the effective Z0 results from Figure 5).

Simple Series Terminated Circuit

Figure 8 expands the previous findings to a simple, often encountered series terminated net topology. The total transmission line length is still approximately one inch divided equally between the three segments. The driver and receiver models are identical to their original configuration, and a 22-ohm resistor is added to the circuit. To simulate a more typical situation, the net transitions layers from top to bottom, and back to the top, necessitating two vias (13 mil drill, 24 mil pad).

Recall from Figure 2 that the driver impedance is 52.7 ohms as indicated by the wizard. The ideal series termination would be the transmission line impedance minus the driver impedance (75-52.7 = 22.3 ohms).[1] For simplicity, a 22-ohm resistor is used since this is a standard value. After running the wizard on this topology, it indicates that the effective Z0 is 64.8 ohms and the recommended termination value is 12.1 ohms (64.8–52.7 ohms = 12.1 ohms). From this example, it is easy to see that the capacitance of the topology is affecting the effective impedance and lowering the recommended termination impedance as indicated by the recommended termination resistor (12.1 ohms).

Investigating the Via Contribution

Figure 9 shows the via construction and its transmission line equivalent model (56

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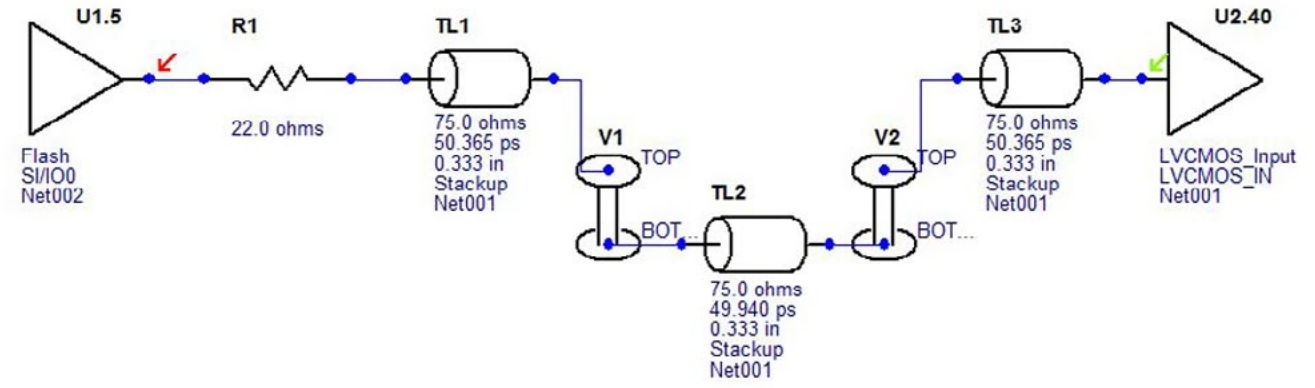

Figure 8: The schematic of the series terminated net topology.

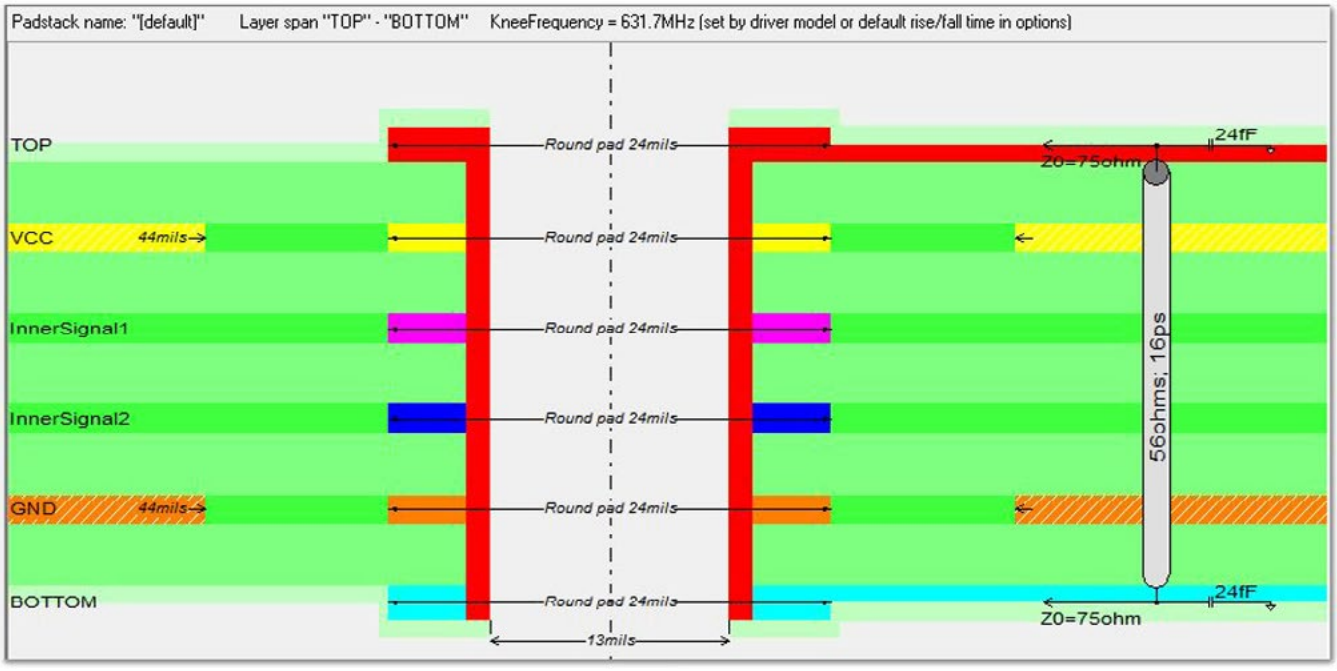

Figure 9: The via construction and its transmission line equivalent model.

ohms, 16ps delay). The transmission line model is calculated from the individual LC sections of the via transitioning through the layers and is shown in Figure 10. According to documentation, the pad to plane capacitance of the entry and exit layers are not included in the transmission line equivalent of the via, but are represented by a capacitor to ground.[2]

Referencing Figure 10, the individual inductance and capacitance values are added up to form a lumped model and verified to be approximately 56 ohms and 16ps by the following well known equations.[1]

$$Zo = \sqrt{(L/C)} = \sqrt{(875pH/282fF)} = 55.7 \sim 56\Omega$$

$$Delay = \sqrt{(L \times C = (875pH \times 282fF)} = 15.7 \sim 16ps$$

After running the wizard with the vias included, the results show the effective Z0 to be 64.8 ohms, and the optimal termination to be 12.1 ohms. What happens if the via characteristics are altered in a way that would better match

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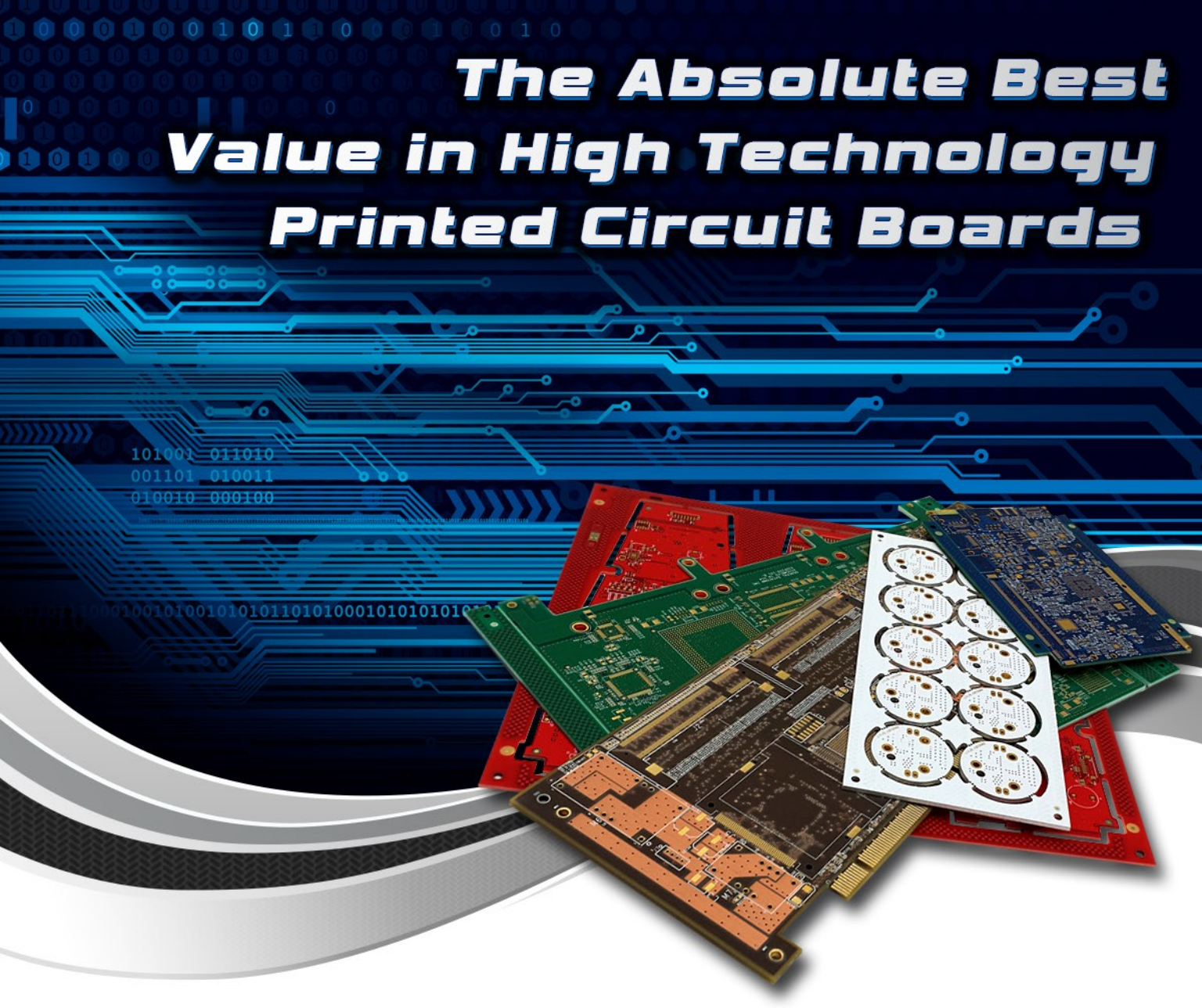

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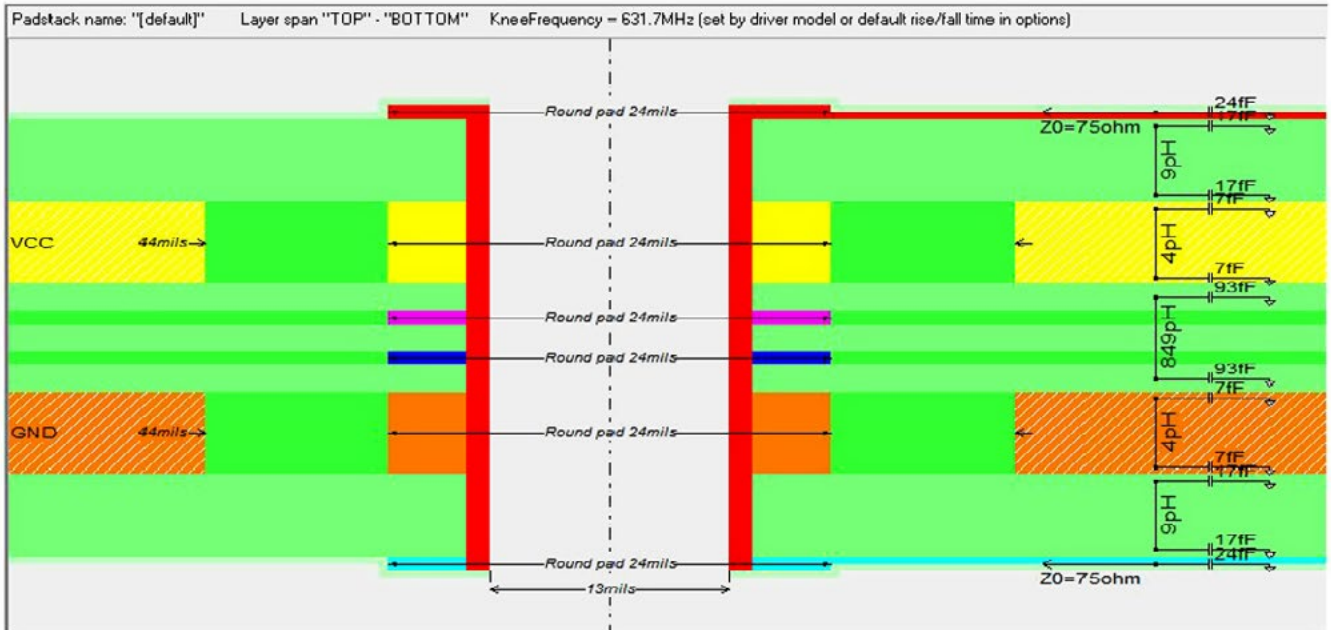

Figure 10: The transmission line model is calculated from the individual LC sections of the via transitioning through the layers.

the characteristic impedance of the connecting nets (75 ohms)? To see these effects, the via is altered to have a 75 ohm impedance and a 13ps delay (5.4 mil pad, 8 mil drill). Running the wizard again on this scenario shows the effective characteristic impedance is now 67.2 ohms, indicating that the vias are no longer loading the driver as much as before. The drill/pad size chosen for the via aren't entirely realistic. This is merely for purpose of demonstration.

Important Points to Remember

- The simulator calculates the driver impedance based on the transistor characteristics in the IBIS model and recommends termination based on the topology and characteristic impedance of the system.
- The receiver capacitance parameters including C_comp, pin capacitance, and package capacitance all impact the loading on the driver, thus changing the effective Z0 parameter.
- The wizard does not appear to consider the system distributive until the interconnection length becomes approximately equal to or longer than 1/6th of the driver's transition time.
- When not considered to be a distributive system, changes to the capacitive properties of the IC are no longer included in the wizard's calculation of the effective Z0 parameter.
- Vias have an effect on the loading of the driver, but their affects can be minimal depending on the driver transition rates. As the driver speeds increase, their effects become more pronounced. **PCBDESIGN**

References

1. Signal Integrity: Simplified, ISBN 0-13-066946-6.

2. Mentor Graphics LineSim User Guide, July 2013.

3. Right the First Time, A Practical Handbook on High-Speed PCB and System Design, Volume 2, ISBN 0-9741936-1-5.

4. IBIS (I/O Buffer Information Specification) Version 6.0, September 20, 2013.

Kirk Fabbri is owner of KSPT Engineering Consulting, LLC and electrical engineer for L-3 Communications – Avionics Systems. He can be reached at kirk.fabbri@L-3com.com.

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by Barry Olney
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At frequencies below 1GHz, the effect of copper surface roughness on dielectric loss is negligible. However, as frequency increases, the skin effect drives the current into the surface of the copper, dramatically increasing loss. When the copper surface is rough, the effective conductor length extends as current follows along the contours of the surface up and down with the topography of the copper surface. At high frequencies, the effective resistance of the copper increases relative to the additional distance over which the current must transverse the contours of the surface. The total loss comprises of the sum of the conductor loss and dielectric loss.

Whilst it may be possible to manufacture copper foil with a perfect mirror-smooth finish, the foil-to-resin adhesion would be compromised. This would considerably increase the possibility of delamination during the thermal stress of the PCB fabrication and assembly processes. For this reason, a reduced oxide coating is applied to the inner core layers to promote adhesion of the prepreg resin as it flows under the applied heat and pressure to cure.

Skin effect is the tendency of an alternating current to become distributed within a conductor such that the current density is largest near the surface, and decreases with greater depths in the conductor. The higher the frequency, the greater the tendency for current to take the path of lower inductance on the outer surface of the conductor. The skin depth is given by:

$$\delta = \sqrt{\frac{2}{2\pi f \, \mu \, \sigma}}$$

where is the skin depth in microns, f is the frequency in MHz, is the magnetic permeabil-

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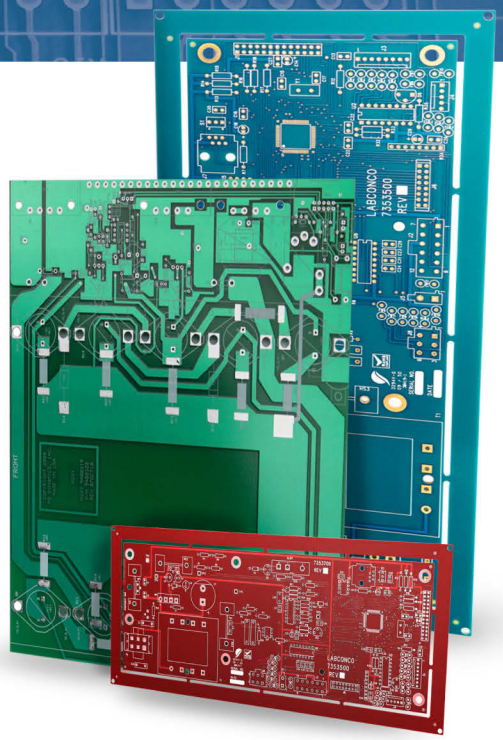

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ity ($4\pi x10^{-7}$H/m) and is the copper conductivity, typically ($5.6x10^{7}$ S/m).

The skin depth (um) can be approximated by:

$$\delta = 66\sqrt{\frac{1}{f}}$$

Looking at this equation, it is apparent that skin depth decreases with increased frequency. Figure 1 shows the skin depth compared to frequency. At low frequency (1MHz), the skin depth is 66um but this decreases to 0.66um at 10GHz. So, at 10GHz, only the very outer surfaces of the trace carry the current. Also, the red horizontal lines represent the trace copper weight and thickness. This shows that at about 10MHz, a signal traveling in a ½ oz. (17.78um) copper trace would not use the entire trace cross-section, but rather the skin effect would be dominant.

In a previous column, Beyond Design: Surface Finishes for High-Speed PCBs, I pointed out that the nickel content of ENIG surface finish has a ferromagnetic property that can adversely affect electromagnetic fields in the high frequency domain. One could argue that since the nickel is plated on top of the microstrip surface, that it would have little effect on properties of the trace. And that due to the skin effect, the current will travel the path of least inductance, which is on the lower surface of the copper closest to the reference plane. However, it has been found that at approximately 2.7GHz, the resonant behavior of the nickel component in ENIG, increases insertion loss. It is for this reason that solder mask over bare copper (SMOBC) processing should be considered for all high-speed designs.

Most substrates are copper clad with either Rolled Annealed (RA) copper, electrodeposited copper (ED) or reverse-treated foil (RTF). RA copper is both smooth and consistent in thick-

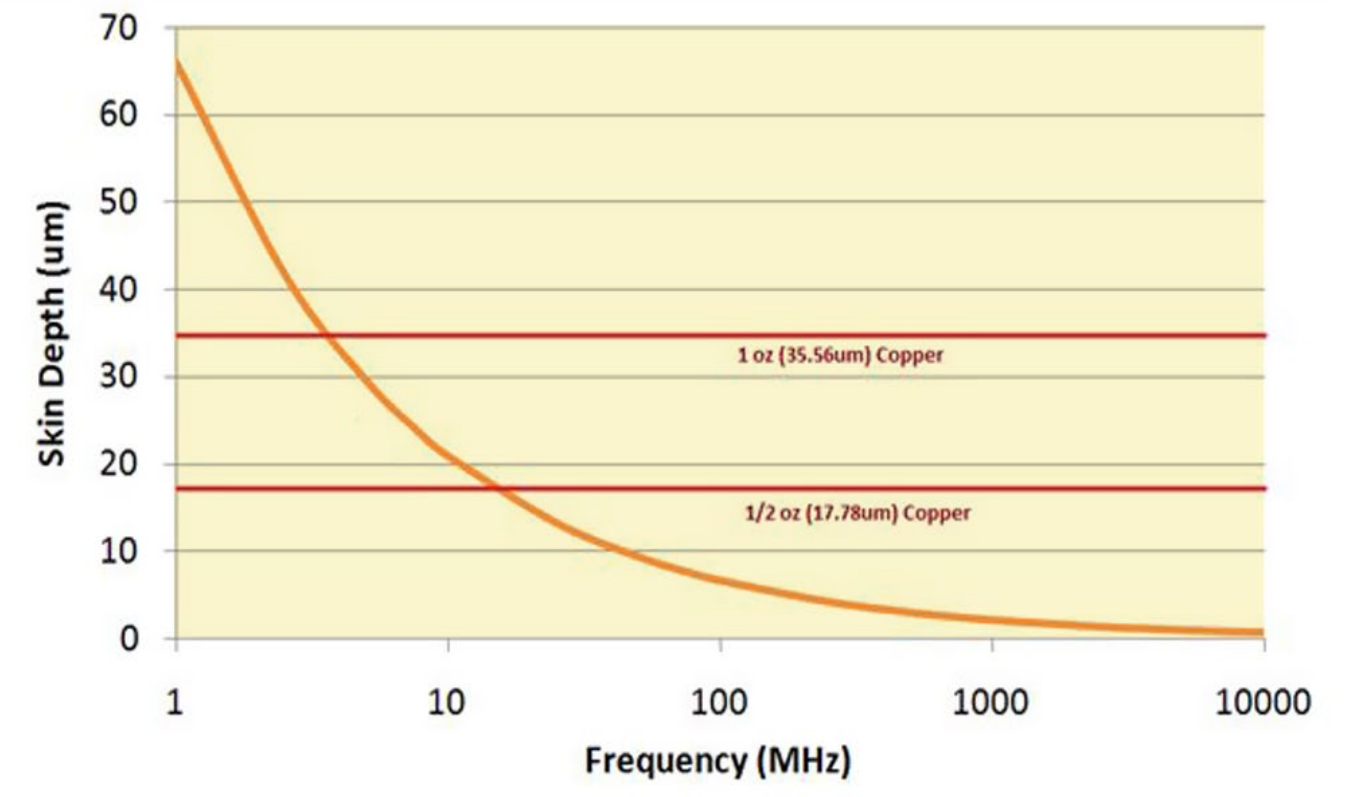


Figure 1: Skin depth (um) vs. frequency (MHz).

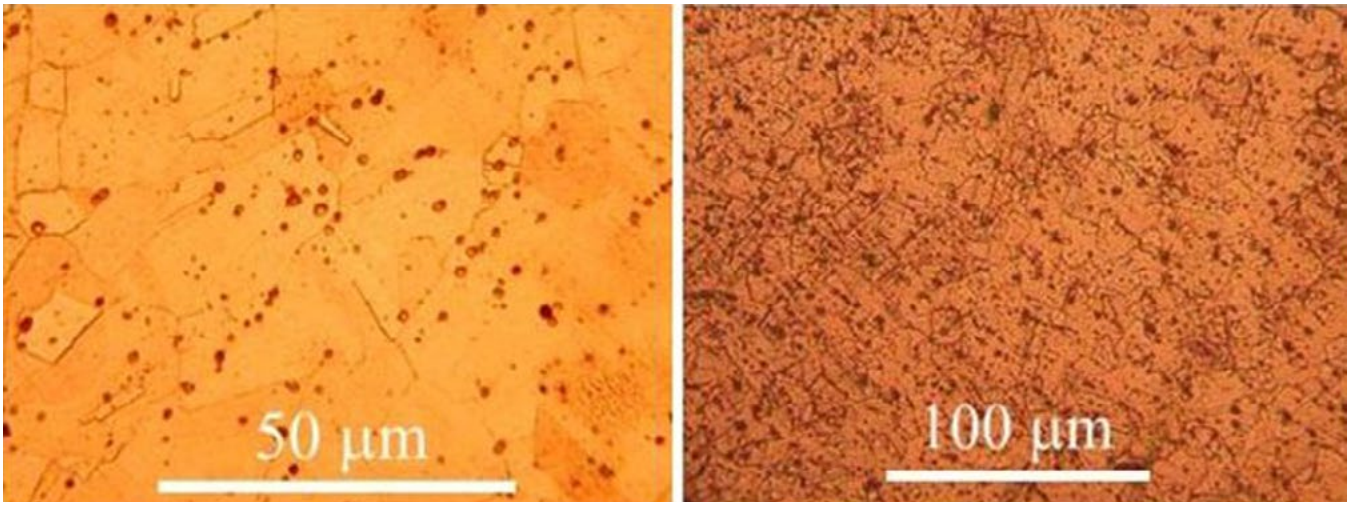


Figure 2: Rolled annealed copper (left) and etched copper (right) under an electron microscope (courtesy of University of Cambridge).

ness, but is the most expensive foil. ED copper has the roughest surface and depending on the application and speed requirements, may be perfectly adequate. RTF copper is smoother, and is much the same cost as ED. However, it does exhibit poor peel strength and is prone to delamination. So it is a trade-off between performance and price.

Electrodeposited copper foil is the standard copper used in the laminate industry. ED foil is deposited from a copper solution, at a specific DC voltage, onto a moving polished titanium drum which forms the cathode. The foil is subsequently stripped from the drum. The grain construction formed by this process forms the dendritic "tooth" of the copper on the "bath side" of the copper. The drum side takes on the smooth texture of the polished drum surface onto which it is plated. Figure 3, illustrates a typical inner layer trace cross-section showing the roughness of both the upper and lower copper surfaces.

Rolled copper is made by running a copper strip through successively smaller and smaller gaps in a rolling mill until it reaches the desired thickness. Rolled copper is smoother and can be made very flexible by annealing. Because it is smooth, its bond to laminates is totally dependent on the quality of the treatment it receives and the adhesive properties of the resin system employed. RA copper also has a different grain

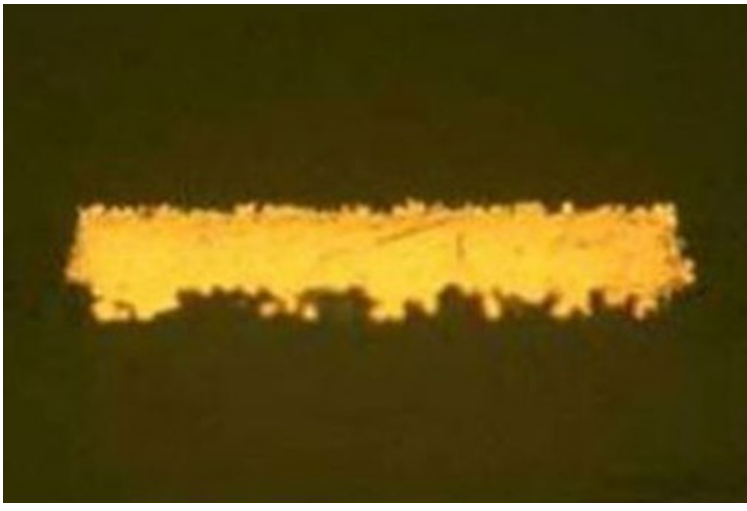


Figure 3: Inner layer trace cross-section [3].

structure than ED copper and will etch at a different rate. Much of the RA copper in the laminate industry is used in flexibly circuits, typically bonded to a polyimide film with an acrylic adhesive.

Reverse treated foils involve the subsequent treatment of the smooth side of the electrodeposited copper. Treatment layers are thin, rough coatings that improve adhesion of the base foil to the dielectric material.

To the naked eye, copper clad laminate appears smooth but at the microscopic level, all

EFFECTS OF SURFACE ROUGHNESS ON HIGH-SPEED PCBS *continues*

materials exhibit surface irregularities. If the average incline of the "teeth" of the conducting surface is 60°, forming an equilateral triangle, then the increase in surface resistance would be approximately twice that of a dead flat surface. Less severe geometries induce smaller effects. However, a better measure of the surface roughness is the root-mean-square (RMS) height (h_{RMS}) of the surface bumps, since the exact profile cannot be established for a working design. Taking the worst case equilateral ridge geometry as a guide, one would expect the RMS roughness to be in the order of 0.29 times the average peak to valley roughness.

The onset frequency (ω) of the RMS surface roughness effect is given by:

$$\omega = \frac{2}{\mu \sigma hRMS\text{^}2}$$

where is the magnetic permeability ($4\pi x10^{-7}$H/m) and is the copper conductivity ($5.98x10^{7}$ S/m) and h_{RMS} for ED copper.

Therefore, inserting the numbers into the above equation, the onset frequency (ω) of the RMS surface roughness effect is 1.28GHz for ED copper. The smoother the copper surface, the higher the frequency at which surface roughness takes effect.

Also, the effective dielectric constant and hence capacitance is increased due to the increased surface area of the teeth of the rough conductor. This, in turn, lowers the characteristic impedance slightly. The capacitance increases by about 5% for microstrip and 10% for stripline traces that exhibit more roughness. So the effect on impedance is -2% to -5%, respectively.

Although the surface roughness is not generally stated in material manufacturer's datasheets, typical values are 3 µm for the outer surface and 6 µm for the inner surface. For example, Panasonic's high-performance laminate, Megtron 6 core material, has a dielectric constant (Dk) of 3.4 and loss tangent (Df) of 0.004 at 18GHz. This material is available in standard ED, VLP, SVLP and HVLP (very/super/hyper low profile) foil with average surface roughness of 7–8, 3–4 and 1.5–2 µm respectively.

Isola uses mostly VLP type coppers for their HSD product offerings. The RTF coppers that Isola offers have roughness values of 4–8 microns. This is standard for FR408HR and IS415 products. VLP2 (Isola's designation) copper is incorporated in high-end products that require the best insertion loss. The roughness for this copper is 2 microns.

So, the smoothest surface HVLP material with 1.5 µm average surface roughness, will therefore not exhibit any noticeable surface roughness effect up to 20GHz. Consequently, one would be well advised to take note of the surface roughness properties if your design is running over 1GHz to ensure you choose an appropriate material for the application.

Points to Remember

- At speeds below 1GHz, the effect of copper surface roughness on dielectric loss in negligible.
- As frequency increases, the skin effect region drives the current into the surface of the copper dramatically increasing loss.
- When the copper surface is rough, the effective conductor length extends as current follows along the contours of the surface up and down with the topography of the copper surface.
- Smooth surfaces considerably increase the possibility of delamination during the thermal stress of the PCB fabrication and assembly processes.
- Skin effect is the tendency of an alternating current to become distributed within a conductor such that the current density is largest near the surface.
- Skin depth decreases with increased frequency.
- The nickel content of ENIG surface finish has a ferromagnetic property that can adversely affect electromagnetic fields in the high frequency domain.
- At approximately 2.7GHz, the resonant behavior of the nickel component in ENIG increases insertion loss. It is for this reason, that SMOBC processing should be considered for all high-speed designs.
- Most substrates are copper clad with either RA, ED, or RTF copper.
- To the naked eye, copper clad laminate ap-

pears smooth but at the microscopic level, all materials exhibit surface irregularities.

- The onset frequency of the RMS surface roughness effect is 1.28GHz for ED copper.
- Typical values of surface roughness are 3um for the outer surface and 6um for the inner surface.
- The smoothest surface HVLP material with 1.5um average surface roughness, will not exhibit any noticeable surface roughness effect up to 20GHz. **PCBDESIGN**

References

1. Barry Olney Beyond Design columns: Surface Finishes for High-Speed PCBs and Material Selection for SERDES Design.

2. "How Surface Roughness Impacts High-Performance PCBs," Judy Warner, Microwave Journal.

3. "Effect of Conductor Surface Roughness upon Measured Loss and Extracted Values of PCB Laminate Material Dissipation Factor," Hinaga, Koledintseva, Anmula and Drewniak.

4. "Signal Transmission Loss due to Copper Surface Roughness in High-Frequency Region," Liew, Okubo, and Hosoi.

5. "Roughness Characterization for Interconnect Analysis," Yuriy Shlepnev, Chudy Nwachukwu.

6. "Signal and Power Integrity Simplified," Eric Bogatin.

7. "High-Speed Signal Propagation," Howard Johnson.

8. The ICD Stackup and PDN Planner, www.icd.com.au

Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. This PCB design service bureau specializes in board-level simulation, and has developed the ICD Stackup Planner and ICD PDN Planner software. To read past columns, or to contact Olney, click here.

I^3: Incident, Instantaneous, Impedance

by Martyn Gaudion
POLAR INSTRUMENTS

In my December 2013 column, I discussed "rooting out the root cause" and how sometimes, the real root cause is hidden when digging for the solution to a problem. In that column, I described how sometimes in an attempt to better correlate measured with modelled impedance, fabricators were tempted to "goal seek" the dielectric constant to reduce the gap between predicted and measured impedance.

To cite a common English saying, "There is an elephant in the room," (i.e., something else that is contributing to the error that should be obvious but has perhaps been overlooked). And why is that?

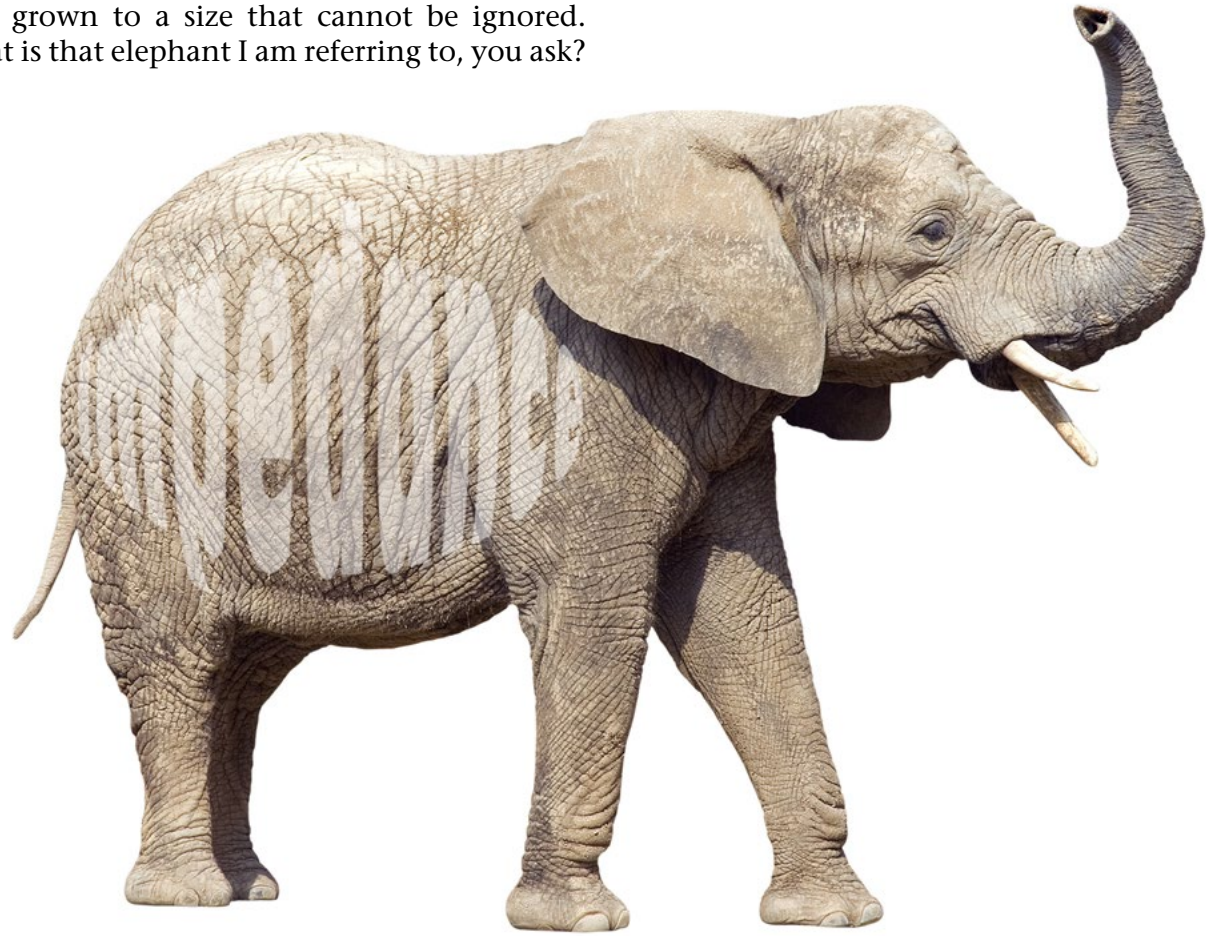
Well, maybe the elephant has been in the room for a while, but it started young and has now grown to a size that cannot be ignored. What is that elephant I am referring to, you ask?

DC and AC resistance of the trace is a good possible candidate for an answer here, something that started very small and has grown gradually and perhaps imperceptibly, until now it is often too big to ignore.

Thinking back to first principles, when designers think of the impedance of a transmission line, it has long been commonplace to ignore the losses. So, look at a lossless line where:

$$Z_0 = \sqrt{\frac{L}{C}}$$

And this is true enough in many cases where the copper is thick enough and the PCB trace



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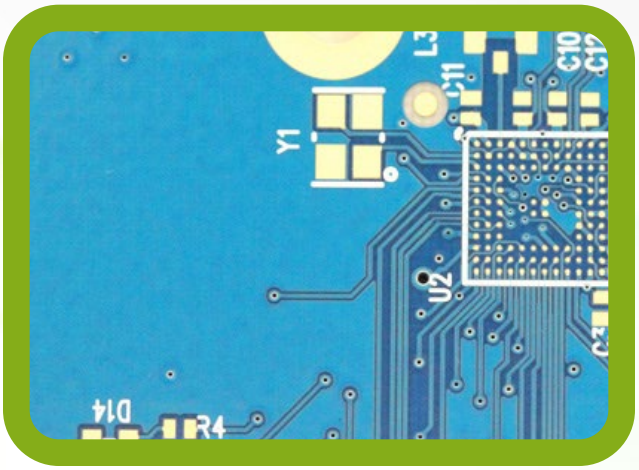

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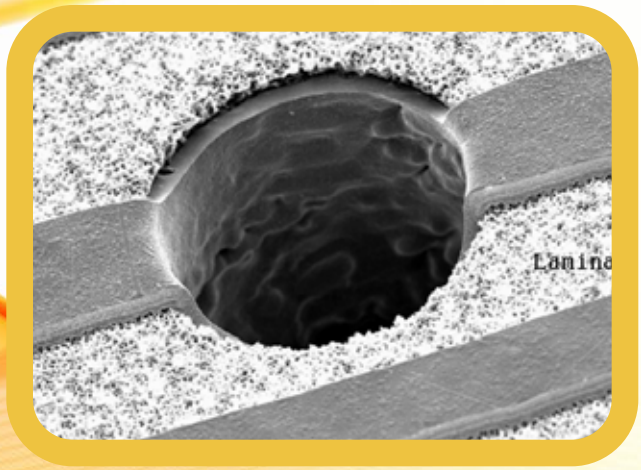

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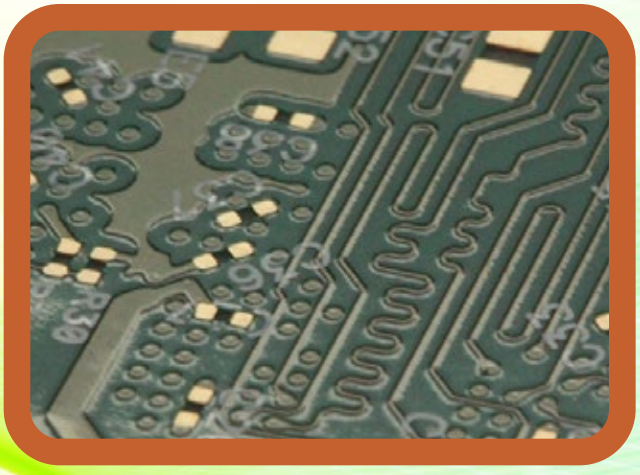

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wide enough for the losses to be ignored. Also, from an instantaneous point of view, the L and C scale per unit length and the ratio of L/C is to all intents and purposes independent of length. However, when geometries shrink, characteristics that could be comfortably overlooked in larger dimensions can no longer be ignored and the uncomfortable fact that the equation for transmission lines approximates to:

$$Z_0 = \sqrt{\frac{L+R}{G+C}}$$

R is the resistance per unit length, a combination of the DC and AC resistance, and the G is the conductance per unit length. Unlike the L and C, unfortunately, the R and G cannot be seen as dimensionless and the R piles up along the trace whilst the G stays close to 0 and the two do not divide out. This means that the TDR trace shows the effect of trace resistance presenting an upward slope as ohm upon ohm of combined DC and AC resistance "pile up" on top of the instantaneous impedance.

Without this knowledge, someone trying to analyze why the measured impedance is somewhat higher than the prediction may seek the source of error. The dimensions are hard to argue with if there is access to precision microsections, especially if three or four sections are taken along the trace and all correlate. So, it may be deduced that, given the dimensions are known and provided the impedance measurement system is calibrated and air line verified, that the only unknown is the dielectric constant. However, deducing (derived from the Latin ducere meaning to lead [1]) is not foolproof: deduction only works if you are certain of the facts. (For example, when you see a person crying, it's easy to deduce the person is sad. Unless they are happy, of course; sometimes happy people cry.) So deducing that an erroneous Er value is the cause of poor measuring and modeling correlation could be challenged if new facts come to light. Sometimes the clue is in the numbers, and I have seen situations where the Er amount has to be "adjusted" to make the impedance correlate appears to defy the laws of physics: for example, when the Er is adjusted to a lower level than each of the primary individual constituents of the base material. This should be a clue that something else is awry here; this is, as I mentioned earlier, the elephant in the room.

In 2009 at DesignCon, Navarro, Chairet and Mayevskiy [2] proposed a technique to measure

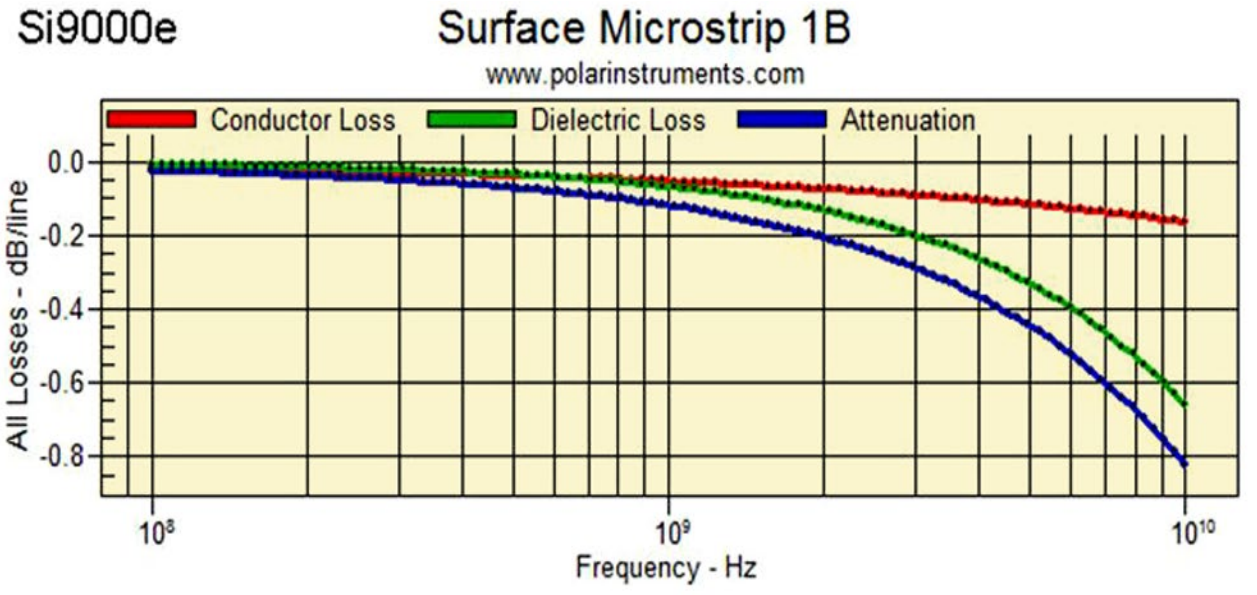

Figure 1: Onset of dielectric loss.

the instantaneous characteristic impedance of high-frequency cables by removing the resistive elements through a technique called launch point extrapolation (LPE) [4]. IPC is now looking at applying this to PCB traces for all the reasons described above. The benefits of applying LPE to PCB trace impedance tests are clear. Linear extrapolation applied to an undisturbed section of the trace and projected back in time to a point close to or at the transition between the probe and the start of the test trace or coupon should remove most of the resistive effects and allow a closer correlation between the modelled impedance and the measured instantaneous impedance. As a precaution and to ensure the copper is not too thin or the line overetched, sometimes a second point is also measured at an imaginary point at the far end of the trace. This ensures that other effects such as trace taper or a higher-than-expected copper resistivity are ruled out.

You might be thinking that "loss" is catered for when measuring insertion loss in the frequency domain, and this is true. But the types of scenario I am referring to in this particular column are those where the lines are operating at "mid" frequencies (i.e., up to one, two or three GHz, where the dielectric losses are still small enough to ignore).

The resistive losses in copper appear at these frequencies because of a couple of reasons: one is the use of thinner copper and the other is that line widths are shrinking too. This means that there are starting to be small but significant losses from DC upwards. To add to that, the onset of skin effect in copper starts to take effect at lower frequencies than need to be considered in the case of dielectric losses.

So it is in this "middle ground" of thin copper/narrow traces and low GHz operating speeds that fabricators and designers start to see impedance traces which rise over time, i.e., distance, with the cumulative build up of resistive effects. This effectively means you need to look at the operating frequency band and the trace geometry and the combination of these to choose the most appropriate method for measurement.

With low-frequency wide traces, trace capacitance is the predominant issue.

With medium-frequency 1 or 2 GHz wide traces, lossless impedance:

$$Z_0 = \sqrt{\frac{L}{C}}$$

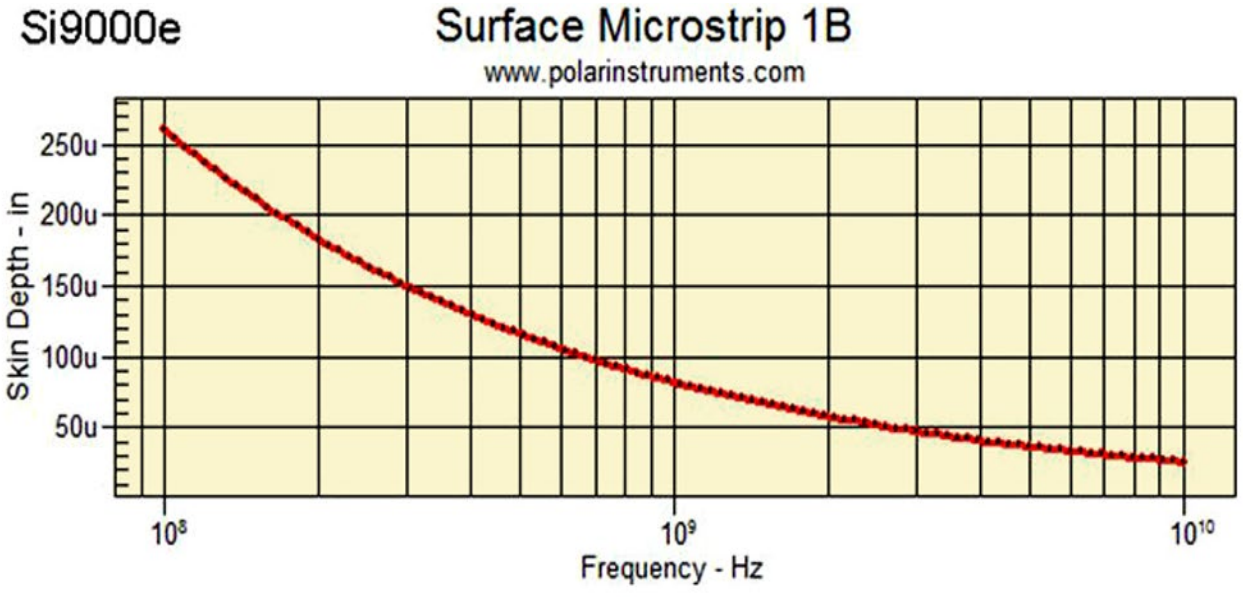

Figure 2: Skin depth.

I³: INCIDENT, INSTANTANEOUS, IMPEDANCE *continues*

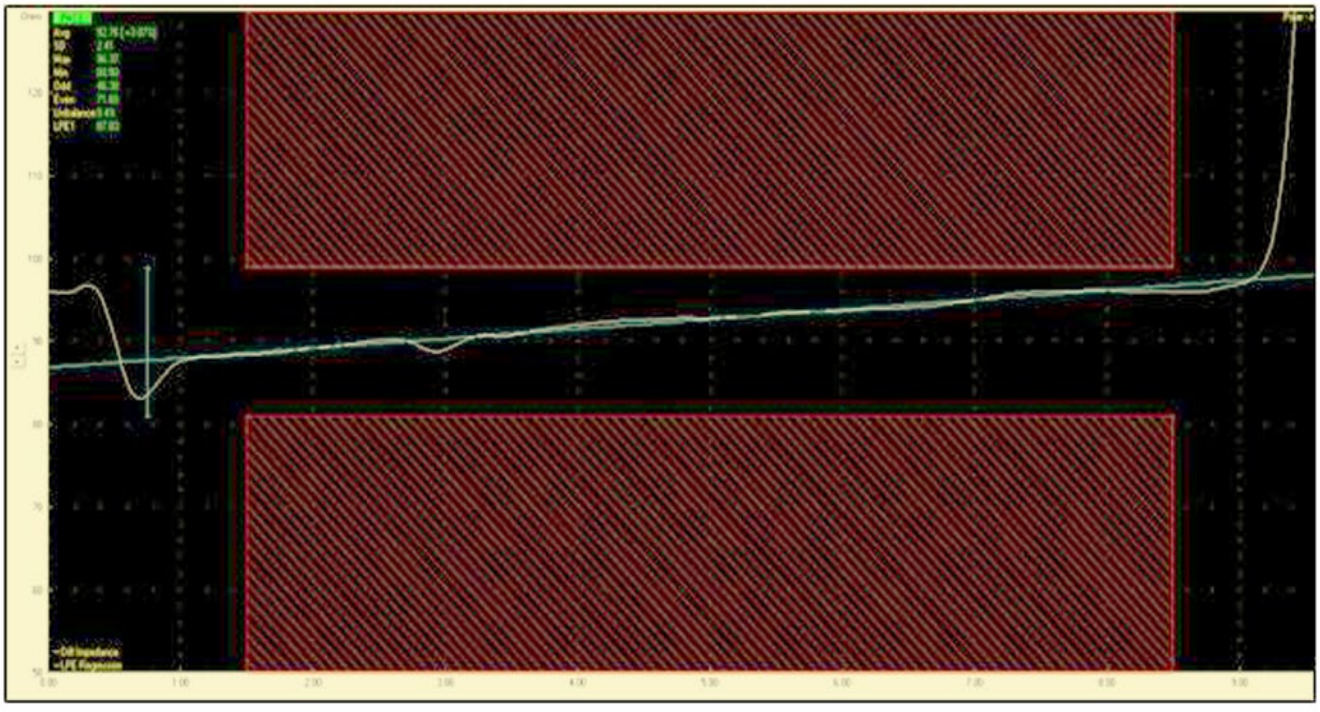

Figure 3: TDR trace with LPE and sloping impedance result.

Medium frequency 1 or 2 GHz narrow traces, impedance:

$$Z_0 = \sqrt{\frac{L+R}{C}}$$

At high frequencies, 3 GHz and above, insertion loss is significant:

$$Z_0 = \sqrt{\frac{L+R}{G+C}}$$

In conclusion, when looking at transmission line measurements and specifying transmission line characteristics, you should ensure that if you are working with narrow traces and thin copper and your frequencies are not yet high enough to worry about dielectric losses, you should take a look at your TDR waveforms for a significant slope in the measurement area. Consider specifying the measurement of instantaneous impedance by using Launch Point Extrapolation. **PCBDESIGN**

References

1. "Deduce" definition: www.vocabulary.com.
2. Luis Navarro, Timothy Chairet, Eugene Mayevskiy, "Application of Launch Point Extrapolation Technique to Measure Characteristic Impedance of High-Frequency Cables with TDR," DesignCon 2009.
3. Lossy Traces: Where and How to use Loss Compensation, Polar Instruments Application Note AP156.
4. Measuring Impedance on Thin Traces with Launch Point Extrapolation, Polar Instruments Application Note AP8505.

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Effects of DC Bias on Ceramic Capacitors

by Istvan Novak
ORACLE

The density of multilayer ceramic capacitors (MLCC) has increased tremendously over the years. While 15 years ago a state-of-the-art X5R 10V 0402 (EIA) size capacitor might have had a maximum capacitance of 0.1 uF, today the same size capacitor may be available with 10 uF capacitance. This huge increase in density unfortunately comes with a very ugly downside: the capacitance is now very sensitive to DC and AC bias across the part.

MLCCs are manufactured with different types of ceramics. With a given case size, dielectric thickness and plate count, the capacitance is proportional to the dielectric constant of the ceramic: the higher the dielectric constant, the more capacitance we get from the same structure. For low-loss, high-performance RF and microwave applications Class 1 materials are used [1]. These provide very good and stable electrical characteristics, practically zero bias and temperature dependence, but their relative dielectric constant is below 100 and hence capacitance density is low. In a 0402-size package we may get 1000 pF with 50V rating. If we need more capacitance in a small package, we have to select Class 2 (or Class 3) ceramics [2], which are ferroelectric materials with a dielectric constant in the 200 to 14000 range.

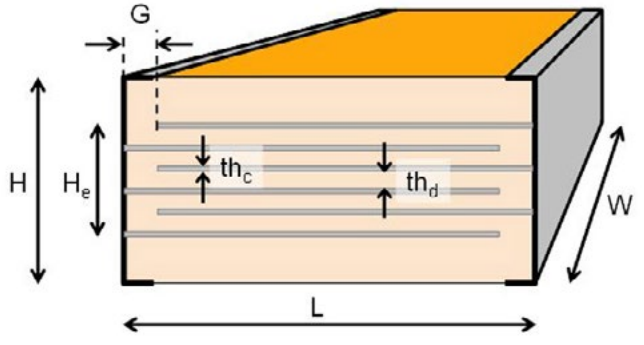

Figure 1: Approximate internal geometry of MLCC.

A typical two-terminal MLCC internal geometry is shown in Figure 1. The two vertical metal terminals connect every other horizontal plate, creating a number of parallel-connected parallel-plate capacitor segments. The stack of capacitor plates fills the H total capacitor body height with an effective height of H_e. The non-connected capacitor plates should not come out to the sidewall of the capacitor body, they are pulled back to create a small G gap. If, for now, we ignore these gaps and consider $H=H_e$ and $G=0$, each pair of adjacent capacitor plates creates a C_u unit capacitance:

$$C_u = \varepsilon_0 \varepsilon_r \frac{LW}{th_d}$$

where e_0 is the dielectric constant of vacuum, or 8.85 pF/m, and e_r is the relative dielectric constant of the ceramic material. In the capacitor body altogether we have N plate pairs, where N (if we ignore the end effects) can be approximated with

$$N = \frac{H}{th_d + th_c}$$

The total capacitance from the N pairs of capacitor plates gives us the following formula:

$$C = \varepsilon_0 \varepsilon_r \frac{LWH}{th_d(th_d + th_c)}$$

In the above expression the LWH product is the volume of the capacitor body. For regular ceramic capacitors the H height typically does not exceed the W width; for a given case size

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this creates the LW^2 upper limit for the volume. To increase capacitance, either the e_r relative dielectric constant has to increase, or the th_d and/or th_c thickness values have to decrease. In case the conductor thickness is much less than the dielectric thickness, the capacitance grows with the inverse square of the dielectric thickness. This gives a convenient scaling possibility to improve the volumetric density of ceramic capacitors: if we use thinner dielectric layers, in the given case size we can produce more and more capacitance.

However, as we make each dielectric layer thinner, the E field strength from the same V voltage applied across the part grows proportionally:

$$E = \frac{V}{th_d}$$

Also, if we increase the e_r dielectric constant, the D electric displacement field will grow proportionally:

$$D = \varepsilon_0 \varepsilon_r E$$

If we plot the relationship between E and D in high dielectric constant ferroelectric materials (Figure 2), D will not follow it proportionally and eventually the curve flattens out, which is called saturation.

Over the many years as we, the users, kept asking for more capacitance in the same package, this scaling helped the industry to give us what we asked for. But we get not only more capacitance; we also get more bias sensitivity. Today the detailed data sheets from major MLCC vendors give us the typical bias sensitivity we can expect from MLCC parts, but unfortunately this kind of data is not a guaranteed specification. In case we want to collect our own data, the techniques and instrumentation is available in professional form [4]. When we look at the data sheet values or at our own measured data [5], we can see in some applications we can easily lose up to 80% of the capacitance just to DC bias effects.

We can also use simple homemade equipment to measure complex reflections and complex impedance and from that we can back-calculate capacitance. Figure 3 shows the DC bias effect measured with a homemade vector-network analyzer on a 100 uF MLCC.

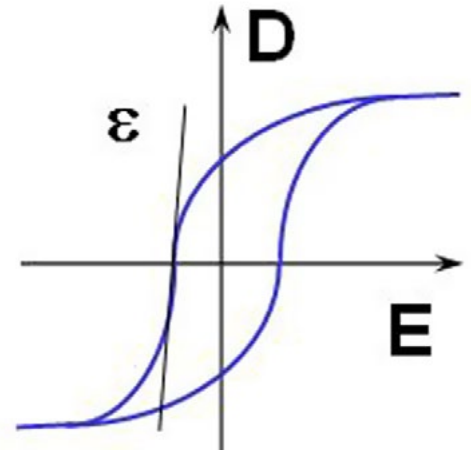


Figure 2: Relationship between the E and D fields in ferroelectric materials.

The 3D surface is put together from multiple individual frequency sweeps, each with a different DC bias value across the capacitor. The DC bias voltage is shown on the left axis; the right axis shows frequency. Note that the capacitance depends not only on the bias voltage, but also on frequency. None of these dependencies are present in Class 1 ceramic capacitors. Figure 4 shows the bias-dependence surface for a 0.1 uF COG MLCC.

The 3D surface of Figure 4 is flat in both directions until we start approaching the series resonance frequency of the part. There is an increasing noise on the measured surface at very low frequencies. At 100 Hz the impedance magnitude of a 0.1 uF capacitor is more than 10 kOhm. The noise illustrates the limitation of the simple home-made instrumentation when we try to measure kilo-ohm impedance values in two-port shunt-through connection.

So, be careful when you use a 6.3-rated Class 2 ceramic capacitor in a 5V application: a big percentage of the capacitance may be gone. The good news is that this bias dependence is hardly present in tantalum and aluminum capacitors, film capacitors and printed-circuit laminates. **PCBDESIGN**

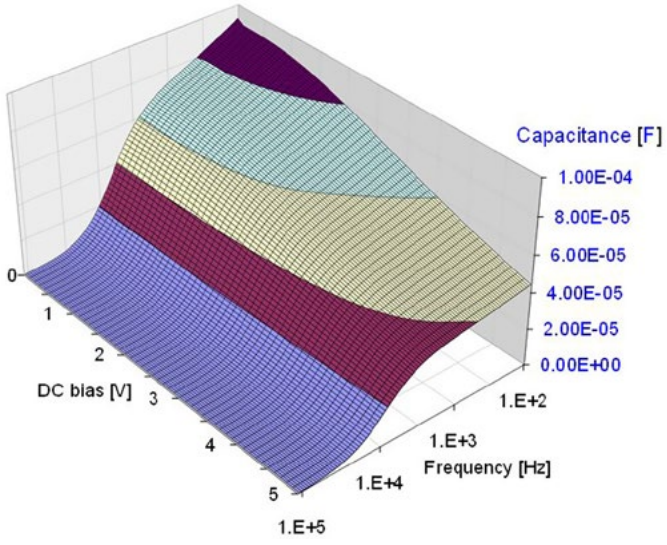


Figure 3: Capacitance as a function of frequency and DC bias, as measured on a 100 uF 4V Class 2 MLCC part.

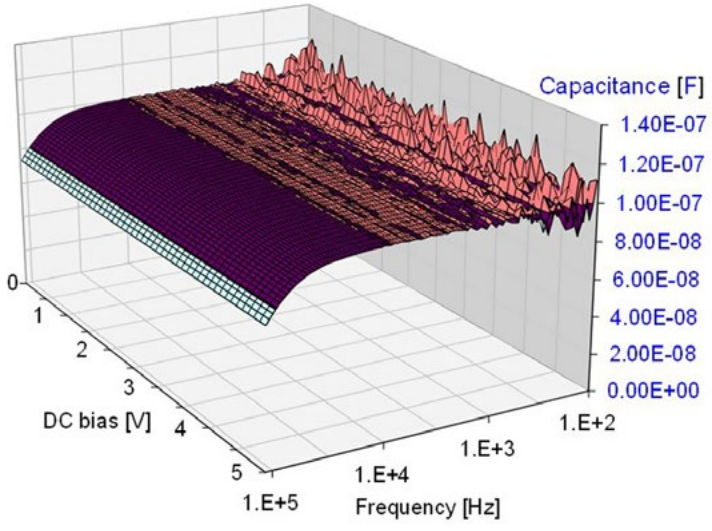


Figure 4: Capacitance as a function of frequency and DC bias, as measured on a 0.1 uF Class 1 MLCC part.

References

1. Wikipedia: Class 1 ceramic capacitors.
2. Wikipedia: Class 2 ceramic capacitors.
3. Wikipedia: Permittivity.
4. Accuracy Improvements of PDN Impedance Measurements in the Low to Middle Frequency Range," DesignCon 2010, February 1–4, 2010, Santa Clara, CA.
5. DC and AC Bias Dependence of Capacitors Including Temperature Dependence," DesignCon East 2011, September 27, 2011, Boston, MA.

Dr. Istvan Novak is a distinguished engineer at Oracle, working on signal and power integrity designs of mid-range servers and new technology developments. With 25 patents to his name, Novak is co-author of "Frequency-Domain Characterization of Power Distribution Networks." To read past columns, or to contact Novak, click here.

Controlled Impedance: A Real-World Look at the PCB Side

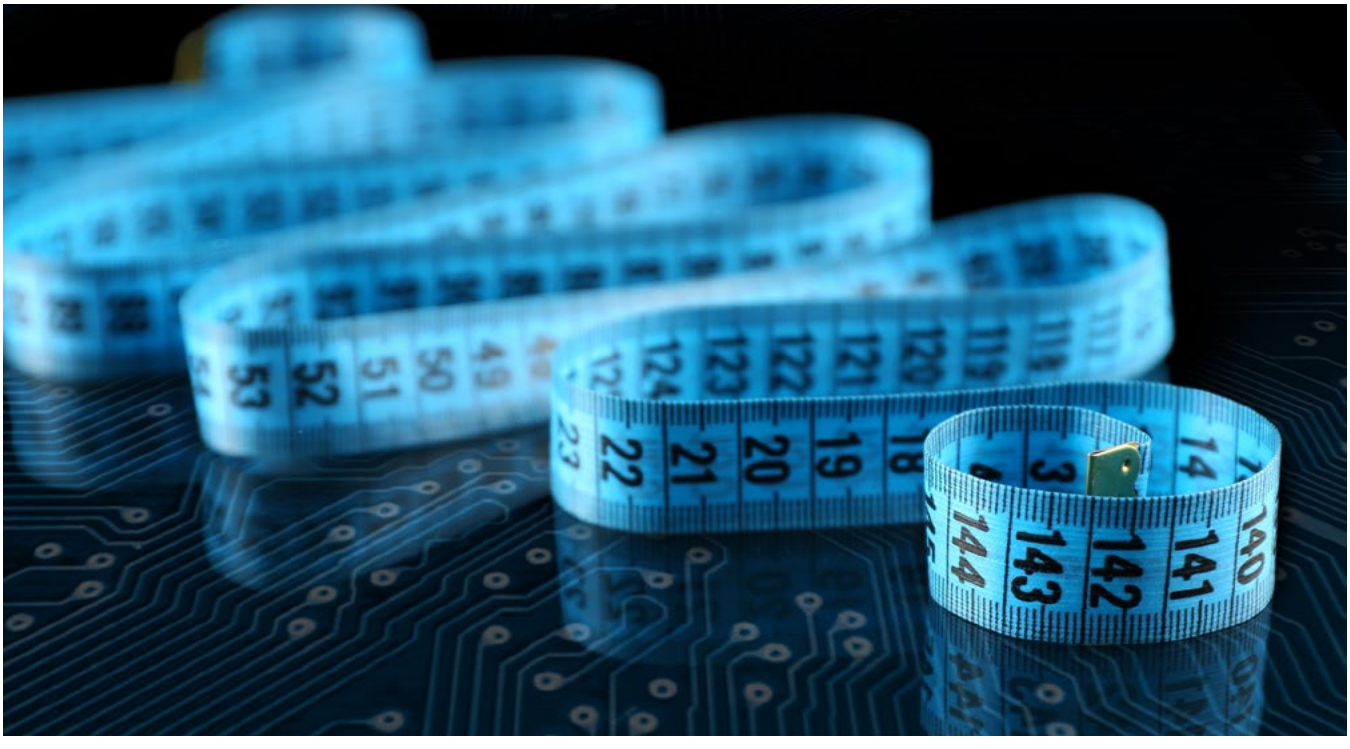
by Dan Beaulieu and Bob Tarzwell

DAN: When I was a very young man, way back in the taped artwork days of the 1970s, I was a program coordinator (a fancy name for expeditor) at Rockwell's Maine Electronics in Lisbon, Maine. One of my programs was the Burroughs Scientific Processor (BSP) created by Burroughs Corporation, based in Paoli, Pennsylvania. We were building very high-tech 14- and 16-layer boards for this program. We were told that these BSP computers were so powerful that the first one was already "running" the airport in Narita, Japan.

Now, this was 1975, mind you. The only computer I had ever seen was being installed in a glass room at the company. I was walking around tracking my PCBs with a pen and clipboard and I had no idea what "running an airport with a computer" even meant. By the way, I did get a chance to see a BSP system being built. It was quite an impressive sight, especially since they had slimmed it down to three refrigerator/freezer-sized units. I remember being amazed that something that small could run an entire airport!

And this was the first time I had ever heard of impedance. All I knew about it was that these two guys, Bob McQuiston from Burroughs and Andy Yenco from Maine Electronics, spent weeks building literally hundreds of boards, inventing ways to measure this impedance thing and then throwing out most of them. It would break my heart to carry all of these great looking boards to the scrap heap day after day.

Finally, one day I heard Andy let out a whoop and slap Bob on the back (there was no man-hugging back then). They had done it! They had finally built and measured some boards with the right controlled impedance. That was 40 years ago, so I'm thinking that maybe I saw the first controlled impedance boards



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CONTROLLED IMPEDANCE: A REAL-WORLD LOOK AT THE PCB SIDE *continues*

being built and measured. Now, can somebody please tell me what controlled impedance is? Bob Tarzwell, can you help me out here?

BOB: Sure, Dan. And to make this really useful (I'm never sure if you really understand my answers to your eternal questions anyway), I'll direct my answer to those guys who really care, the PCB designers.

As a designer, your project may require a specific impedance of, say, 52 ohms, plus or minus 7% percent. The big question is: Does the fabricator give you what you ask for? Well, maybe, and maybe not. Here is why.

The standardized coupon the PCB manufacturer inserts into the panel is designed to reproduce the same impedance effects your circuit should see, but because it is not inside the circuit it's only a close approximation test. When PCB manufacturers set up the panel, of course they use as much of the panel as possible, which means the impedance coupon will be on the outside of the production 18x24" panel. The question would be, is there any difference between the center of the circuit board and the very outside where the impedance coupon is located? Unfortunately many times the answer is yes.

"The problems associated with the lamination cycle and differences between measuring methods and machines can mean four different test coupons on four different machines, which can result in 16 different measurements. Which one is right? Well, perhaps all of them; impedance is an elusive, theoretical number, and the standard PCB coupon's impedance does not always represent the exact impedance inside the shipped PCB."

The edge of the PCB does have slightly different impedance characteristics than the center; the edge can have less resin than the center due to resin flowing out at the edge of the lamination book. The resin/glass percentage across the entire panel determines the impedance; the more resin, the higher the impedance.

Why do the edges have different resin/glass percentages? As the layup book in the hydraulic press heats up, the different layers do not always heat at the same rate—the outside panels will heat quicker than the inside ones. The rate of change in the temperature through a critical point near the Tg of the resin system will affect how much resin will flow out of the package. Typically we can see a wide range of resin squeeze out along the edge of the lamination package, from a small dark brown flow indicating very little resin loss, to a larger white flow with a lot of air bubbles equating to a lot of resin movement out of the lamination package.

The problems associated with the lamination cycle and differences between measuring methods and machines can mean four different test coupons on four different machines, which can result in 16 different measurements. Which one is right? Well, perhaps all of them; impedance is an elusive, theoretical number, and the standard PCB coupon's impedance does not always represent the exact impedance inside the shipped PCB.

The PCB manufacturer also has a few disadvantages to work around to achieve the 5 or 7% impedance measurements you require. The prepreg used to laminate cores together only comes in a few various thicknesses, and each thickness has a different Dk due to its different resin content, and it also has relatively wide variations in that resin/glass percentage.

Also, the cores they buy direct from the manufacturer will have a slightly different Dk than the same prepreg if they tried to copy the core directly. The core laminate manufacturers use fresher prepreg and much larger lamination presses than the PCB manufacturer. To add to the confusion, the impedance calculators are not always correct; all impedance calculating equations are approximations. Each PCB manufacturer will add or subtract a bit (5–10%) to account for their particular lamination press

cycle, material and the amount they will press out the resin.

Another area where the variability of PCB manufacturing affects the coupon differently than the circuit is etching. Typically, the process of copper plating and etching varies in etchback around the PCB based on density (i.e., denser center areas of the actual circuit will plate a bit less and etch a bit finer than the outside edge where the impedance coupon is located). Copper plating has the nasty effect of plating areas of less copper density at a higher rate than on more dense areas of the PCB. The thickness of the copper is one of many variables in determining final impedance calculations. The etch rate across the PCB is also affected by circuit density, with typically less dense outside areas where the impedance coupon is located being slightly overetched, and line width is a major factor in impedance numbers.

> "If the impedance coupon is not the correct impedance, does that mean the PCB is bad? Not really, as most PCB manufacturers will do a cross-section and verify the trace width, thickness and dielectric spacing, and if they are built as designed, one must assume that the coupon is incorrect."

If the impedance coupon is not the correct impedance, does that mean the PCB is bad? Not really, as most PCB manufacturers will do a cross-section and verify the trace width, thickness and dielectric spacing, and if they are built as designed, one must assume that the coupon is incorrect. I did a test with one coupon on two identical impedance measuring units. They were over 10% different; one operator had his hand close to the circuit, and one machine was on a stainless steel countertop. But even after correcting the difference in setups and measuring techniques, the units were still 6% different. As the coupon was just over the specified impedance, the PCB manufacturer did a cross-section and everything was within design specifications. The customer was notified of the difference and the subsequent cross-section retest, and the boards worked as planned.

Many designers do not know that the impedance in a PCB trace varies significantly as it winds its way inside the PCB circuit. Traces close to ground planes, other traces running along the same path—even the thickness of the soldermask all change the impedance at that particular point of the trace. There can be a 2x impedance difference in two close points along a trace, if one point is close to a glass bundle and a second point along the same trace is a few thousandths of an inch away over a high-resin section. However, the average impedance along the trace will be close to the designed ohms.

The balance between what the designer needs in his matching impedance traces and what a PCB shop can deliver is really not that far apart. As a designer, you should be knowledgeable of the limitations and actual usefulness of the coupons we and the PCB shop uses use to obtain the desired impedance. If you have a difficult design, contact your PCB manufacturer. I know that they will gladly run the design criteria through their different calculators to help solve the problem.

So there you go, Dan. I hope you caught all that. **PCBDESIGN**

Bob Tarzwell is a PCB consultant who has spent 50 years in the PCB industry, inventing technology and building almost every type of PCB. He is the co-owner of DB Publishing, publisher of the *PCB 101 and Quality 101* handbooks. For more information, visit www.dmrpcb.com.

Dan Beaulieu is a well-known industry consultant and co-owner of DB Publishing. His column *It's Only Common Sense* appears Monday mornings in the I-Connect 007 Daily Newsletter. He can be reached at danbbeaulieu@aol.com.

Advanced Boards Drive Demand for AOI Equipment

Currently, AOI is chiefly applied to PCB and TFT-LCD industries. However, for China, the penetration of AOI in the two industries is still rather low, with only 20 to 30% of production lines in the PCB industry equipped with AOI.

Cicor Improves Financial Flexibility with New Financing

The arranged credit facility with a consortium of banks, led by Commerzbank Aktiengesellschaft, has a duration of three years, with two extension options of one additional year each, therefore running for a maximum term of five years.

HKPCA & IPC Show Sets New Attendance Records

This year's show again broke all previous records for participation, making it not just the largest ever in the 13-year history of the event, but the largest trade show in the entire world for the PCB and electronic assembly industry.

Omni Circuit Boards Signs R&D Agreement with D-Wave

Omni Circuit Boards Ltd. announced today the signing of a research and development agreement with D-Wave Systems Inc., the first commercial quantum computing company, in support of the further advancement of aluminum trace printed circuit boards (Al-PCB) for quantum computing applications.

AT&S Offers Embedded Power Electronics

Due to constant technology development and strong partnerships, AT&S has achieved outstanding results in the field of power electronics. This solution provides a significant increase in efficiency and performance for industrial and automotive applications.

MFLEX Concludes Solid Q4 Financial Results

Reza Meshgin, Chief Executive Officer of MFLEX, commented, "We generated another quarter of solid profitability during the December quarter. Strong demand, including continued contribution from our group of eight newer customers, supported an anticipated 21 percent sequential increase in net sales."

TTM Receives Foreign Approvals to Acquire Viasystems

TTM Technologies Inc. has received the approvals of the Ministry of Commerce of the People's Republic of China, the Federal Cartel Office of Germany, and the Estonian Competition Authority to proceed with the acquisition of Viasystems Group, Inc.

Saturn Electronics Opens Doors for PCB Tours

Saturn Electronics is opening its doors to customers this January as part of its "Open House" initiative, where PCB experts from the company will be on hand to answer any questions regarding the fabrication process of the PCB and Saturn Electronics' capabilities at its Romulus, Michigan facility.

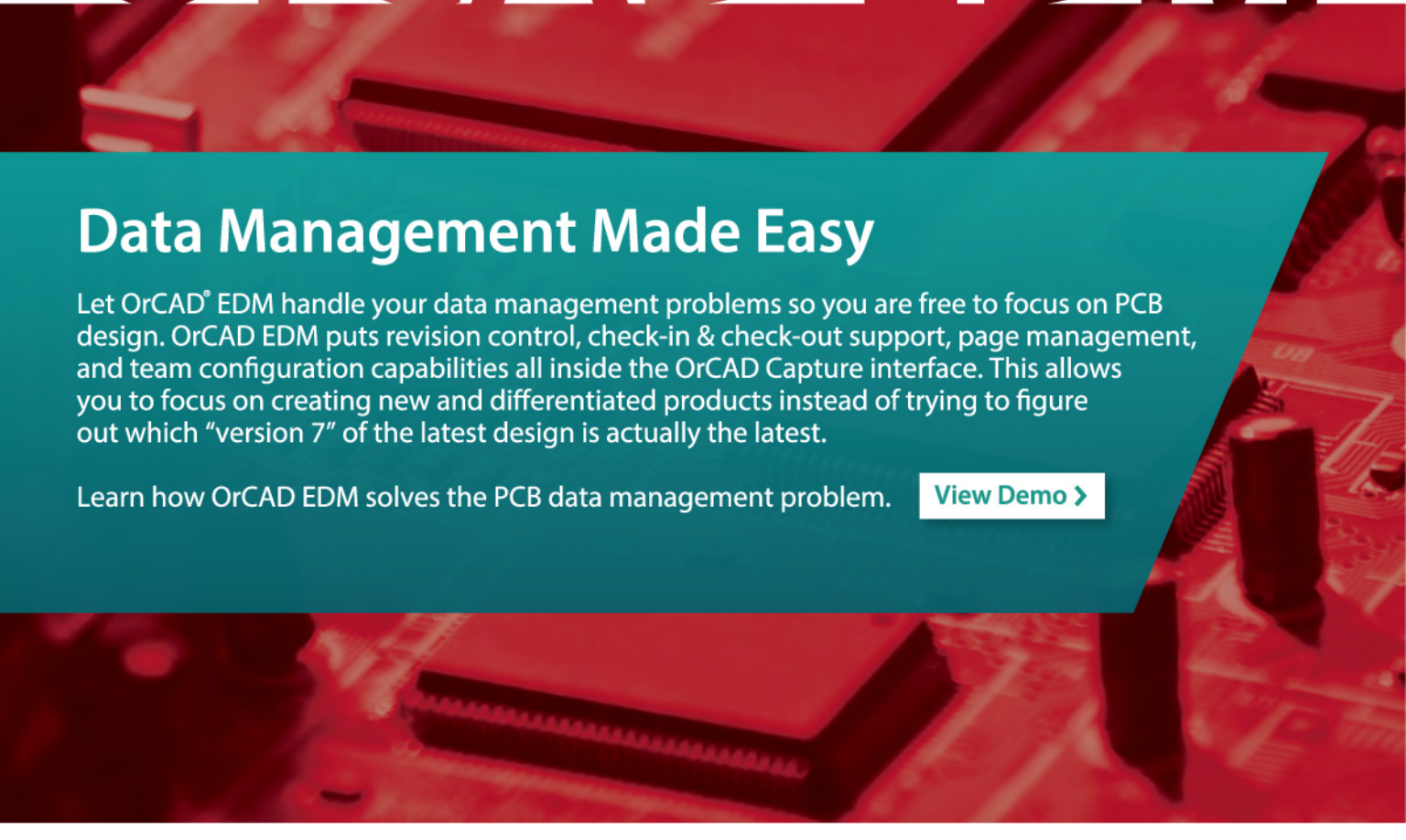
IPC: N.A. PCB Order Growth Bolsters Book-to-Bill Ratio

"Although PCB sales in North American continued below last year's level in November, orders again came in above last year," said Sharon Starr, IPC's director of market research. "Strong orders in the fourth quarter have driven the book-to-bill ratio into positive territory, which offers hope that year-on-year PCB sales growth will turn positive in 2015."

IPC Establishes Local Presence in Korea

The Standards Committee of IPC Korea will help members to develop and revise global standards, educate and train workers, provide technology consultation, hold technology development forums, standardize electronics terminologies in Korean, and hold networking events. This will help establish a collaborative relationship among the government, electronics industry, and academia.

INTRODUCING THE REVISION TRACKING HEADACHE AVOIDING FILE MANAGING KNOW WHO DID WHAT WHEN OrCAD EDM



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Insertion Loss: A Bigger Concern in High-Speed Digital?

by John Coonrod
ROGERS CORPORATION

In the past, one of OEM customers' main concerns when dealing with their PCB fabricators was characteristic impedance. Many times, a PCB design is considered controlled impedance and the PCB fabricator is held to a specification for impedance control. A design may be 50 ohm nominal impedance, and the PCB is tested to show that it has the correct impedance within some tolerance. The tolerance is sometimes ± 10%, other times ± 5% or less.

As digital rates continue to increase, there are more requests for fabricators to perform insertion loss and other types of electrical testing. Understanding the basics of digital signaling can help explain why these new electrical tests are desired for ensuring a quality PCB for high-speed digital applications.

Digital pulses are made up of analog sine waves. In order to make a digital pulse, sine waves of different frequencies are added together to form the digital pulse. Each of these sine waves is a high-frequency RF wave at a specific frequency. As an example, when a 10 Gbps pulse is generated from a combination of the RF waves, the frequencies used will be approximately 5 GHz, 15 GHz, 25 GHz and 35 GHz added together. Actually there can be more, but this is a simple example of showing the adding of sine waves using the fundamental harmonic (5 GHz), 3rd harmonic (15 GHz), 5th harmonic (25 GHz) and the 7th harmonic frequency at 35 GHz.

Figure 1 shows how the digital pulse can be formed from adding these sine waves.

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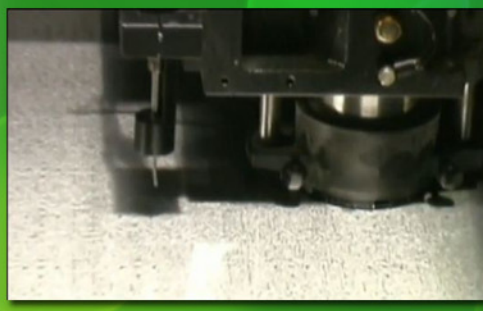

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INSERTION LOSS: A BIGGER CONCERN IN HIGH-SPEED DIGITAL? *continues*

In reality, digital pulse generation is more elaborate than shown here, but Figure 1 gives an example why high-speed digital applications have more concern with high-frequency RF components. One big concern with high-frequency RF components is insertion loss and if the RF wave has more loss for the 7th harmonic as compared to the 3rd harmonic, then digital pulse will not be well formed.

The example given in Figure 1 assumes a 10 Gbps application and if a high-speed digital application is at 28 Gbps then the corresponding frequencies will be 14 GHz, 42 GHz, 70 GHz and 98 GHz. This example is using very high-frequency RF components and the losses are typically much worse as the frequency increases. In this example the difference for insertion loss between 14 GHz and 98 GHz can be extreme. The insertion loss difference can cause the amplitude of one RF signal to be different than another, which can cause poor digital pulse formation.

PCB fabricators typically use a time domain reflectometer (TDR) to test PCBs for impedance. However, very few fabricators have the equipment necessary to test PCBs for insertion loss. Although a network analyzer is typically used for insertion loss characterization, some test methods have defined the use of TDR to obtain insertion loss.

The circuit materials needed to support these high-speed digital applications, where insertion loss is critical, are typically defined by dissipation factor, although copper surface roughness is another key factor for insertion loss. For existing and previous digital applications, circuit materials that are considered mid-loss have been used. Mid-loss substrates have dissipation factors of

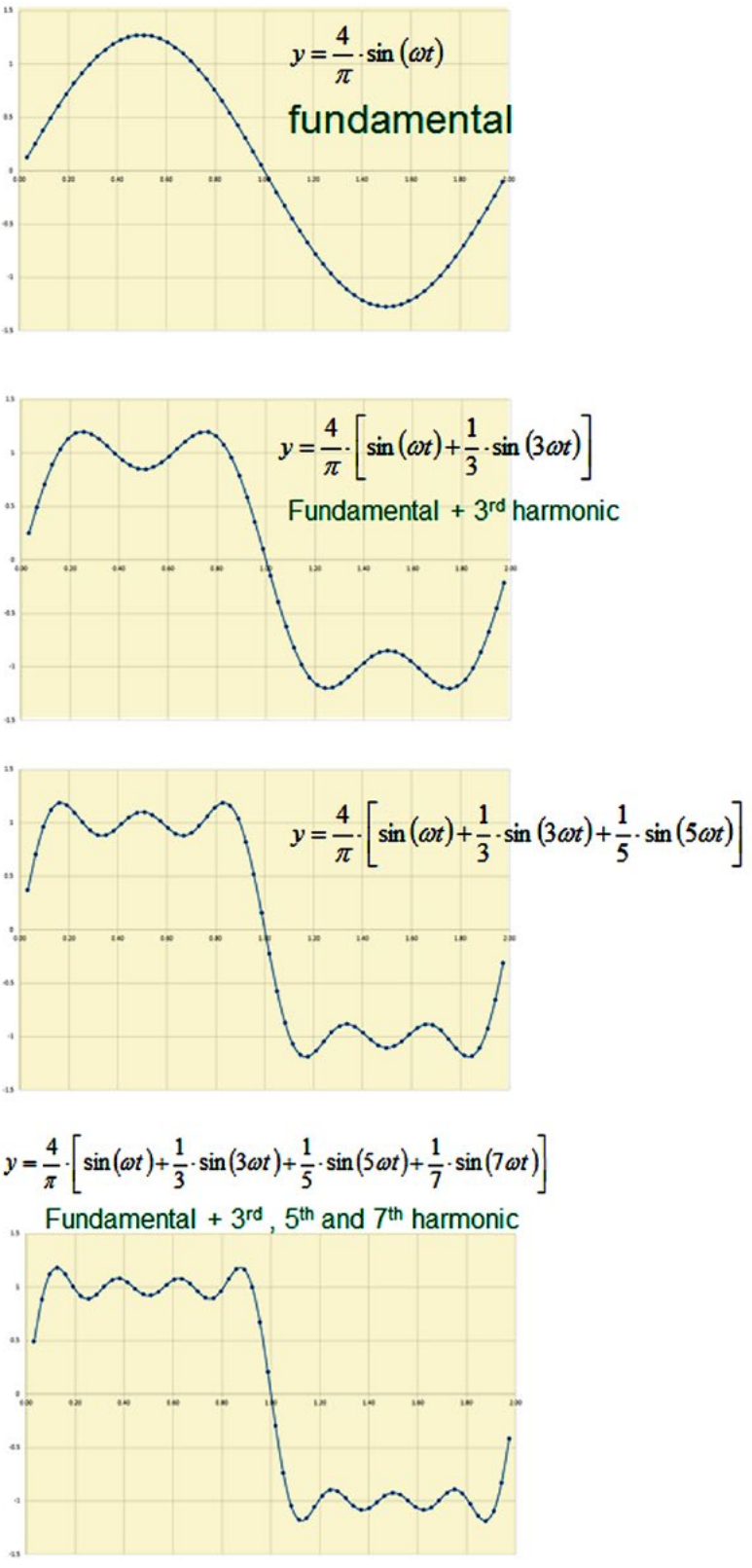


Figure 1: Adding sine waves of different frequencies can form a digital pulse.

INSERTION LOSS: A BIGGER CONCERN IN HIGH-SPEED DIGITAL? *continues*

about 0.010 or less. These materials will likely cause too much insertion loss for 10 Gbps digital rates and circuit materials with lower loss are necessary.

The low-loss material used for 10 GBps applications usually has a dissipation factor of 0.005 or less. The next generation high-speed digital designs will probably be in the range of 25 to 28 Gbps and then another shift for low-loss material will be necessary and these materials will be considered very low-loss materials with dissipation factor in the range of 0.003 or less. Finally, some early work with 56 Gbps has shown that extremely low-loss or ultra-low loss materials with a dissipation factor of 0.0015 or less are necessary. **PCBDESIGN**

John Coonrod is a market development engineer for Rogers Corporation, Advanced Circuit Materials Division. To read past columns, or to reach Coonrod, click here.

Electronic Circuits with Reconfigurable Pathways

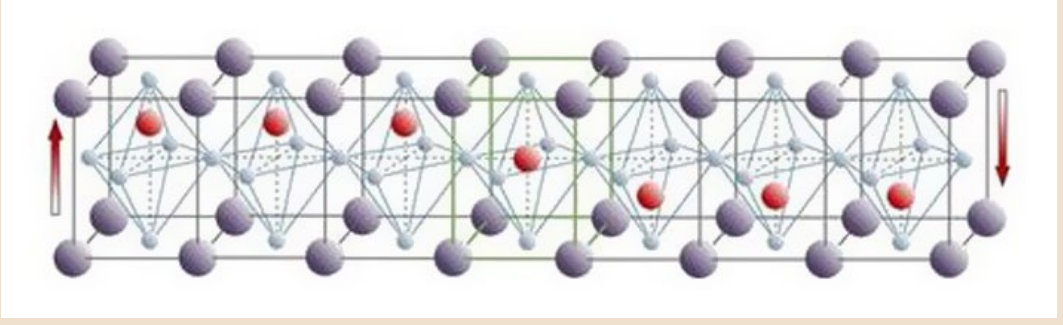
Multitasking circuits capable of reconfiguring themselves in real time and switching functions as the need arises—this is the promising application stemming from a discovery made at EPFL and published in Nature Nanotechnology. Other potential uses: miniaturising our electronic devices and developing resilient circuits.

Adaptable electronics is generating significant interest in the scientific community because of the many applications. Imagine for a moment that one single microchip was capable of accomplishing the tasks of several different circuits.

Underlying this promising technology are so-called "ferroelectric" materials in which it is possible to create flexible conductive pathways. These pathways are generated by applying an electric field to the material. More specifically, when the electric current is applied, certain atoms moves either "up" or "down," which is known as polarisation. In recent years, the academic world has observed that conductive pathways several atoms wide—called 'walls' – form between these polarized zones. The only problem is that, until now, it was impossible to control how these pathways form.

At EPFL, the researchers demonstrated that it was possible to control the formation of walls on a film of ferroelectric material, and thus to create pathways where they wanted at given sites. The trick lies in producing a sandwich-like structure with platinum components on the outside and a ferroelectric material on the inside.

At this point, the researchers have tested their research on isolated materials. The next step consists in developing a prototype of a reconfigurable circuit. Leo McGilly would go even further. "The fact that we can generate pathways wherever we want could allow us to imitate in the future phenomena that take place inside the brain, with the regular creation of new synapses. This could prove useful in reproducing the phenomenon of learning in an artificial brain."



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News Highlights

FlexTech Lauds Gov't Approval of Flex Hybrid Electronics

The industry consortium fostering the growth, profitability, and success of the flexible and printed electronics supply chain welcomes the U.S. Government's selection of flexible hybrid electronics (FHE) as the next topic for a Manufacturing Innovation Institute (MII). FHE was one of several topics under consideration and joins eight other technologies already identified for MIIs.

New Defense PCB Regulations Take Effect December 30

The changes to the U.S. Munitions List, which is regulated through the International Traffic in Arms Regulations, states that PCBs "specially designed" for defense-related purposes will be controlled under USML Category XI. Additionally, any designs or digital data related to "specially designed" PCBs will be controlled as technical data.

Elvia PCB Renews Nadcap Certification

"The renewal of the Nadcap certification shows strong continuity in the technology and quality support that we provide to our strategic customers" commented Edouard Piedagnel, site Operations Director of Elvia PCB Group's main plant. "This is a true sign of maturity for Elvia PCB Group, which enables us to continue to offer the most up-to-date standards to our strong, growing aerospace customer base, both in Europe and the Americas," added Benoit Hareng, head of international sales.

Military Infrastructure, Logistics Market Post Growth

The report forecasts the industry to grow at a CAGR of 1.29% during 2014–2019. Developing countries in the BRIC are placing military infrastructure and technology revamp at the top of their priority lists.

DoD Awards Accreditation of Trust to Hunter Technology

The company announces that it is one of only 60 suppliers to achieve an Accreditation of Trust from Defense Microelectronics Activity (DMEA), and is the only accredited EMS provider owned and operated exclusively in the U.S. As an accredited trusted supplier, Hunter addresses counterfeit risk using a proprietary system that meets all 12 requirements set forth by the Defense Federal Acquisition Regulation Supplement (DFARS).

Electric UAV Market to See 18% CAGR for 2013–2018

According to this electric unmanned aerial vehicles market (UAV) report, the industry will grow at 18.20% CAGR for 2013–2018. The cost-effectiveness of UAVs is a major draw for buyers in this market.

NASA Enters Collaborative Partnerships

The Collaborations for Commercial Space Capabilities (CCSC) initiative is designed to advance private sector development of integrated space capabilities through access to NASA's spaceflight resources and ensure emerging products or services are commercially available to government and non-government customers within the next five years.

ESA Performs Experiment with Force-Feedback in Space

NASA Astronaut Berry Wilmore conducted the Haptics-1 experiment on-board the International Space Station. The scientific technology demonstration experiment was conceived, designed, developed, and implemented by the European Space Agency Telerobotics and Haptics Laboratory and sets a new technology milestone for space robotics.

Air Traffic Control Equipment Market Report

ReportsnReports.com adds "Global Air Traffic Control Equipment Market 2015–2019" and "Global Air Traffic Management and Control Market 2014–2018" research reports to its online business intelligence library.

Report: Radiation Detection Devices for Military & Security

The market for radiation detection devices in domestic security will grow from a current market value of $1.35 billion, to $1.92 billion by 2022 and that the military market will grow from a $617 million market today to $868 million by 2022.

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Push the Button, Max

by Tim Haag
INTERCEPT TECHNOLOGY

Many years ago, my dad worked as a television technician at KOIN TV, the local CBS affiliate in Portland, Oregon. He spent his time there operating the cameras, monitoring the audio, fine-tuning the video output, or working one of the two master control boards in the control room. For a 12-year-old boy, it was a fantastic adventure to visit him at work; I spent my time playing in the huge studios, watching different productions being broadcast, and sneaking leftover candy from the little kids' cartoon shows.

But the most prominent memory I have from those days was when I was a little guy, probably five or six years old. My mother had brought me down for a visit and the technicians were all congregated around the larger master control board working on a production that was being shot in the main studio. While this was going on, the network feed was coming in and being processed by the smaller master control board and then going out over the air. Essentially it was on automatic while the technicians on the

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PUSH THE BUTTON, MAX *continues*

large board were working the studio production. I was told to go and sit at that smaller control board to keep me out of the way.

You don't have to be a child psychologist to guess what happened next. I was alone, unsupervised, and sitting in front of a control panel that held millions of levers, knobs, and buttons. I can still hear the very thought that ran through my mind that day: "It won't hurt to push just one."

Of course my eye was attracted to one of the buttons that was lit up (circuit enabled), and I pushed it. Immediately the greater Portland area was without sound for their favorite afternoon TV show on KOIN. And unlike today, when there are hundreds of different programming options to pick from, back then there were only the three big networks and a couple of independent stations. So what I did had a profound impact.

I was too young to understand the seriousness of what I had done, but I still knew that I shouldn't have done it. Through the glass partition that separated the two control boards, I could see my father's head snap up to check the line monitor, then over to check the on-air monitor, and then down to look at me. Up to that point I can clearly remember the events, but after that I don't remember a thing. It's a fair guess though that I was in really big trouble.

"I was too young to understand the seriousness of what I had done, but I still knew that I shouldn't have done it. Through the glass partition that separated the two control boards, I could see my father's head snap up to check the line monitor, then over to check the on-air monitor, and then down to look at me."

Now if this was a parenting magazine, I would probably talk about discipline, trust, and keeping a tight rein on your child so they don't unexpectedly disable TV entertainment for tens of thousands of people. But since it's not, instead I'm going to simply say, "Push the button, Max!"

Does this mean that I am advocating disrespect for authority? Of course not. I believe that children should honor their parents and do their best to be obedient. But as adults, sometimes we need to jump off into the deep end and take a chance on something that is completely out of our comfort zone. Sometimes you just need to push the button and see what happens.

Towards the beginning of my career as a circuit board designer, I was working as a temp employee at a large company. They offered me a permanent position and made a lot of promises, but those promises were attached to a lot of unattractive conditions. The range of design technology was limited and the career path they offered was not very appealing. But the security of a full-time position was a very tempting reason to sign on, and I seriously considered it. On the other hand, though there was this little service bureau that didn't offer the best salary, benefits or security. But the variety of different design opportunities that this job offered was fantastic. So my choice was to either stay where it would be safe, or make the risky jump. I pushed the button, took the chance, and was rewarded with a plethora of rich opportunities to enhance my skill set and design experiences.

At another point in my work history I was enjoying success as a department manager, but as time went by the company started to change. The momentum of the company shifted, my job description was changed, and I could see that my dream of a long career with this company was coming to an end. I could have elected to stay where I was and tough it out for a while, but I decided to move on to a new position with a new company. It was a different company, a different work environment, and I was doing something very new which made it all very intimidating. As it turns out, this new job didn't last for very long and less than two years later I was off again seeking something else.

But forcing myself to jump into the unknown when I did helped me to learn to think

fast, grow, and adapt to change. If I hadn't made the change in jobs when I did, I may have ended up stranded when that first company eventually eliminated my department. But as it was, I pushed the button and rode the wave of uncertainty into a new future.

Some time back, a friend came to me with an idea for a new company. He and I spent many hours developing the basic footprint of how this company was going to work; what our roles were to be, and what kind of resources it would take. We created a business plan and even began talks with investors. Then behind the scenes our plans were derailed by events that we couldn't foresee, and all of our long hours burning the midnight oil on our preparations went up in smoke.

Although it is a disappointment that we were unable to start the business that I had planned on, what I ultimately gained from our efforts was well worth the time spent. I learned about the process of creating a business, developing a plan, and executing it. This gave me a huge sense of confidence knowing that I had done something that I had never expected to do, and that confidence has carried through to this day. If I had listened to the inner voice of fear that said, "Don't get involved. Stay where it's safe. It's not worth the effort," then I never would have benefitted from the new skills and the boost of confidence that these experiences gave me.

"Although it is a disappointment that we were unable to start the business that I had planned on, what I ultimately gained from our efforts was well worth the time spent. I learned about the process of creating a business, developing a plan, and executing it."

Now, I have no idea what your circumstances are and I am in no way advocating that you do something foolish or dangerous. I also would never suggest that you take a big risk without first considering all the possible ramifications. But I am encouraging you to at least take a look at whatever situation you may be up against, and give consideration to any ideas that at first seemed too risky to consider. You are the only person who can make the final decision, but when you are at a jumping off point and you've done your homework and it seems like a good idea, don't be afraid to take a chance.

This Christmas I noticed that I had a strand of Christmas lights that wasn't lit. It was Christmas Eve and I really love those lights on my house, so I was annoyed to find that part of the house was dark due to some wires that had been cut. But here was my dilemma: Should I go without this strand of lights on Christmas Eve, or take a chance by splicing some severed wires back together again and hoping for the best? It was as if the lights were daring me. So on a ladder, at night, in the rain, and armed only with a roll of duct tape and a flashlight, I pushed the button. I really didn't know which wire went with which, but I took my best guess based on their length and was rewarded once again with a fully lit house.

Not every chance we take will work out the way we want it too, I've certainly had my own share of misses. But I have also been amply rewarded with confidence, unexpectedly rich new experiences, increased skills, and even the simple joy of colorful Christmas lights by taking a chance. Sometimes you just need to "Push the button, Max." Oh, and if anyone out there can correctly name which movie that quote came from, Editor Andy Shaughnessy will give you a free subscription to this magazine! (Of course, this magazine is free already.)

See you next time. **PCBDESIGN**

Tim Haag is customer support and training manager for Intercept Technology.

Welcome to the 2015 IPC APEX EXPO Show Guide

Feb. 22-26, 2015, San Diego Convention Center, California, USA

This year, IPC APEX EXPO returns to sunny San Diego, California, at the San Diego Convention Center. More than 440 exhibitors will come together this year (even more than last year!) to showcase new technology and participate in technical conference sessions, professional and standards development courses, certification opportunities, and more. Click here for the event schedule, or visit the IPC APEX EXPO 2015 homepage for complete information.

Here are just a few highlights of what you can expect this year:

- 440 exhibitors showing equipment, materials and services for printed boards and electronics manufacturing.
- The largest technical conference in the industry, worldwide. Presenters will be offering new research and innovations from experts in the fields of electronics assembly, test and board inspection, and board fabrication and design.
- Free industry poster sessions.
- Professional development courses that provide comprehensive updates on trending industry concerns.
- Standards development meetings that will help shape the future of our industry.
- IPC International Hand Soldering Grand Championship on the show floor.
- Show floor welcome reception on Tuesday that displays cutting-edge products and services in the New Product Corridor and the IPC Bookstore.
- Networking opportunities including the International Reception, First-Timer's Welcome, IPC Tech Talk, Women in Electronics Networking Meeting, and IPC Government Relations Committee Open Forum, designed to allow attendees to meet colleagues, get updates on key issues and share ideas.

To register to attend IPC APEX EXPO 2015, click here.

Traveling to San Diego and need help? Visit the IPC APEX EXPO travel page for hotel, directions, and airfares (including a United Airlines 5% airfare discount offer).

Be sure to keep an eye on the I-Connect007 site throughout the show for breaking news and event coverage from the show floor. If you're at the show, stop by our booth—#2645—and say hello to the I-Connect007 team, find out how you can become a contributor, or share your thoughts on our content and coverage.

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VT-4A2	2.2W/m.K.	✔			
VT-4B1	1.0W/m.K.	✔	✔	✔	✔
VT-4B3	3.0W/m.K.	✔	✔	✔	✔
VT-4B5	4.2W/m.K.	✔	✔	✔	✔
VT-4B7	6.5W/m.K.	✔	✔	✔	✔

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2015 IPC APEX EXPO Show Guide

Opening Keynote Address:
Tuesday, February 24, 2015
8:30–9:30 a.m.

The Xbox Story: Lessons in Strategy, Team Management and Entrepreneurship

Robbie Bach

Former President of Entertainment & Devices at Microsoft, Xbox visionary and civic activist

Chances are you or your kids own an Xbox, or at least have played games on one. But do you know the story behind this groundbreaking game console? The Xbox saga— from garage-shop inception, through numerous crises and challenges, to ultimate business success—is a multi-faceted tale with several compelling story lines. Bach joined Microsoft in 1988 and worked in various marketing and management roles for 22 years. Beginning in 1999, he led the development of the Xbox business, including the launch of the original Xbox and the highly successful follow-up product, Xbox 360. Bach will speak from his experience as the chief Xbox officer, taking the audience "behind the scenes" and sharing the triumph of a strategic process that brought together a disparate group of talented individuals. Bach will explain how this collection of individuals transformed into a powerful team that applied entrepreneurship principles to build a successful consumer business within the larger Microsoft structure.

Day Two Keynote Address:
Wednesday, February 25, 2015
9–10 a.m.

Flying Saucers and Science/ Science was Wrong

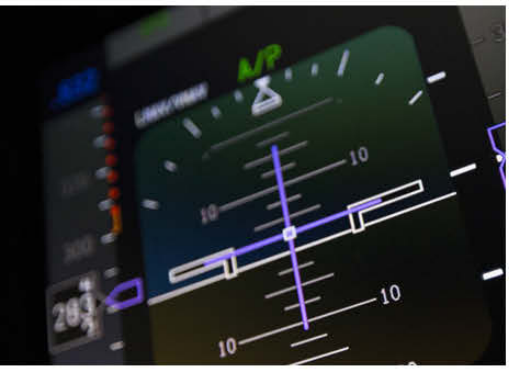
Stanton Friedman

Nuclear Physicist, UFO Researcher

Do you take UFOs seriously? Nuclear physicist and lecturer Stanton T. Friedman does. Friedman will challenge the audience as he draws on more than 40 years of research on UFOs, and his work on a wide variety of classified advanced nuclear and space systems. He will answer a number of physics questions in layman's terms, and establish that travel to nearby stars is within reach without violating the laws of physics. The audience will journey with Friedman to locations in the universe where aliens reside, learn why they've come to Earth and their motives to cover-up their visits. You'll never feel the same about the universe again.

Friedman was a nuclear physicist for 14 years for companies such as GE, GM, Westinghouse, TRW Systems, Aerojet, General Nucleonics and McDonnell Douglas, working in such highly advanced, classified, and eventually canceled programs as nuclear aircraft, fission and fusion rockets and various compact nuclear power plants for space and terrestrial applications.

Since 1967, Friedman has presented at more than 600 colleges and 100 organizations across the 50 U.S. states, 10 Canadian provinces and 18 other countries in addition to various nuclear consulting efforts. He has published more than 90 UFO papers and has appeared on hundreds of radio and TV programs, including three appearances on Larry King (2007 and 2008) and in several documentaries.



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2015 IPC APEX EXPO Show Guide

Free IPC APEX EXPO Buzz Sessions

Find out what's got the industry buzzing at the many complimentary sessions that are designed to keep attendees in the loop. This year's topics include a diversity of great discussions:

- Advanced Fabrication Instruction Exchange Between Design and Manufacturing: IPC-2581B Model
- U.S. Federal Funding Opportunities: Grant Programs and Public-Private Partnerships for R&D and Advanced Manufacturing
- California Chemicals Regulations
- PERM Discusses Pb-free—Are we there yet? (Panel Discussion)
- Electronic Technology Roadmaps
- IPC Worldwide Events 2015–2016
- More!

For a full listing of Buzz Sessions, click here.

EMS and PCB Management Meetings

Designed to help industry members become better leaders, management meetings at IPC APEX EXPO 2015 offer exclusive learning and networking opportunities with senior-level managers and executives of PCB fabricators and their suppliers. The management program meetings address issues related to improving executive decision-making in the industry, focusing on market trends, customer requirements and the economy.

EMS Management Council Meeting—Executive Level

Monday, February 23, 2015
7:15 a.m. (welcome breakfast) to 5:30 p.m.
- For a complete agenda, click here.

PCB Supply Chain Leadership Meeting—Executive Level

Monday, February 23, 2015
7:15 a.m. (welcome breakfast) to 5:30 p.m.
- For a complete agenda, click here.

IPC APEX EXPO 2015 Technical Conference

Recognized worldwide as the most selective in the world, the IPC APEX EXPO 2015 technical conference will present new research and innovations from experts in the areas of board fabrication and design, electronics assembly and test. Course moderators are carefully selected from within the electronics industry community.

Sign up for one day, the full conference or an All-Access Pass. Click here for complete registration information and forms.

2015 IPC APEX EXPO Show Guide

Professional Development Courses

Sunday and Monday, February 22–23
Thursday, February 26

Learn about the latest in design, lead-free technologies, materials, process improvement, solder joint reliability and more at IPC APEX EXPO 2015. Choose courses by general topics to help you focus on the sessions that best meet your professional needs. This year's tracks include:

- Assembly processes for lead-free and tin-lead
- Cleaning/coating/contamination
- Design
- Emerging technologies
- PCB fabrication and materials
- Quality, Reliability and Test
- More! Click here for the complete Agenda Planner.

The PCB List—Find out what it's all about in the I-Connect007 booth!

Brought to you by PCB007, The PCB List is the world's most comprehensive online directory of printed circuit manufacturers, anywhere. Buyers, specifiers, designers and others looking for a PCB fabricator benefit from the intuitive navigation, detailed search capability, and global reach of The PCB List. With a Showcase listing, a PCB fabricator can create a neat, organized presentation that puts all pertinent information at a potential customer's fingertips.

Drop by the I-Connect007 booth to see for yourself how easy it is to find a fabricator, or create a Showcase listing!

Real Time with...

This year, I-Connect007 and the Real Time with…program return to sunny San Diego to bring our readers video coverage of IPC APEX EXPO 2015. Expect to see our team of editors, guest editors, and videographers roaming the show floor throughout the event, to capture one-on-one interviews with the industry's top technologists, engineers, and business leaders—as the action happens!

Visit Real Time with... during the show for updated information about IPC APEX EXPO 2015.

2015 IPC APEX EXPO Show Guide

Technical Education with a Design Focus

IPC has renewed its emphasis on design education, recognizing the critical role it plays in product reliability – see our lineup of courses at APEX EXPO and the revitalization of our Designer Certification program.

A commitment to professional development makes a big difference to your customers, suppliers and colleagues. Make the most of your time and training budget with just one trip.

Engineering staff and managers in design, sales, purchasing and quality teams will benefit:

- **Design Forum —** A full-day educational program featuring design thought leaders
- **Professional Development courses —** Three-hour classes led by subject-matter experts
- **Designer Certification Program —** CID and CID+ class and exam sessions
- **Exhibition —** The show floor is an educational experience in itself: 400+ exhibitors offer additional technical information

The Design Forum

Monday, February 23
7:30 am – 1:30 pm

7:30 am:
Networking Breakfast

8:00 am:
Keynote: Design for Success
Carl Schattke, PCB Design Engineer, Tesla Motors, Inc.

IPC-7070 Component Mounting issues and Recommendations
Rainer Taube, Master Trainer, Taube Electronic GmbH and FED – Germany

IPC-7351C Requirements for Surface Mount Design and Land Pattern Standard
Tom Hausherr, CID+ President, PCB Libraries, Inc.

12:00–1:30 pm:
Luncheon

2:00-5:00 pm:
Professional Development Courses with Focus on Design

Successful Communication with Cross-cultural Teams
Stephen V. Chavez, CID+, Engineering Associate, PCB Designer, Electronic Systems Center, UTC Aerospace Systems

Success Through Control of Cost and Quality
Rick Hartley, CID, Hartley Enterprises and retired Principal Engineer, L-3 Communications

TOP TEN

News Highlights from PCBDesign007 this Month

1 DesignCon Names Best in Design & Test Awards Winners

DesignCon posted the 2015 winners of the Best in Design & Test Awards. Mentor Graphics won in two categories: Xpedition Package Integrator won for Interconnect Technologies & Components, and Xpedition Enterprise took home a prize for Board & System Design & Simulation.

2 EMA and Arena Solutions Form Strategic Alliance

EMA Design Automation and Arena Solutions, the pioneer of cloud-based PLM applications, have formed a strategic alliance combining Arena PLM with EMA's data management solution for Cadence OrCAD to improve the overall user experience. The OrCAD and Arena integration provides a number of benefits for organizations using both systems.

3 IPC-2231: The Cookbook for Design Excellence

IPC-2231, Design for Excellence Guideline during the Product Lifecycle, provides guidelines for establishing a best practice methodology for developing a formal DFX, specifically for layout of printed board assemblies. Think of it as a cookbook for DFX, where you can skim the design recipes you know, or dive into ones that you need more details on.

4 UcamX: A New Paradigm in CAM Software

Ucamco has released UcamX, its ground-breaking all-in-one CAM software suite for the rigid, flex and HDI PCB manufacturing industries. UcamX takes all that's great about Ucamco's leading Ucam line of software and takes it to the next level with a series of new developments and improvements that set the new paradigm in CAM software.

5 Altium, Valydate Enter Strategic Partnership

ValydateVERA has effectively streamlined this entire process. With VERA's integration in Altium Designer, PCB designers can now automatically inspect their schematics against a pre-defined checklist that takes advantage of an intelligent component library that automatically checks for thousands of error violations in schematic designs.

6 ANSYS 16.0 Expands Design Capabilities

ANSYS 16.0 delivers major advancements across the company's entire portfolio, including structures, fluids, electronics and systems engineering solutions—providing engineers with the ability to validate complete virtual prototypes.

7 Mentor Unveils HyperLynx Alliance

Co-developed with industry vendors, the HyperLynx Alliance virtual labs include the complete HyperLynx design environment, partner IBIS-AMI and/or S-parameter electrical models, a reference design based test case, and a step-by-step instruction guide.

8 Cadence Expands Sigrity 2015 Technology Portfolio

Cadence Design Systems has announced an expanded Cadence Sigrity technology portfolio with the Sigrity Parallel Computing 4-pack and the Sigrity System Explorer, an updated power-aware system signal integrity (SI) feature, as well as flexible purchasing options for PCB and IC package design and analysis. The Sigrity technology portfolio enables product creation efficiency by increasing signoff-level PCB extraction accuracy.

9 Zuken Expands CADSTAR Reseller Network in Russia

Zuken has expanded its CADSTAR reseller network in Russia with the addition of Point. CADSTAR is Zuken's desktop PCB design software for companies of all sizes, from individual designers to small and mid-sized design teams and corporations operating across multiple sites.

10 PCB Drives EDA Industry's Revenue Growth in Q3

The EDA Consortium (EDAC) Market Statistics Service (MSS) announced that EDA industry revenue increased 5.7% for Q3 2014 to $1.8 billion, compared to $1.7 billion in Q3 2013. PCB & MCM revenue led the way, with revenue of $167.4 million for Q3 2014, an increase of 9.7% compared to Q3 2013. The four-quarters moving average for PCB & MCM increased 11.4%.

events

For the IPC Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For a complete listing, check out *The PCB Design Magazine's* event calendar.

Energy Innovation Summit
February 9–11, 2015
Washington D.C., USA

MD&M West
February 10–12, 2015
Anaheim, California, USA

2015 Flex Conference
February 23–26, 2015
Monterey, California, USA

IPC APEX EXPO 2015
February 22–26, 2015
San Diego, California, USA

FPD China 2015
March 17–19, 2015
Shanghai, China

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ADVERTISER INDEX

Coming Soon to *The PCB Design Magazine:*

March:
Design for Manufacturing (DFM)

April:
Surface Finishes

May:
Controlled Impedance