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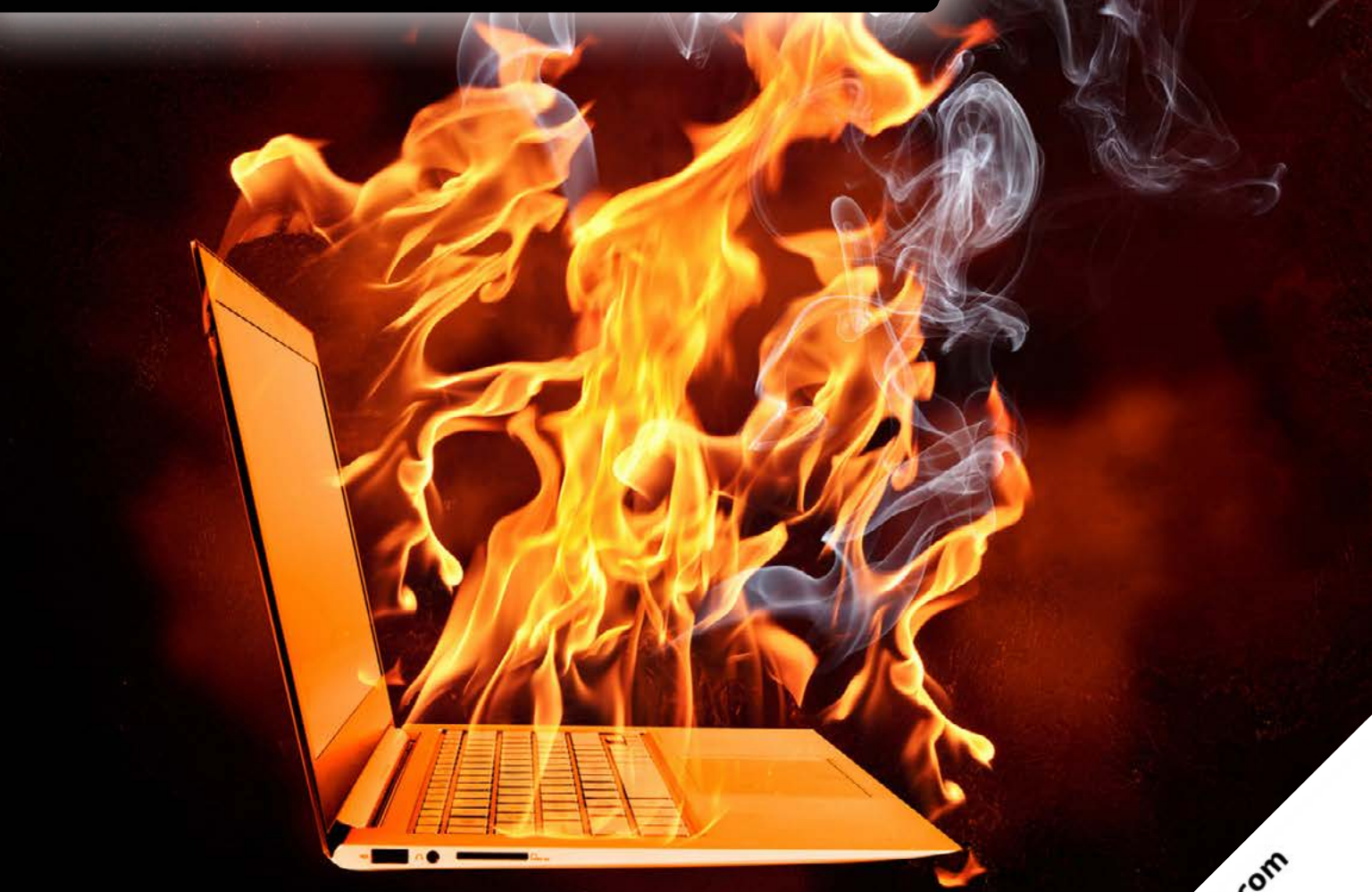
Materials



Thermally Conductive Substrates & Thermal Management

by Ian Mayoh — Page 12

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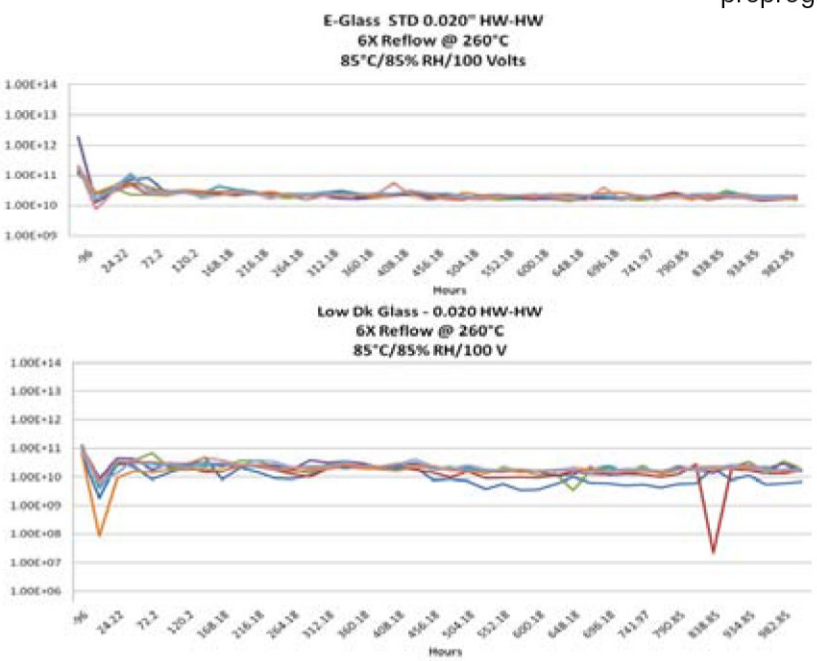

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Electric Cars Are the Future

by Ray Rasmussen
I-CONNECT007

Although I'm an environmentalist at heart (where would we be without the Clean Water and Clean Air acts?), this article isn't driven by that bent. I don't have solar panels powering my house because it doesn't make financial sense, and I won't buy an electric car until it does, either. I guess I'm a practical environmentalist. But the adoption of electric cars as the main source of personal transportation, worldwide, is a done deal and it's coming, fast.

Of course, I'm no expert, but when you see just about every car manufacturer on the planet introducing or developing electric cars, you have to believe they see the writing on the wall. From what I've read, there will be seven new electric cars (in addition to the 14 on the market in the U.S. today) entering the market in 2014 and lots more in 2015. Many of these will be pure electrics, not hybrids. For me, the tipping point is a 200-mile battery range. I don't mind paying more, initially, for an electric car since I'll be saving about $3 for every gas-equivalent gallon of electricity I buy, adding up to thousands in savings each year, but I've got to have more range.

But think of this: As the cost of these cars comes down, and as the cost of gas continues to rise, buying an electric car will basically be free, with the difference in the cost of fuel offsetting the monthly payment. That's when the market's going to explode. When the monthly cost of owning an electric vehicle, including electricity, is less than what it costs to fuel a gas powered car, people will be lining up to buy them. You'll see it in Europe, first, where gas is about $8 per gallon. Electrics will be an easy decision once the range issue is settled. And if you're paying attention at all, you've certainly noticed the billions of dollars flowing into battery R&D. Most major car companies see a 200-mile range battery for an average priced car hitting the market in the next few years. Tesla already does this if you're willing to pay $70k.

Another game-changer is that these cars perform better than their internal combustion engine (ICE) cousins. You get a lower cost for fuel, a safer vehicle for your family to ride around in, lower maintenance costs, higher reliability and a more powerful and better driving experience. That's why it's a game-changer.

Why fight it? The only thing holding back electric cars are the batteries' cost and range. That's it. Everything else is vastly superior to cars powered by ICEs.

Rimac's concept electric "supercar."

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Pundits of ICE-powered cars tout the improving efficiency as proof that there's a lot of life left in this 150-year-old technology. I disagree. ICEs are too complicated and costly (environmentally and geopolitically). By comparison, they're slow, noisy and smelly.

Here's what convinced me: I recently changed the spark plugs and spark plug wires on my 2005 Chevy Malibu, which had 100,000 miles on it. Three cylinders were upfront (really easy to get to) and three were up against the firewall with little room to get to the plugs. I got the job done, but it was a bear. Of course, shortly thereafter an engine warning light came on and after some Google searches I determined that I had to change the thermostat, which I did after draining all the radiator fluid. I had to dispose of the old fluid, buy more and refill the radiator. Sometime later, another warning light suggested I was low on oil. I guess my car was showing its age by requiring more oil than usual. In the past, I hadn't had to add any oil between oil changes. Then, another warning light indicated (after more Google searches) I needed a new gas cap since my original factory cap was causing the fuel system to lose pressure. That's when I knew the gasoline-powered car was finished. The ever-increasing complexity required by ICEs to meet the stringent government efficiency standards makes the ICEs a losing proposition. They can't compete.

Electric cars don't need oil; they don't need to be cooled and therefore have no radiators. They don't have a gas tank (a bomb, literally), either. Electric motors have worked reliably by the millions, day in and day out for years without any, or very little, maintenance. Electric cars are very powerful and will shame any ICE comparable car off the line. You see it more and more at local drag strips as electrics take on ICE muscle cars, crushing them in head-to-head duels. Global refueling stations (a plug) are already in place in every commercial building and in just about every home on the planet. Oh, and,

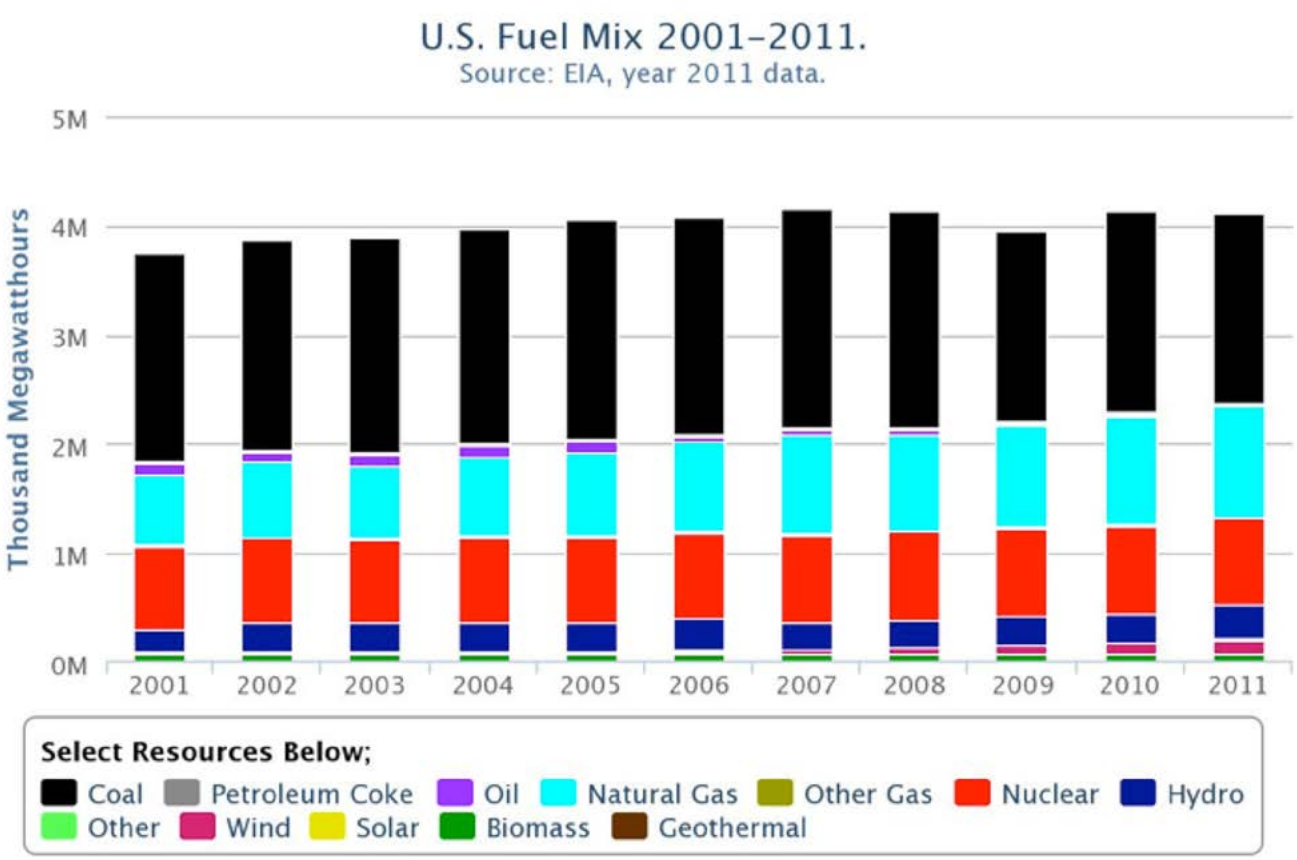

Figure 1.

they don't pollute, directly. Their sources do, mostly coal and natural gas, but the rest don't unless you consider nuclear and its very long term, long life to be pollution. But an electric car powered by mostly wind, hydro or solar doesn't pollute, and it doesn't contribute to the U.S.'s need to keep petroleum supply lines open in the Middle East. It actually does contribute to the stability of the long-term U.S. energy picture. It's a beautiful thing.

What does this mean to us in the PCB and EMS industries? Not too much since more and more electronics have been added to ICE power trains over the years. Instead of ICE controllers and sensors, electronics in electrics will control and monitor AC motors, the transmissions and the batteries. The brake controllers will be a bit more sophisticated because of the regenerative braking. Electronics for safety and entertainment will likely progress along the same path as ICE electronics. Adding solar into the roofs of electric cars, which Ford just announced it will be doing, will contribute a bit more electronics, as well. I think we just need to be aware of what's coming. Will companies like Tesla emerge as major automakers in the coming years? One company already in prime position with Tesla is Viasystems, which makes all of the PCBs, assemblies and battery buss bars for Tesla's cars.

What about Fisker and BYD? Warren Buffet made a large investment in BYD a few years ago. They plan a bunch of new electrics in the coming years. Fisker is building a high-end Tesla-like car. For our industry, it's more about the winners and losers. When the industry shifts to electrics, who will be left standing, and are they on your customer list?

Check out this concept car from Rimac. They're calling it a "supercar."

What we also see happening, as batteries improve, is a move away from gas-powered tools. Laptop batteries did a lot to advance this market. There are entire companies now building lines of outdoor power tools to replace gas-powered lawnmowers, trimmers, blowers, etc., and you'll see more and more electric motorcycles and bikes hitting the streets. They're working on electrics for planes (manned and unmanned). They're a lot quieter and more reliable. Dyson, the vacuum cleaner maker, believes that their new battery-powered vacuum cleaner, the DC59, could potentially replace corded vacuums—it cleans that well. All these products need electronic controls. That's where we come in.

There is another major impact of the electric car, which isn't being discussed too much: its impact on the fossil fuel industry. Combined with solar, the predictions are that within the next 10 to 15 years, many utilities will be out of the power generation business. That's the prediction in a new book from Stanford University lecturer Tony Seba. As the cost of solar drops, solar electricity will continue to be integrated into the energy mix. As consumers and businesses alike choose to lower their energy costs by installing solar panels, there will be a continual decline in the need for utilities to provide energy, relegating them to maintaining the grid as opposed to providing energy. Electric cars accelerate the consumer's move to residential solar systems since they help justify the system costs by offsetting the high price of gasoline. It's an interesting transition and we get a front-row seat in watching this transition from fossil fuels to an all-electric economy based on renewable energy.

Conclusion

Electric cars don't just offer an alternative form of fuel like diesel or hydrogen; the technology is *disruptive*. The dramatic reduction in fuel costs, the way the fuel (energy) is distributed and the simplification of the entire power-drivetrain is a game-changer. That's why, once we get the batteries in place, the shift will happen almost overnight. Buying an electric car, for most, will be a no-brainer and in many cases "free." We certainly live in exciting times!

That's the way I see it. **PCB**

Ray Rasmussen is the publisher and chief editor for I-Connect007 Publications. He has worked in the industry since 1978 and is the former publisher and chief editor of *CircuiTree Magazine.* To read past columns, or to contact Rasmussen, click here.

Thermally Conductive Substrates & Thermal Management

by Ian Mayoh
VENTEC EUROPE LIMITED

Continued and growing interest in cost-effective thermal management of electronic devices and substrates, at component level, continues to drive the development of thermally conductive printed circuits as a solution of choice.

Insulated metal substrates (IMS) or metal core printed circuit boards, shortened to MCPCB, or thermal management boards, are printed circuit boards built with a base metal core used to disperse heat through the components of the board, effectively lowering the core temperature of high heat applications. They are used when conventional heat-sink/fan-cooling techniques are insufficient for cooling the entire system or there are size/cost constraints.

It is the intention here to review the current status of thermally conductive printed circuit substrate options, in terms of performance, construction and processing, and future developments. With particular reference to insulated metal cored substrates, the paper will explore the mechanical, thermal performance and cost considerations to be taken into account when selecting an appropriate IMS material for a particular application, questions will be raised in terms of suitability for purpose and reliability considerations.

Firstly, consider the current trends that continue to be the driving force for more effective thermal management:

- Miniaturization of MLB
- Thermal performance
- HDI
- Embedded technology, within MLB
- Flex and formable circuits
- Light-emitting diodes (LEDs)

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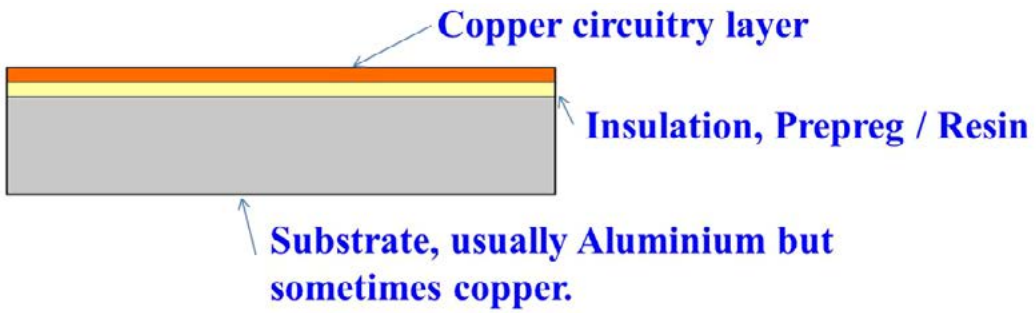

Figure 1: IMS construction.

The need to dissipate heat from electronic modules and assemblies has, over the years, become increasingly important; this is not only as a consequence of the inevitable "smaller, faster, cheaper" trend for microelectronics to operate at higher frequencies and higher-performance levels. In the field of automotive engineering, an increasing number of functions, previously accomplished mechanically, are now solved electronically: braking and power steering are two examples. Elsewhere in power electronics, thermal management becomes a critical consideration in the design of DC power supplies, inverters, power controllers and motor drivers. But it is the global and exponential growth in general, and automotive, LED lighting technologies that is creating huge market demand for efficient, reliable, low-cost thermal management, IMS solutions.

Keeping heat generating components (LEDs/embedded components) cooler—increases component life, which in turn increases product life and long term reliability. The move to increased usage of IMS is primarily driven by the need to reduce system costs through, in the main, reduction in size of or elimination of costly, and bulky cooling fans and heat-sinks.

LED key applications:

- Back light units, typically
- Notebooks and desktop computers
- High-end televisions
- High-end monitors for medical and industrial uses
- General lighting
- Street safety
- Automotive

Recent advances in high-brightness (HB) LED technology have alleviated concerns about excessive costs and have led to an increasing number of local authorities across the world installing eco-friendly LED lighting, and its adoption in domestic, industrial and automotive applications is rapidly, and exponentially, accelerating.

Putting things into perspective, a standard FR-4 laminate has a thermal conductivity coefficient of around 0.25W/mK, thermally conductive prepregs, laminates and insulated metal substrates offer thermal conductivity coefficients of up to 8W/mK, and development continues.

Global regulation is becoming more stringent, fuelling the increasing demand and penetration of more energy efficient lighting, and with a global energy gap looming, is this a surprise?

Earlier estimates suggested that LED technology would capture over 46% of the Global lighting market by 2020, more recent estimates suggest that this will exceed 70%, this alone provides a huge market potential for thermally conductive printed circuits.

Considering LEDs: Good thermal management is required to achieve a bright light, whilst maintaining the colour spectrum, without overheating the junction or the LED unit itself. The life expectancy of an LED is closely related to operating temperature. For example 10°C reductions in temperature will approximately double the life expectancy of the LED.

How to disperse the heat? Conduction, convection or radiation cooling? Probably the most efficient mode of heat transfer is conduction through the substrate. Many power-electronics

and under-bonnet automotive devices are built using direct bonded copper (DBC) substrates on ceramics with good thermal conductivity, particularly materials such as beryllia, silicon nitride or aluminium nitride, which are significantly better heat conductors than alumina, although at a significantly higher cost.

Other areas seeing a significant increase in the use of IMS are power conversion systems (telecom, industrial, high voltage regulator, power supplies) and hybrid/electric motor control applications. These sectors typically use a more complex constructions of IMS printed circuits. Heavy copper weights for high current low voltage applications are used, and the engineering flexibility offered by IMS lends itself readily to this sector. The metal substrate can be of varying thicknesses with complex engineering requirements that may need milling, shaping, threading or even anodizing.

Four Main LED Substrate Types

1. Metal cored PCBs/IMS—insulated metal substrates
2. Conventional PCB—mid- and high-T_g FR-4
3. DBC—direct bonded copper
4. LTCC—low temperature co-fired ceramic (LTCC)

LED manufacturers have been adopting packaging technologies from the power-electronics field with the result that they can offer efficient thermal coupling from the semiconductor to the interconnecting substrate the device is mounted upon. However, although common printed circuit materials have good electrical insulation properties, they generally provide excellent thermal insulation as well. Heat dissipation has traditionally been promoted by the incorporation of internal or external heat sinks and fans: Heavy copper inner layers with thermal via holes, or bonded aluminium heat ladders—all of which work, but potentially add significant cost in terms of materials and processability.

The family of thermally conductive printed circuit laminates, known as IMS, have now become widely established as a preferred base material for the manufacture of circuits for HB-LED applications, and offer cost-effective performance with straightforward fabrication, good mechanical stability and a range of thermal conductivities to suit particular configurations.

Whilst other materials are available, in terms of thermal conductivity, there remain significant challenges in terms of processability, cost and material robustness.

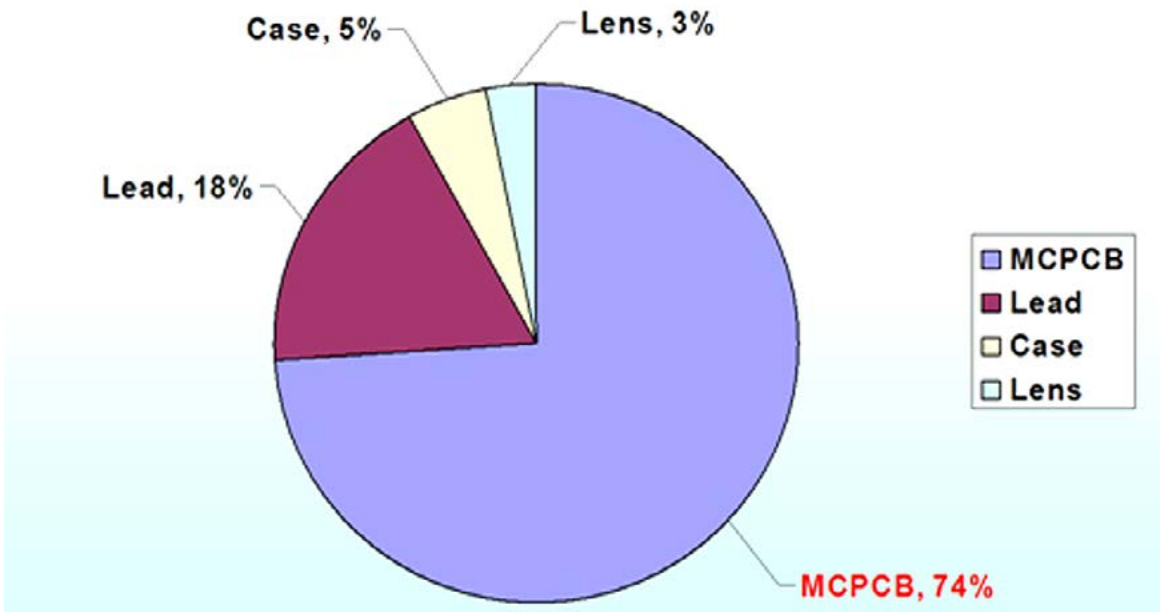

Figure 2: Thermal dissipation of a typical LED build.

LEDs, like all light sources, are not 100% efficient—they generate heat. This heat causes the LED chip's temperature to rise. As the temperature rises, it can reach a point where the light conversion efficiency actually decreases as the input power is increased. Also, as the temperature rises, the long-term life of the LED decreases: the brightness of the light permanently drops.

The heat generated by an LED is quite different from the heat generated by a regular incandescent bulb. Because the LED heat is trapped in the chip, heat must be conducted out via a path of low heat resistance. This keeps the LED at a temperature where it will function efficiently and have a lifetime that maps to the life of the application. It is necessary to remove the heat, not only from the LED chip, but also from the LED light platform, by conducting it into a heat sink. The heat sink could be the light fixture itself. The best conductor of heat is metal, so heat sinking the LED light to a large metal object delivers optimal heat conduction, which is where IMS or MCPCBs step in.

Conversely, incandescent bulbs radiate most of their heat into the surrounding air, which assists significantly in cooling the bulb. Unlike LEDs, incandescent bulbs do not conduct substantial heat into the Edison socket, which stays relatively cool.

IMS materials generally consist of a thermally conductive dielectric layer, heavily loaded with ceramic type fillers, sandwiched between a copper foil and an aluminium plate, the dielectric may be unreinforced, or woven-glass reinforced. Due to its superior mechanical properties, aluminium remains the most preferred backing substrate however; alternatives include copper and steel plate.

The choice of filler is always a balance between thermal conductivity, cost and electrical insulation properties. You can see from the

Filler Type	Thermal Conductivity (W/m*K)	Breakdown Voltage (Based on 70%Filler)
Al_2O_3	25~40	+ +
MgO	25~50	+
SiO_2	9.6	+
Si_3N_4	50	-
BeO	270	-
SiC	25~100	- -
AlN	120~220	+
BN	100~250	+

Table 1: Effect of filler on thermal conductivity and breakdown voltage.
(Key: ++ Better + Good - Bad - - Worse)

above chart that aluminium nitride and boron nitride give the best thermal conductivity with good breakdown voltage, alumina gives a higher breakdown voltage but with lower thermal conductivity, the filler blend needs to be carefully selected bearing in mind ultimate performance requirements balanced against long term reliability.

Traditional PCB substrates are designed to have good electrical insulation, but due to the glass component they also tend to be good thermal insulators as well.

The increased thermal conductivity, of conventional glass style prepregs is achieved by loading the resin with thermally conductive ceramic fillers. These materials can be used to build multilayer PCB structures which can then be bonded to a heat-dissipating base using thermally conductive prepregs.

Insulated metal substrates are commercially available, and they offer cost effective performance with straightforward fabrication, good mechanical stability and a range of thermal conductivities to suit particular configurations. IMS are not a new concept, these materials have been available since the 1960s, but only recently has the volume demand driven the development of new and improved versions and warrantied volume production.

Functions of the dielectric layer:

- Thermal conduction
- Electrical insulation
- Promote adhesion—bonding to copper and aluminium
- Choice of woven-glass reinforced or non-reinforced dielectric

The dielectric serves a number of functions, including, thermal conduction, insulation and promoting good bonding. Generally the dielectric is a laminating resin, loaded with thermal conductive ceramic filler, designed to give a good bond to the copper foil, the base laminate and to the metal substrate, if it is a pure IMS. It may be glass-reinforced or unreinforced.

Conventional FR-4 glass reinforced dielectrics create a thermally resistive, as well as an electrically resistive barrier. At this stage thermally conductive glass reinforced dielectrics currently allow in excess of 12x more heat transfer than standard FR4, the use of non-reinforced dielectrics is significantly increasing this figure to, currently, in excess of 25x and still developing

As can be seen above, the choice between reinforced and un-reinforced dielectric is a trade-off, glass reinforced material offer a marginally better thickness uniformity and higher breakdown voltage (obviously the two are linked), and the cost is lower. The trade-off is that the ultimate thermal conductivity of the glass-reinforced material is less (because there's not as much room in the cross-section to accommodate the required thermally-conductive filler and glass is a thermal as well electrical in-

Item	Reinforcement	Un-reinforcement (Unsupported)
Breakdown Voltage	+++	++
Cost	++	+
Thickness Evenness	++	++
Thermal Conductivity	+	++
Bendability	--	++

Table 2: Comparison of woven-glass reinforced and non-reinforced IMS.

sulator). But that's not necessarily a disadvantage. It's all about applications engineering and choosing the most appropriate material for the job.

For a given application, the choice of dielectric is determined by the need to achieve a balance between thermal conductivity, dielectric strength, reliability and of course unit cost. In general, the reinforced dielectrics have lower thermal conductivity, but higher breakdown voltage and slightly better thickness uniformity. The cost, of glass reinforced dielectrics, is generally lower than the non-reinforced grades, which demand extremely critical manufacturing control to ensure uniformity of filler dispersion and the absence of traces of particulate foreign material which could lead to premature dielectric breakdown. Also, due to thickness distribution considerations, most manufacturers can only laminate non-reinforced materials in small panel sizes—increasing unit cost and potentially limiting applications.

Typical characteristics of IMS laminates are: Aluminium from 0.5 mm to 3.0 mm thick, available in different grades to suit mechanical requirements, copper from 18 um to 410 um , and dielectric thickness from <50 µm to 150 µm. Printed circuit fabrication is by conventional print-and-etch techniques. The aluminium is protected during etching by a peelable film. Single-layer technology is suitable for most applications, but multilayer constructions are feasible by sequential lamination using thermally conductive prepregs and thin laminates constructed from thermally conductive prepregs.

Watt per Metre-Kelvin (W/mK)

The commonly quoted unit of thermal conductivity. Definition: a measure of the ability of a substance to conduct heat, determined by the rate of heat flow normally through an area in the substance divided by the area and by minus the component of the temperature gradient in the direction of flow: measured in watts per metre per Kelvin. Symbol λ, ***k*** sometimes shortened to just conductivity, is also known as the coefficient of heat conductivity. Because it's a coefficient, it needs to be considered in conjunction with thickness. The reciprocal is, ther-

Dielectric Thickness	Thermal Conductivity 1.6W/mK	Thermal Conductivity 2.2W/mK	Thermal Conductivity 3.0W/mK	Thermal Conductivity 5.0W/mK	Thermal Conductivity 6.5W/mK
50um	-	-	0.026 (0.160)	0.018 (0.110)	-
75um	0.074 (0.462)	0.054 (0.337)	0.040 (0.250)	0.029 (0.180)	0.019 (0.111)
100um	0.099 (0.618)	0.072 (0.450)	0.053 (0.331)	0.038 (0.240)	0.024 (0.150)
125um	0.123 (0.768)	0.089 (0.556)	-	-	-
150um	0.148 (0.925)	0.107 (0.668)	-	-	-

Table 3: Variation of thermal impedance (°C.in²/W) with dielectric thickness, for different W/mK values of thermal conductivity. To reduce the thermal impedance by half, double the thermal conductivity or halve the thickness of the dielectric.

mal impedance is proportional to the ratio of thickness to CTE, and is probably a more practical parameter.

So, rather than just demand a high W/mK value, consider whether a lower W/mK at a lower dielectric thickness will give the same thermal impedance, at lower cost, provided that the dielectric strength is sufficient, and it's really only at high operating voltages that this becomes a serious consideration. So for most LED, and low voltage applications, the lower W/mK materials are perfectly adequate.

Halve Dielectric Thickness, Halve Thermal Impedance

As discussed above, thermal conductivity is only part of the equation … halving the dielectric thickness will in turn halve the thermal impedance and so in effect double the thermal capacity, but this also brings challenges:

- Thickness control of the dielectric
- Risk of dielectric breakdown and hi-pot failure
- Stability

We are now producing commercial quantities of IMS materials with a dielectric thickness of 50 µm and below, but this has only been possible following a lengthy investment program, including, but not limited to:

- Proprietary treaters and coaters
- The introduction of ultra purity fillers
- Introduction of super fine filters
- Proprietary modifications to the resin supply lines

With the above modifications we are now able to produce, in commercial quantities thin cores down to 35 µm guaranteed against hi-pot failure.

IMS materials are currently available with thermal conductivity values from approximately 1.0 watt per metre Kelvin (W/mK) suitable for low-power LED applications, and up to about 8W/mK for power electronics. For reference, copper is 380W/mK, aluminium 200W/mK and FR-4 laminate around 0.4W/mK. It is important to systematically evaluate and characterise an IMS material for a particular application, rather than rely on data-sheet information, which may overstate certain critical parameters or, at the very least, be difficult to use comparatively due to a variety of different test methods being used to generate critical datasheet values, such as thermal conductivity and electrical breakdown strength.

Insulated metal substrates are generally compatible with lead-free soldering processes, although construction has a considerable influence on reliability, the resin chemistry determines characteristics, such as T_g (glass transition temperature) and T_d (decomposition temperature), which, likewise, affect reliability under thermal stress and thermal shock conditions.

In typical LED street lighting applications, the main reliability issue for insulated metal substrates is not dielectric breakdown, since operating voltages are relatively low, but the effect of shear stress resulting from CTE differences between copper, dielectric and aluminium during the severe thermal cycling between power-on and power-off, together with day-night and seasonal ambient temperature and humidity variation.

Some key points to consider in selecting dielectric type and thickness for IMS:

- Understand the thermal, electrical and mechanical performance requirements of the design
  – performance/reliability/cost trade off
- Thermal Conductivity of the Dielectric
  – Lower thermal conductivity—thinner dielectric required?
  – Higher thermal conductivity—thicker dielectric possible?
- Copper Thickness
  – Heavy coppers have a larger treatment profile
  – Consider the peak-to-peak dielectric separation between copper treatment and the treated surface of the aluminium/copper/steel backing
    – this directly influences electrical breakdown performance & reliability:

<=105 µm copper—75–100 µm dielectric
>=140 µm copper—100–150 µm dielectric

Item	Unit	Reinforced Dielectric (100um)	Unsupported Dielectric (50um)	PI Film (20um)	Ceramic Substrate (AIN)
Thermal Conductivity	W/m-K	Limit ~3.0	5.0	0.8	170
Thermal Impedance	°C*in²/W	0.08	<0.018	0.06	0.001
Breakdown Voltage	VDC	4000	2000	2000	5000
Water Absorption	%	0.5~0.8	0.8~1.0	1.0~1.5	0.08
Tg	°C	130	120	230	-
Peel Strength	Kgf/cm	1.6~2.0	1.2~1.4	1.0~1.2	
Price	-	Low	medium	Expensive	Very Expensive

Table 4: Dielectric comparison.

If you really need a thinner dielectric with a heavy copper, you can consider the use of RTF foil…but peel strength will be reduced.

Beware of Data Sheet Values and Manufacturers Claims

There is still a tendency for some manufacturers to quote figures based on in-house test methods, even thermal conductivity data is significantly overstated against recognised test methods by some producers.

Until the IMS market matures and a universally accepted set of test methods emerges, inconsistent test methods will result in some anomalies making direct correlation of data sheet values difficult.

Dielectric breakdown and dielectric withstand values—results depend on the design of the test coupon for some commonly used test methods—as a manufacturer we tend to use the well-recognised methods of IPC-TM-650.

Only use data sheet values as a guide, which means:

- Don't rely on the accuracy of figures where the exact test method is not stated.
- don't take the results too literally, even when a recognised test method is stated
- To quote from ASTM D149, Standard Test Method for Dielectric Breakdown Voltage and Dielectric Strength of Solid Electrical Insulating Materials at Commercial Power Frequencies:

Results obtained by this test method can seldom be used directly to determine the dielectric behaviour of a material in an actual application. In most cases it is necessary that these results be evaluated by comparison with results obtained from other functional tests or from tests on other materials, or both, in order to estimate their significance for a particular material.

International standards for production of IMS, and metal backed circuits; part of the problem is that there are no concrete standards at the moment. Committees are in place to develop standard for IMS and conductive substrates, we along with a number of manufacturers and LEADING end users are involved. Until this is resolved, buyer beware!

Over the last few years, there has been a pro-

liferation of IMS manufacturers.

The big issue in the market now is one of long term reliability. There are plenty of low prices for these materials out there, but no one knows how long PCBs made from these low-price materials will function in the field, or at times if they are even true thermally conductive substrates.

Given the investment being put into the switch from traditional to LED lighting, saving a few pennies per PCB could be false economy if they fail in the field. Emphasis, for both the IMS manufacturer and the PCB producer, has to be put on the equation of cost vs. reliability.

Further, given the disparity in in-house test methods and the current lack of international standards as outlined above, as a PCB manufacturer, supplying to an emerging market (LED lighting) with product life expectations in excess of 50000 hours, at a usage of 10 hours a day, for nearly 14 years, you need to be absolutely sure of your material manufacturers credentials.

Put simply, there is no point crying over the cost of product failure or loss of reputation, when to save a few pennies a supplier for IMS has been chosen purely on price!

All professional producers are generally geared to the provision of test and reliability data in line with industry recognised standards and test procedures, where available, from the likes of IPC, ISO, ASTM and UL. Along with the significant investments in product development and manufacturing infrastructure, this means the professional IMS manufacturer will not necessarily be the lowest price, but will invoke the price vs. reliability/reputation analysis and become very competitive in terms of cost.

PCB Fabrication Considerations

Thermal Prepregs ML Lamination

The heavy loading of these materials, with filler, leads to "low-flow" prepreg characteristics therefore there is a need for rapid temperature rise and early application of lamination pressure.

It is possible to encapsulate 2 oz. copper tracks however, heavier copper weights will present some challenges.

Machining

Due to the type and content of filler in IMS, there is a tendency for rapid tool wear.

Undercut, diamond-coated drill bits are preferred; spindle speed will be around 80% of that used for FR-4.

Two-flute end mills give best finish on aluminium, and adjust cutter depth at 50% tool life to compensate for local abrasion by filler.

Lead-Free Soldering and Thermal Cycling

Insulated metal substrates are generally compatible with lead-free soldering processes however; construction has a significant influence on reliability. Woven-glass reinforcement of the dielectric reduces its coefficient of thermal expansion both in the XY plane.

Resin chemistry determines characteristics, such as T_g and T_d, which, likewise, affect reliability under thermal stress and thermal shock conditions.

Surface treatment of aluminium prior to bonding is critical, both to achieve high bond strength and to avoid high-resistance shorts from metallic debris.

Summary

There continues to be increasing interest in cost-effective thermal management of electronic devices and PCBs, and thermally conductive printed circuit substrates, or insulated metal substrates, are becoming the solution of choice

When specifying or pre-selecting materials, think in terms of actual thermal impedance of an IMS material, rather than judge everything on the thermal conductivity figures—watts per metre Kelvin.

Choose your materials to suit the application. And importantly, do your own qualification tests, and don't take data sheet values too literally. **PCB**

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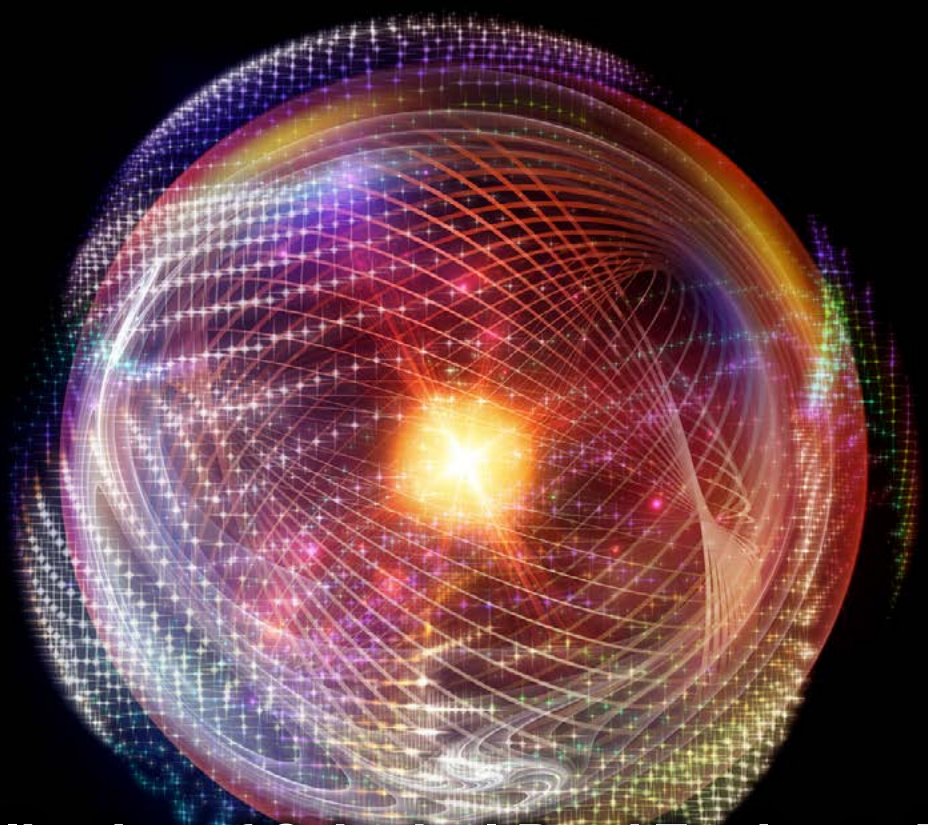

The Application of Spherical Bend Testing to Predict Safe Working Manufacturing Process Strains

by John McMahon, P.Eng
and Brian Gray, P.Eng
CELESTICA (CANADA)

Abstract

The increased temperatures associated with lead-free processes have produced significant challenges for PWB laminates. Newly developed laminates have different curing processes, are commonly filled with ceramic particles or micro-clays, and can have higher T_g values. These changes designed to reduce Z-axis expansion and improve the materials resistance to thermal excursions through primary attach and rework operations have also produced harder resin systems with reduced fracture toughness.

Celestica has undertaken an extensive "Spherical Bend Test" program to assess lead (Pb) free compatible materials and area array packages. This work has confirmed "pad crater/ pad lift" as the dominant failure mode in Pb-free materials in agreement with observations from multiple streams of field returned product. This work discusses the multiple phases of testing and the implications for mechanical reliability of Pb-free product. The initial phase was designed to confirm or refute the established relationship between strain rate and safe working strain in Pb-free materials. The second phase studied the effect of extended thermal excursions for an extensively used standard loss laminate material. The third phase was designed to directly compare standard loss laminate materials and has confirmed the impact of filled resin systems identified by other investigators.

This new work seems to confirm the relationship between board thickness and safe working strain established by in IPC/JEDEC-9704: "Printed Wiring Board Strain Gage Test Publication." Data is only available for a limited number of package designs but these selected packages are believed to generate conservative strain limits for manufacturing process guidelines. The design of the most recent test plan was intended

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to generate data that would allow investigators to generalize the effect of package compliance on the safe working strain of the assembly by correlation of test data from multiple packages to an existing simplified mechanical model.

Assembly processing, test methods and results will be documented in addition to discussion on resultant data, failure analysis, distribution parameters. The effectiveness and predictive range possible from the simplified model will also be discussed.

Introduction

The transition to lead-free assembly is essentially complete for many product sectors. Low thermal mass products designed for sale directly into the consumer market such as handsets, smart phones, gaming systems, PCs and netbooks, are all routinely built with lead-free solder alloys and comply with widely enacted environmental legislation. The vast majority of these products are built with alloys in the tin silver copper (SAC) but there have been some recent introductions of tin copper (SnCu) and tin bismuth (SnBi) alloy systems. There are a wide variety of choices available but the impact of SAC and SnCu alloys is that the minimum solder joint temperature for proper re-melting of solder spheres and powders is in the 230–240°C range. SnBi systems reduce melting temperature significantly but are currently most commonly used in conjunction with alloys of the other two systems to replace wave solder operations. While there have been some ver y extensive field failure issues related to material selection, in general the materials required for robust assemblies in these low warranty time, high replacement rate product categories are now readily available. Proper analysis, material qualification and product design will result in "wear out" failure mechanisms and in-warranty repair rates that are in line with those experienced with eutectic tin lead (SnPb) assembly processes.

Two principal factors are now driving other higher-reliability and higher thermal mass product sectors to Pb-free assembly processes. First, the resolution of the European Union discussions on the "lead in solder" exemption has produced reasonably clear timelines for the Enterprise Computing and Telecommunication (EC&T) sector. There is a wave of these server room and backbone type products that will transition over the next few years. These products are typically designed to the maximum area that can be processed through standard SMT, wave solder and test equipment. Current products typically have 20–30 Cu layers and thicknesses of 0.100–0.130 inches (2.5–3.5 mm) but certainly higher layer counts and thicknesses of 0.25 inches (6 mm) are predicted for these products. These high layer counts are combined with board dimensions which can exceed 16 x 20 inches (40 x 50 cm). The high thermal mass associated with this type of assembly can drive a 5x to 10x increase in the heat energy requirements when compared to consumer products. These increased energy requirements translate into longer thermal profiles and extended exposure times at high temperatures for all processing steps. In addition to thermal considerations these high complexity assemblies have another common feature: Multiple populations of application specific integrated circuits (ASICs) that usually exist as large BGA packages based on built up substrates with metal heat spreaders. The combination of thick laminate structure and large stiff package design almost certainly defines the maximum stress condition and therefore the lower boundary condition for mechanical integrity under flexure in high complexity assembly. Second, EC&T and other sectors with

"The combination of thick laminate structure and large stiff package design almost certainly defines the maximum stress condition and therefore the lower boundary condition for mechanical integrity under flexure in high complexity assembly."

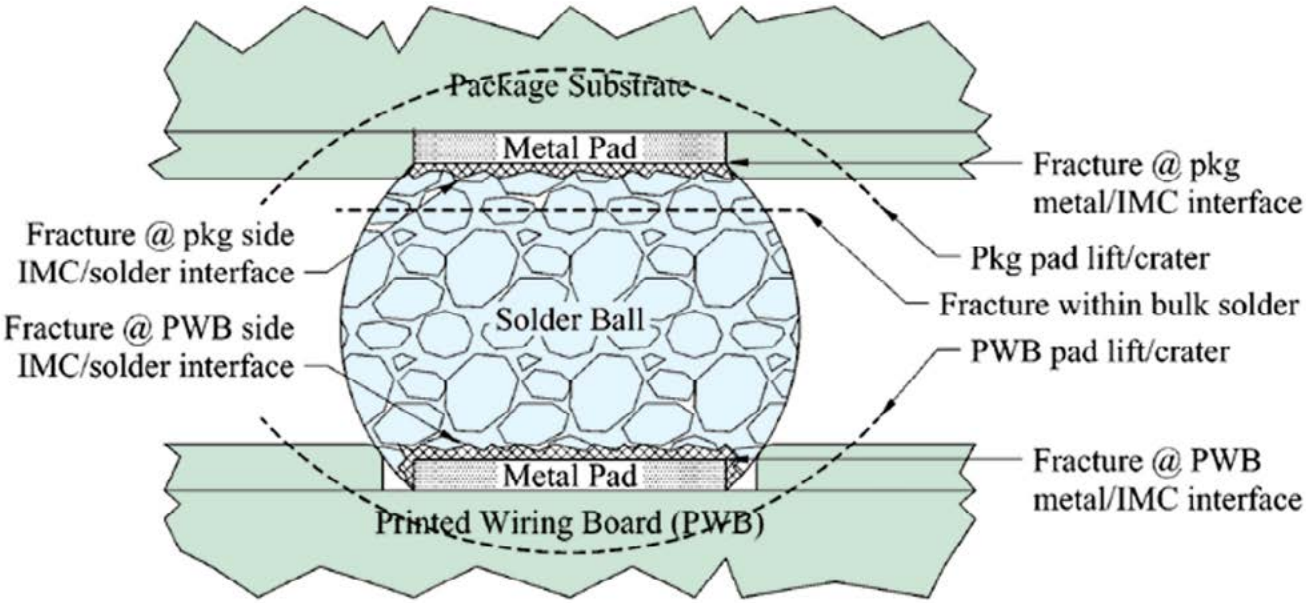

Figure 1: Failure modes in BGA solder joint systems[5].

higher reliability requirements are also being forced to convert as the supply chain, which is primarily driven by the consumer product sector reduces the availability of Pb- bearing components. These high- reliability sectors represent such a small percentage of the total component consumption that producers will over time stop production of all Pb-bearing processes. Compliant lead plating and attached solder spheres will only be available in Pb-free options.

Reliability of Pb-free solders has been a topic of research for over 10 years and there is a plethora of studies on the thermal mechanical degradation of these materials. Less is known about the mechanical robustness of lead-free systems. The work that is available for review is primarily related to drop shock improvements for handheld devices. There have been a variety of new additions to low silver alloys attempting to enhance the energy absorption of these alloys. Very little work has been documented on mechanical failures of larger assemblies, where the fracture toughness of the solder itself does not appear to be the limiting factor. Nadimpalli et al.[1,2] have discussed the substantially lower energy required to initiate cracking in epoxy resin systems than in Pb-free solders. This must be attributed at least in part to the changes that laminate suppliers have implemented over time to reduce the Z-axis expansion and raise thermal decomposition temperatures with the intention of making their materials more robust when subjected to extended solder reflow cycles. Unfortunately these implementations have had a detrimental effect on some mechanical properties of laminates, particularly toughness. Roggerman et al.[3,4] and others have published "cold ball pull" and "hot pin pull" testing results which identify that filled phenolic cured FR-4 epoxy laminate systems fail at lower loads and absorb less energy to failure than unfilled resins from the same group. These micro particle fillers have been introduced to reduce Z-axis expansion and are widely implemented. We believe that this category of resin system represents the limiting case for mechanical integrity.

Mechanical failures in BGA solder joint systems have been categorized into ten modes to simplify industry discussion and acceptance of standardized testing. There is wide industry agreement that Mode 3, failure at the package NiP/SnNi IMC layer was the limiting case when current procedures were designed. There has been some movement in the industry to con-

vert to Cu-Sn based interfaces at the package side and this has reduced the number of maverick lot incidents considerably. This change combined with conversion to lead free processing has produced a new dominant failure mode. Anecdotally mechanical failures in lead-free systems are almost always reported as Mode 10, pad lift/pad crater unless some significant process defect is present in the solder.

This work outlines our efforts to generate working strain guidelines for manufacturing processes that produce equivalent safety factors for Pb-free compatible materials[6] when compared to materials that have been in use for Eutectic tin lead systems. This work will be conducted on test vehicles constructed and processed to be consistent with high complexity assembly.

Spherical Bend Testing

Various flexural test bending modes have been employed in the electronics industry. IPC-9702[4] is based on four-point bend geometry with the package aligned parallel to the bending direction. This mode reduces scatter in the results primarily because individual solder joints are reinforced by near neighbors. IPC-9702 was intended to reduce repetitive package qualification testing by standardizing methods.

The results are easily compared between packages, but they do not represent the limiting condition and therefore are difficult to translate into safe working limits for tool qualifications and process characterizations. Orienting the package at 45 degrees to the bending direction increases the stress in the corner solder joints and provides a more conservative estimate of flexural limit. Hsieh & McAllister[7] have published an excellent comparative study of the various flexural options and identify spherical bend testing as the method that generates the highest tensile stress in the corner solder joint for a given displacement from the as built condition. Celestica has selected the spherical bend test setup which is depicted in Figure 2 for this work for three primary reasons

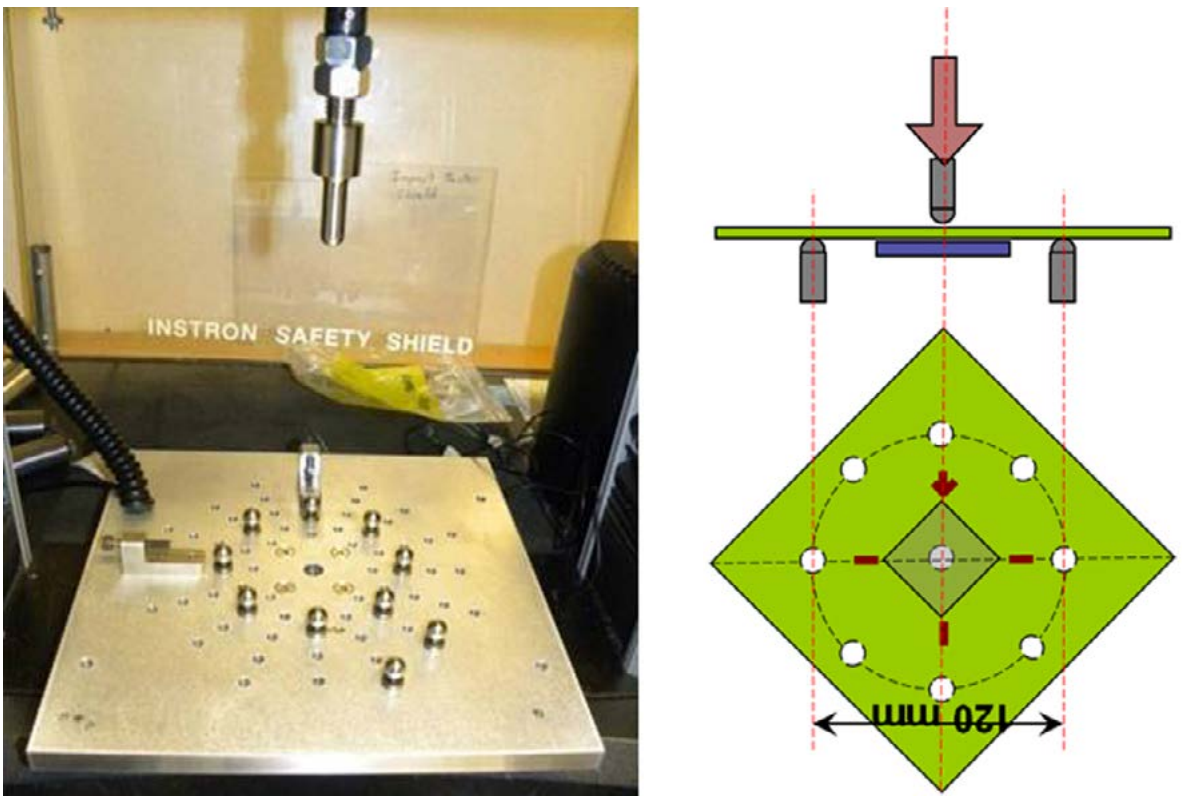

Figure 2: Spherical Bend Test Geometry[11].

out lined in previous work by the authors[8,9,10]. First, it represents the most conservative estimate of deflection limit. Second, it matches the conditions imposed by ICT equipment, which is a standard process step for many products and is a known source for board deflection. Third, it generates data at all four corners of the package because they are loaded equally.

The spherical bend test fixture is based on a support plate with eight spherically ground pins evenly spaced on a circle with a diameter roughly 3x the diagonal dimension of the part. The sample under test is centered on the circle and the load is applied from the back side in the center of the package footprint by another spherically ground pin. The effect is to force the flat assembly into an area segment of a sphere whose radius is inversely related to the displacement of the loading pin. The attached package acts as a stiffener in the center of the slab and stress is imposed in a manner directly related to the diagonal distance from the center of the package. The effect is to load the corner solder joints to failure. In fracture mechanics engineering terms the loading is mixed mode I & II as depicted in Figure 3.

- **Mode I:** A tensile component of the load as the stiffener (package) resists being deformed by flexure imposed on the board. This is a crack opening mode when describing a horizontal crack in the solder joint.
- **Mode II:** An in-plane shear stress component as the package resists being stretched as curvature is imposed on the system.

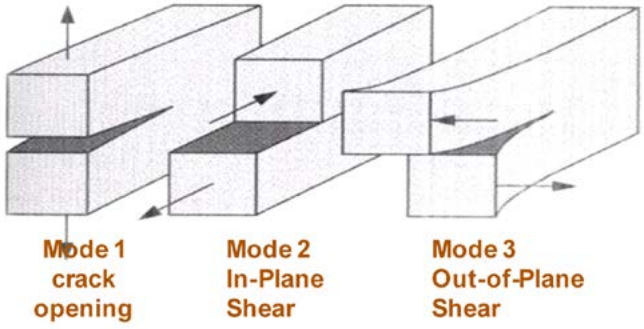

Figure 3: Crack Stress Modes[11].

The principal strain on the board surface may not be coincident with the diagonal of the package but the maximum bending

or minimum bend radius for the board is coincident, therefore the strain gauges are located on the board at the corners of the package in the diagonal orientation. If the assembled test unit is relatively compliant, gauges attached to the package corner in the same orientation also provide information. However the heavy metal heat spreader and its attachment to the package substrate make that information indecipherable for this sample set. Data collection is set up to simultaneously record resistance in the daisy chain, strain in the six gauges attached to the sample, displacement of the test head and the load induced by that displacement. Diagonal strain is recorded in the four aligned gauges and strain rate is calculated from the recorded data. The additional two gauges at a single corner allow calculation of the principal strain and principal strain rate.

Experimental Design: DOE1

The initial experiment was designed to assess the mechanical strain limits for lead-free high-complexity assembly and

characterize the effect of lead-free alloys and extended thermal requirements on safe working limits for board flexure in terms of peak strain and rising strain rate.

Surface strain analysis in PCBAs is the method by which we normalize a whole group of sub-parameters. Surface strain in uniform slabs is a function of deflection or curvature and board thickness (distance from the neutral axi s of the slab). In electronic assembly it is complicated by non-uniform reinforcement of the system by soldered components. Our interest is actually in the stress/strain concentrations that are inherent in the soldered connections. Specifically, the stresses that are imposed on the solder, the interfaces of the solder joint and the resin systems that are directly in contact with the solder pads. In this work we have introduced two factors which are "designed" to generate variation in the results. These are board thickness and strain rate. The other three factors: sphere alloy, laminate and pad plating are under study. The expectation i s that each

Factor	Levels
Sphere alloy	SnPb / SAC105 SAC305 / SAC405
Laminate	Standard Filled Phenolic / Toughened Filled Phenolic
Pad Plating	OSP / ENIG

Table 1: DOE1 Design Variables.

combination of strain rate and board thickness will generate a separate distribution of failures. The experimental design is actually to produce an evaluation of the reduced factor list outlined in Table 1 at each of these six combinations.

The strain rate dependence of fracture in epoxy resin systems is well documented in basic materials research, and has been widely incorporated into existing industry specifications and guidelines, such as IPC/JEDEC-9702—Monotonic Bend Characterization of Board-Level Interconnects[2] and IPC/JEDEC-9704—Printed Wiring Board Strain Gage Test Publication[3]. A proper treatment of this topic is beyond the scope of the current paper, but testing for this experiment was targeted at three specific principal strain rates intended to cover the acceptable ranges of all major assembly processes. Th ose three targeted principal strain rates are 1000, 3500, 7000 micro strain per second (με/s).

Eight sub-lot variations of a mechanical test vehicle were procured. Solderable surfaces were plated in both OSP and ENIG to generate interfaces based on both Cu6Sn5 IMC and Ni4Sn3 IMC systems. The PWBs were obtained in two laminates provided by Isola. A standard filled phenolic cured FR-4 and a non-commercial variant of the first which had been modified to reduce room temperature Young's modulus by approximately 40% in an attempt to toughen the resin system.

Two versions of physical design were generated, each with identical footprints and outlines but with two distinct laminate stacks to represent incremental levels of assembly complexity. The first version was made up of 20 copper layers and had a nominal thickness of 0.100 inches (2.54 mm), the second contained 26 copper layers and had a nominal thickness of 0.130 inches (3.3 mm). The 185 x 185 mm

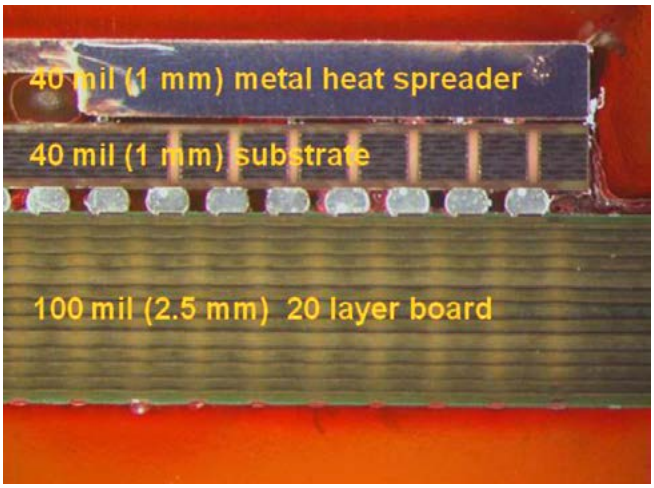

Figure 4: Typical structure—40 mm pkg on 20-layer board.

test vehicles have a single BGA footprint for a 40 x 40 mm – 1.0 mm pitch device. A sectional view of the 0.100 inch version of the test vehicle is presented n Figure 4.

The 40 mm 1517 I/O built up flip chip packages were daisy chain devices provided by LSI. The package substrates were all plated with SAC305 over copper before spheres of the various alloys were attached. The BGA spheres were provided in Sn37Pb, SAC105, SAC305 and SAC405. Assemblies were preconditioned by one pass through the SMT oven prior to BGA attachment to account for the fact that these large devices usually exist on the top side of double sided assemblies. Where forced rework was required assemblies were processed through two further hot gas cycles to simulate removal and replacement of the BGA device. Solder joints from these processes were properly formed with acceptable voiding and typical microstructure.

Two thermal profiles were prepared for the testing program. The SnPb devices were attached with SnPb paste while all of the Pb-free devices were processed with SAC387 paste. The characteristic Pb-free profile is presented in Figure 5. This induces minor modifications to all of the SAC alloys in the final solder joints but it is typical of results generate throughout the industry. Time zero cross sections for all process lots were inspected by optical microscopy.

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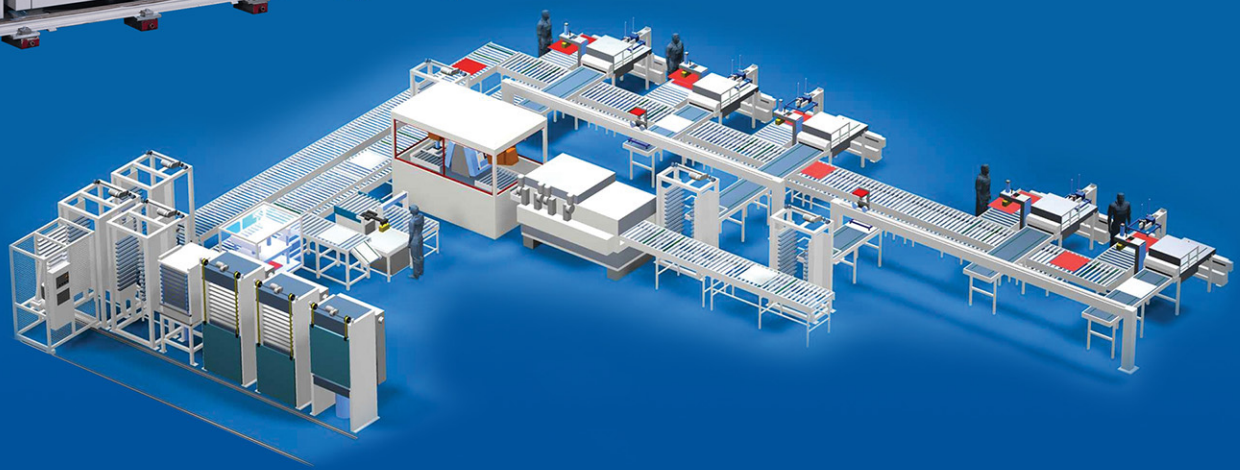

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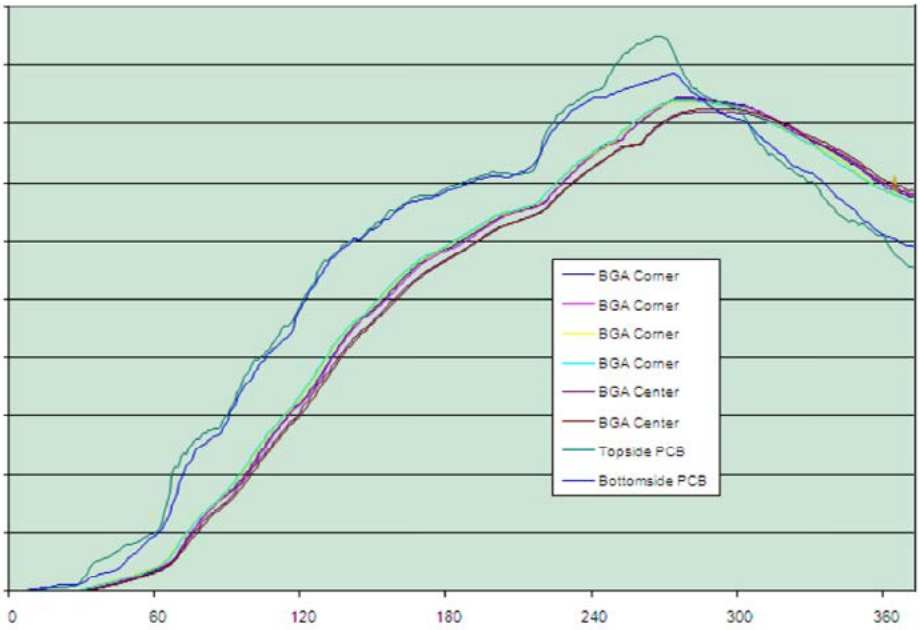

Figure 5: SMT reflow profile: primary attach.

There were no remarkable results from primary attach. Solder conformation was normal, very little voiding was evident and the all of the standard phase compositions were measured. Packages are pre-plated with SAC305 directly over Cu so OSP boards produce Cu6Sn5 interfaces at both top and bottom interfaces. ENIG boards produce Cu6Sn5 at the top interface and a much more complicated Ni3Sn / Ni4Sn3 / (Cu-Ni)4Sn3 interface at the board side pad.

Experimental Design: DOE2

The intent of this experiment was to identify and quantify differences in pad crater resistance and therefore survivable strain

on a typical filled, phenolic cured laminate after forced BGA rework. Boards supplied in a single laminate from a single source were assembled with the 40 mm BGA devices using the standard high thermal mass conditioning and attach reflow excursions using the profile displayed in Figure 5. The lot for comparison was then subjected to two further thermal excursions on standard semiautomated hot gas rework equipment. The initially attached component was removed the site was dressed using standard methods and then another component was attached using SAC305 solder. The assembly lots were then spherical bend tested at a target primary strain rate of 3000 microstrains per second. Microstructures were examined and failure distribution parameters were established for each lot. Board and component design and construction were identical to those tested in DOE1.

Experimental Design: DOE3

The premise for this experiment was that by holding all other factors including board design constant the inherent

susceptibility of the resin/glass system would be comparable. Test vehicle assemblies built from a single set of design da ta and specifications were built with OSP solder surface by a variety of qualified suppliers in a variety of laminate resin systems. The PWB suppliers provided sample lots that complied to the design criteria which were then all assembled with the same 32 mm monolithic ceramic device using a single thermal recipe for SMT reflow. This process did allow for some variation in the material beyond the resin system. Thickness specifications are normally +/10% which allowed the PWB facilities to utilize their qualified pressing

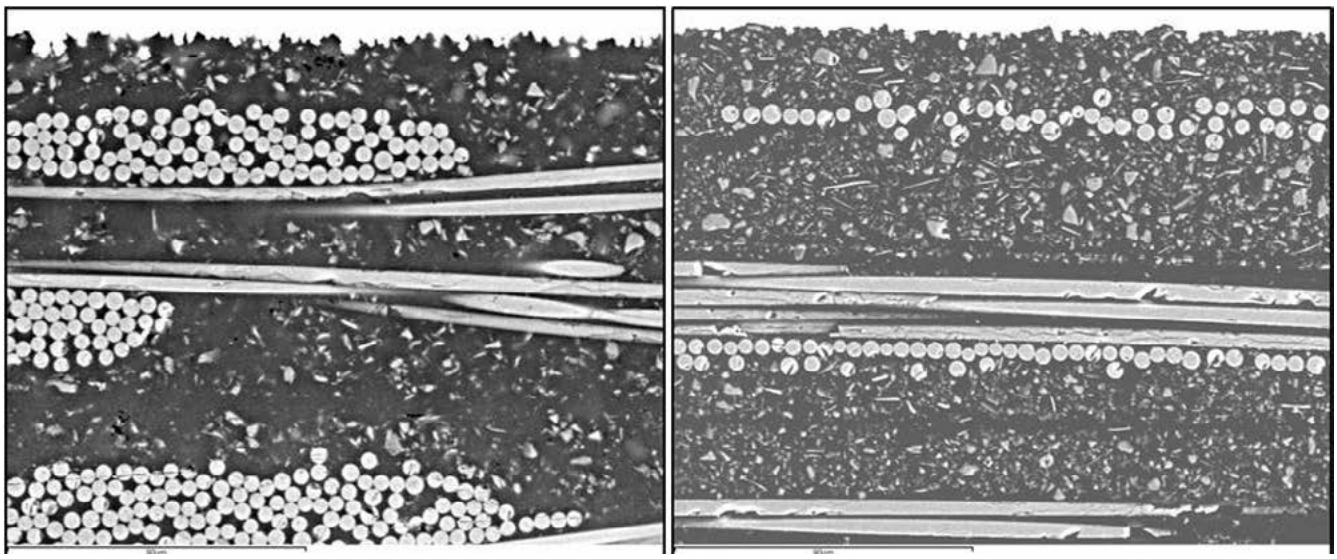

Figure 6: Variation in glass reinforcement.

processes which must be optimized for both resin cure and finished st ack height. The resin and glass systems themselves were worthy of inspection. There is a notable difference in the bundles of glass reinforcement fibers. In some lots they were very well defined elliptical shapes while in others the glass was far more dispersed and difficult to identify in the filled resin system. This dispersed glass is implemented by some suppliers to improve the consistency of laser ablation drilling techniques. The variation in glass reinforcement is displayed in Figure 6.

Results: DOE1

Previous work with more compliant systems has allowed us to record either the change in resistance that signifies failure at one of the solder interfaces or a localized minimum in the strain profile that indicates a laminate failure in either the board or the package substrate. These very stiff "high complexity typical" systems do not store enough energy in the package to create these events in the strain gauge signal at low strain levels. Strain events only occur at higher levels of displacement where they are related to catastrophic failures and do not represent the first damage to the system. Alternatively events may occur at low strain levels but the systems produce enough signal noise from vibration effects to make the events undetectable. In this experiment Mode 10, "Pad crater" was not only the dominant failure mode under this test method, it was the only failure mode detected in assemblies from standard "primary attach" processes. Destructive evaluation of samples subjected to increasing levels of displacement (flexure) determined that for this material and test setup there are three distinct displacement zones where the material response can be defined. These zones are depicted in Figure 7 and are described as:

- Zone 1: A safe zone where no damage occurs
- Zone 2: A mixed zone where package corners both fail and survive
- Zone 3: A zone where all package corners fail

The intent of further testing was to define the boundary conditions for Zone 2 and generate distributions that would allow extrapolation to safe working limits. We defined a "step stress" procedure to test groups of samples to progressively higher peak strains at fixed displacement rates. For each data point peak strain, rising strain rate and outcome were recorded. The distributions of these estimates of survivable strain were used to generate working limits.

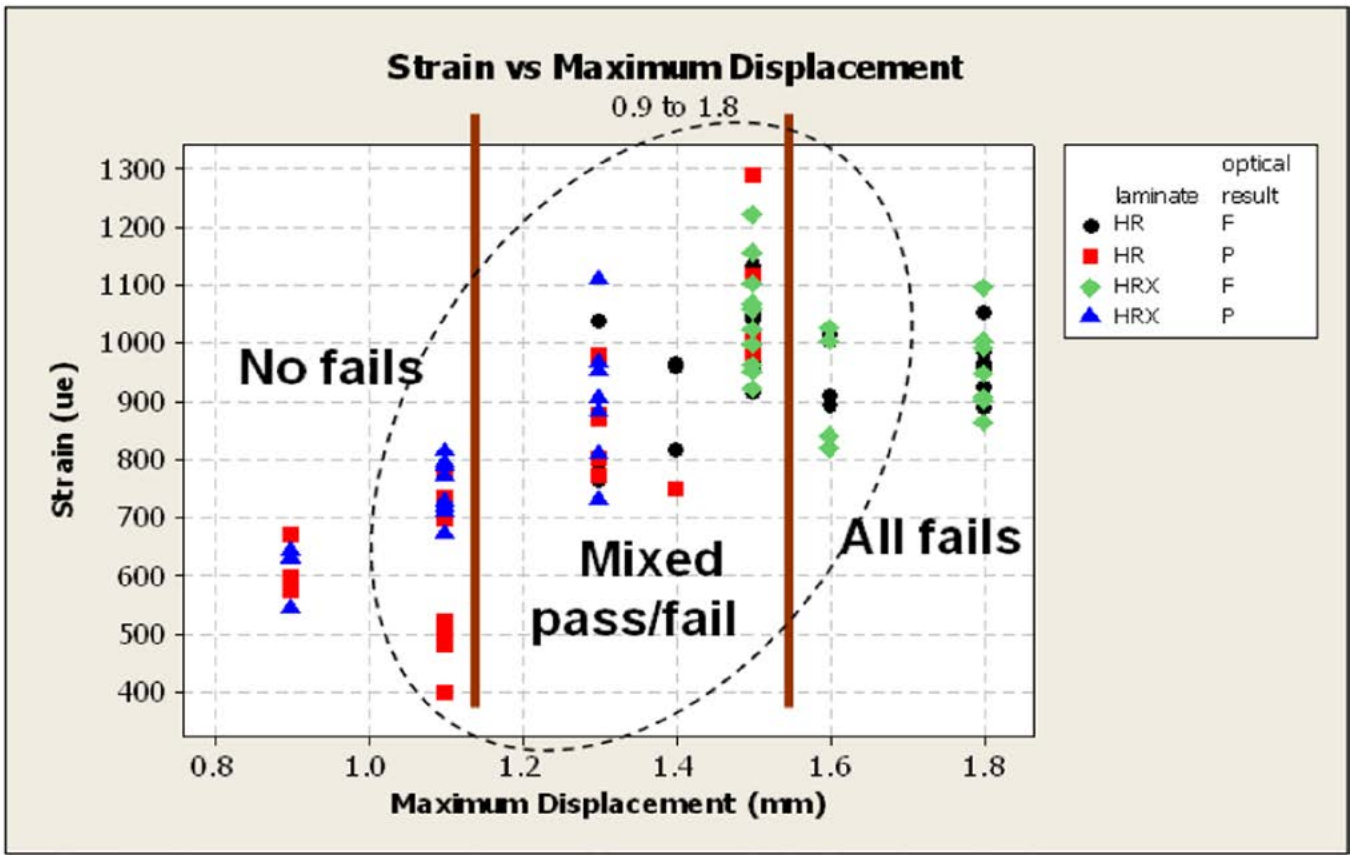

Figure 7: Mixed response zone.

This work also required that we redefine our criteria for failure. In most compliant systems where "strain events" are recorded, failed samples inspected after penetrating dye has been applied exhibit complete separation of the BGA structure from the board. The crack path is very consistent; it involves a cone-shaped failure in the "butter coat" of the laminate and follows the top surface of the glass bundles in the first reinforcing layer. We have yet to see any work in the literature that investigates the crack path. We normally assume that cracks initiate at the surface but it has been postulated and subsequently demonstrated that there could be internal separation and coalescence of micro cracks below the surface before this catastrophic failure occurs. As result of our analysis we have defined two distinct portions of the pad crater crack, which represent two different levels of failure categorized as cohesive and adhesive separation.

- **Cohesive Separation:** The crack initiates at the surface of the laminate in close proximity to the solder pad and travels at approximately 45 degrees to the first level of reinforcement. Testing identified that this portion of the damage can be generated without any progression under test conditions to the next phase
- **Adhesive Separation:** The crack subsequently follows the top surface of the first reinforcement layer until it finds a short path back to the surface inboard of the solder pad

We understand now that in these stiffer systems the cohesive portion of the crack occurs without generating any discernible disturbance in the strain profile, but we believe that it represents a significant risk to product shipping into service environments. To summarize, any damage to the laminate resin system discernible by dye penetration and optical microscopy is considered to be a failure.

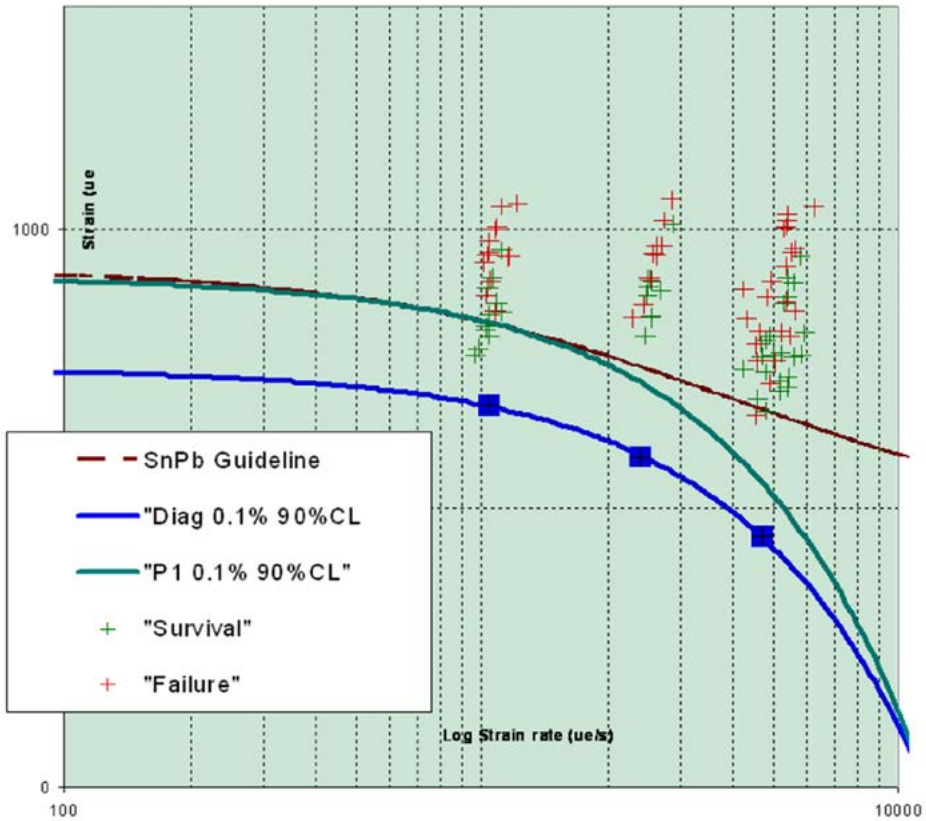

Figure 8: Typical strain/strain rate behavior in FCBGA devices.

Failure distributions were best modeled using Weibull distributions for two reasons. First: The failure rate is expected to be constantly increasing as the stressing factor is increased. In fact, there is a point at which no further survivors will be detected. This is the boundary between Zone 2 and Zone 3. The data includes both failures and survivors. In statistical terms the data is right censored. As expected the scatter in the results increases as the testing strain rate is increased. In general the distributions of all data at the various strain rates are consistent with the behavior currently accepted by the industry. The survivable peak strain decreases as rising strain rate increases.

Distributions are combined for individual board thicknesses. Data and calculations of safe limits were plotted in the common strain / strain rate format on log linear graphs. Basic regression techniques were used to generate safe working limits over the range strain rates associated with manufacturing processes. Figure 8 is a typical output from this process and displays individual data points, and the two limit curves based on diagonal and principal strains for a single board thickness. This process was repeated for all board thicknesses under study. This data was compared against the current estimate of the board thickness relationship and seems to correlate well. There is some evidence that the strain rate dependency for this fracture mode is different than the relationship currently accepted by the industry for SnPb assembly.

Results: DOE2

The two process streams provided very different thermal histories for the lots. The "primary attach" lot was exposed to approximately 6000 degree seconds above T_g for the laminate whereas the "forced rework" lot was exposed to approximately 14000 degree seconds above the T_g point.

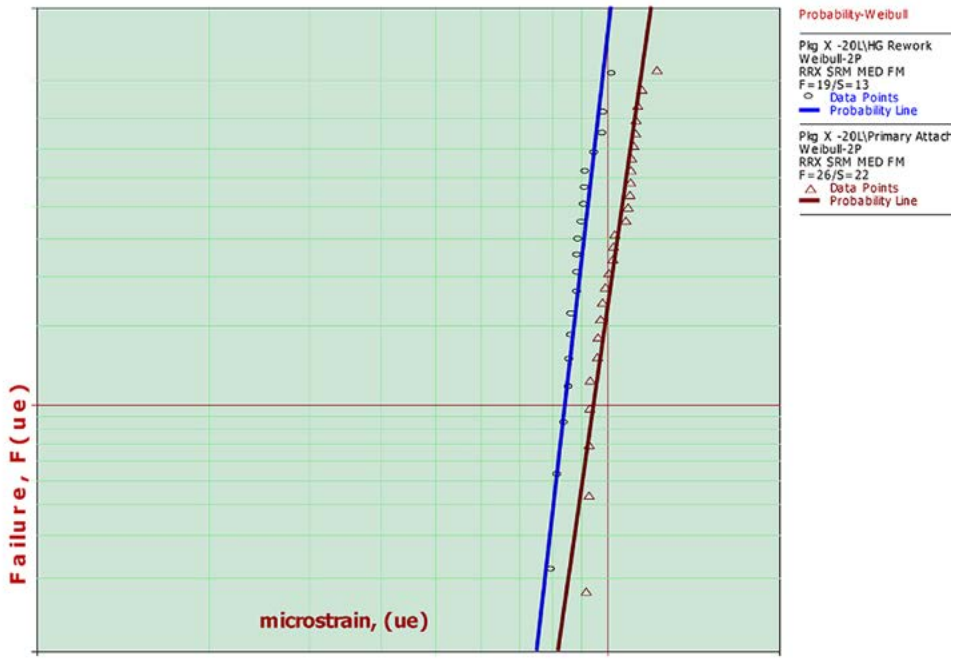

Figure 9: Weibull distributions for thermal excursion lots.

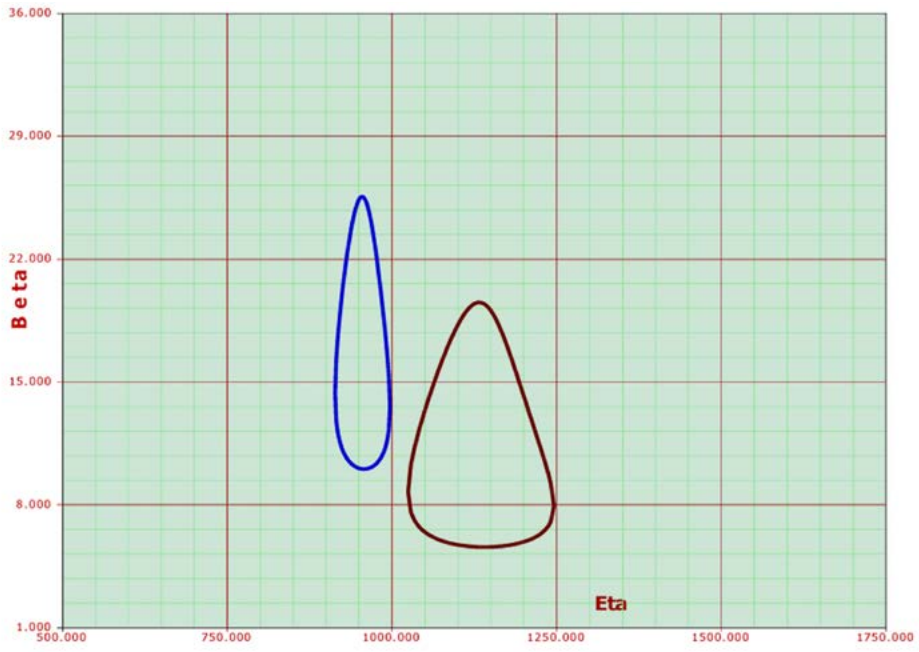

Figure 10: 95%CC for thermal excursion distributions.

The Weibull distributions shown in Figure 9 are well formed. When reviewed together with the 95% confidence contours (CC)s displayed in Figure 10 they clearly define a statistical difference between the sample lots. Based on these distributions there is a 13% reduction in survivable strain associated with the forced rework of this laminate material. Apparently,

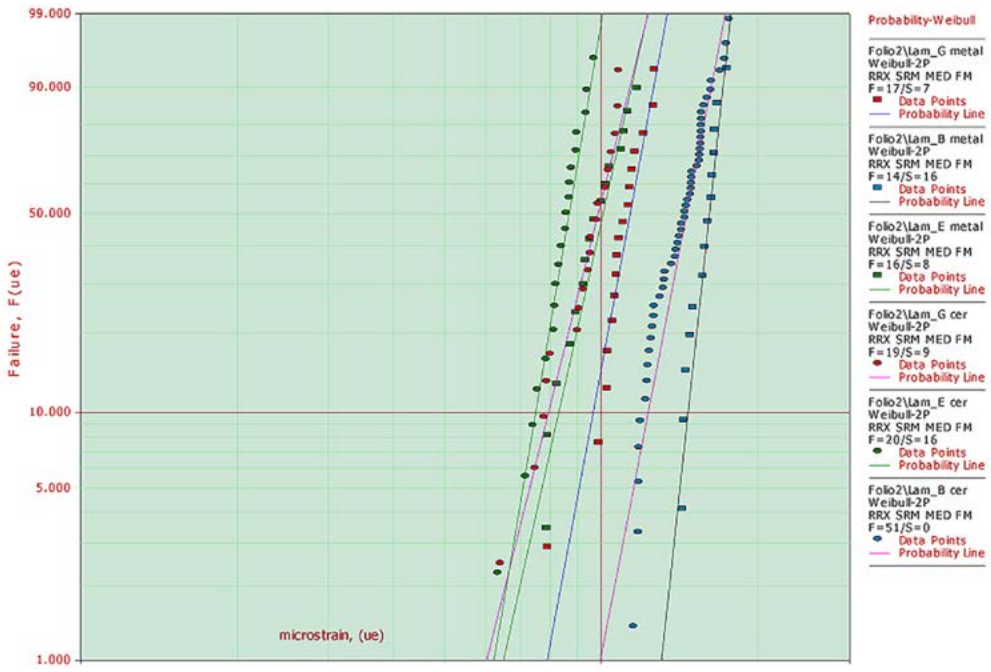

Figure 11: Weibull distributions—DOE3.

the substantial additional thermal excursions related to hot gas rework of BGA devices do affect the resistance of the material to damage. This might be attributed to higher levels of cross-linking in the polymer, which reduce the compliance of the material.

The additional thermal exposure of laminates and solder pads caused by forced rework of large BGA devices also produces changes in the board side solder interfaces and where ENIG pad plating is present. A second failure mode, Mode 8— Fracture at the NiP/NiSn IMC layer at the board side was identified as a second failure mechanism but Mode 10 remains dominant. The occurrence of two failure modes did not significantly affect the distribution of the data or the calculated limits.

Results: DOE3

The six lots processed for this experiment were selected from a larger group of tested laminates with the intention of covering the range of responses that have been encountered. We have endeavored to select a laminate from the worst and best performers as well as one from the middle of the pack. All lots meet the experimental expectations for Beta values based on testing from that significant number of laminate lots. The selected lots exhibit the well-formed distributions that are expected for single failure modes and meet our condition for a well defined mixed response zone.

The Weibull distributions are plotted in Figure 11. As expected there is a benefit to characteristic life by moving to a more compliant package construction. It is also notable that the rank order of laminates in terms of survivable strain has not changed under the more compliant system.

The plot of 95% CC for the Weibull distribution parameters displayed in Figure 12 clearly demonstrates the increase in characteristic life for each individual laminate which are defined by color. There is some variation in Beta value driven by the proximity of the boundary condition for laminate B. The top ends of both of these distributions are very close to or at the strain level where mixed failure modes would be expected to occur.

Summary

The spherical bend test methodology has been shown to provide informative comparisons between sample lots created by varying

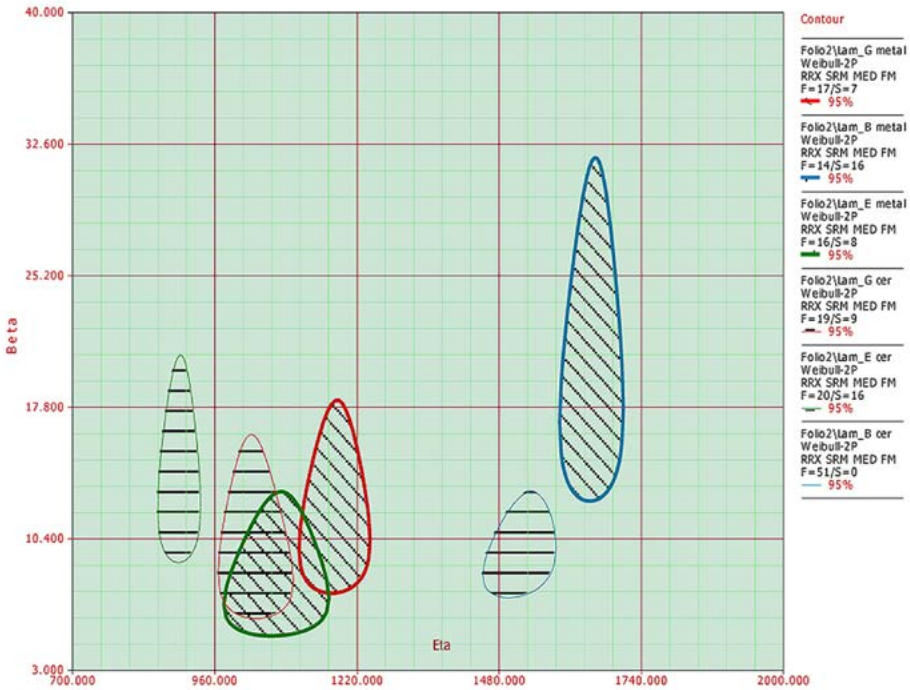

Figure 12: 95% CC for DOE3 distributions.

laminate material, process thermal history and package construction. The nature of the test produces comparisons at extreme or boundary case conditions but the information provides insight into more standard conditions as well and may be widely applicable. The expansion of the test program to begin to establish the relationship to package stiffness may enable a first level model of susceptibility to this type of mechanical damage around BGA devices. The fact that the rank order of laminate materials did not change with alternate package construction leads us to believe that a more comprehensive model than the current is possible. We would with increased amounts of data be able to expand on the current, board thickness and strain rate model to include laminate material and package stiffness.

Observations

- The dominant failure mode for Pb-free compliant materials under flexure is pad crater
- The process strain limit model developed for IPC 9704 when interfacial fracture was the dominant failure mode can be modified to produce more realistic results for Pb-free compliant materials
- Under the spherical bend test geometry Pb-free-compliant materials have been shown to have a different strain rate dependency for mechanical failure under load
- Significant differences in laminate material performance are evident under this test method
- Laminate material susceptibility to this defect increases with thermal exposure

Acknowledgements

The authors would like to thank LSI and IBM for their contributions of material. **PCB**

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Behavior of Materials in the Manufacturing Environment

by Hardeep Heer
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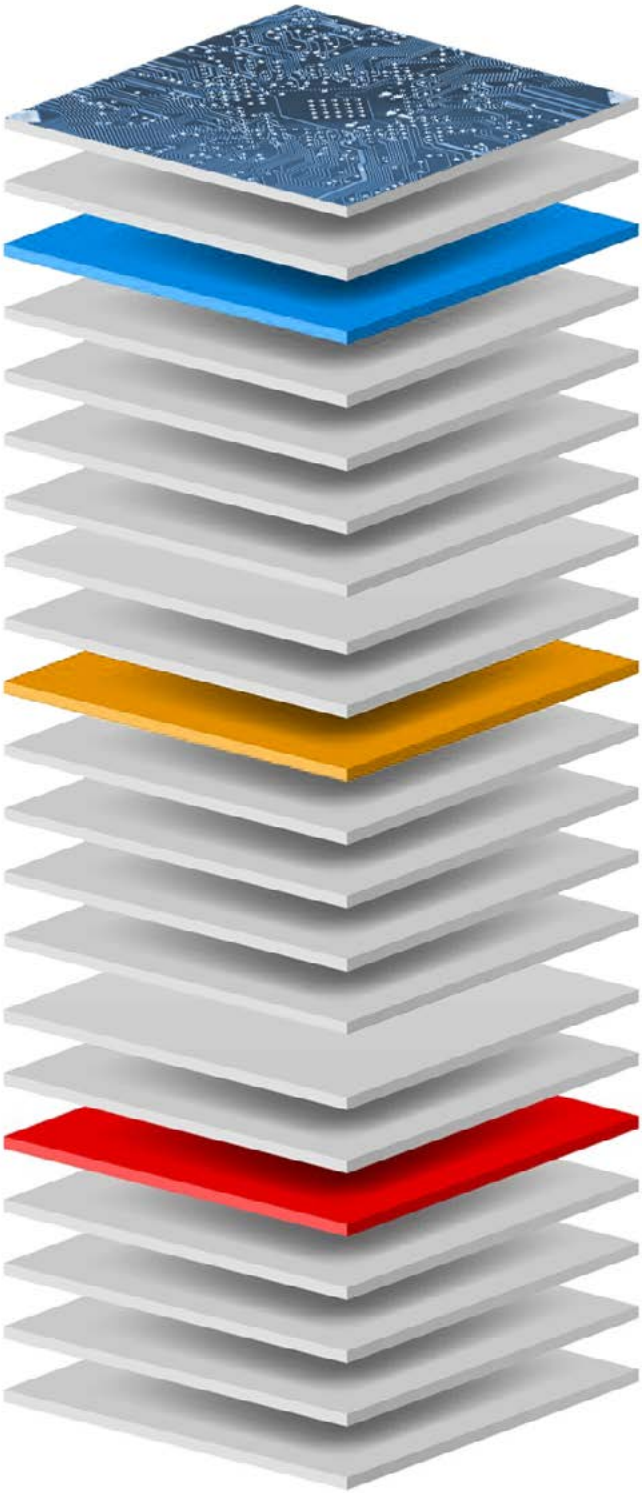
Abstract

This study was conducted to understand seven materials' reliability, behavior of dielectric constant and dissipation factor over medium to high frequencies. A modified version of HDPUG design was used for evaluation. This test board contains IST, CAF, thermal cycling and impedance (both microstrip and stripline) coupons. In addition to these we added HATS coupons. Materials were chosen from FR4 family and selection was made based upon our present and future needs. Dielectric constants of these materials ranged from Dk 3.6–Dk 4.2, as published, at 10GHz. This document shows the effect of Dk and Df values from 10GHz to 20GHz and also shows their performance for lead free assembly process when tested using IST and HATS test methods. In addition, CAF testing was done on five of the seven materials.



Introduction

As signal speeds are getting higher, a better understanding of material performance is required. Materials which were good at low frequencies may not be good for higher frequencies. The goal of this study was to:

1. Compare material reliability using HATS and IST test methods.
2. CAF analysis of these materials.
3. Study insertion losses for materials chosen and do a comparison of these materials for frequencies between 1GHz—20GHz.

A modified HDPUG design (Figure 2) was adopted as a test vehicle. To keep the testing

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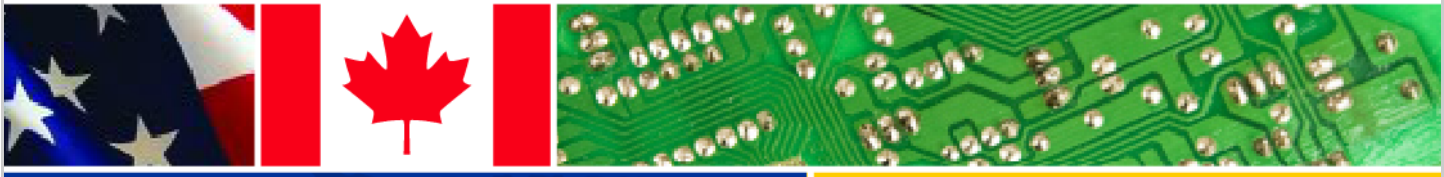

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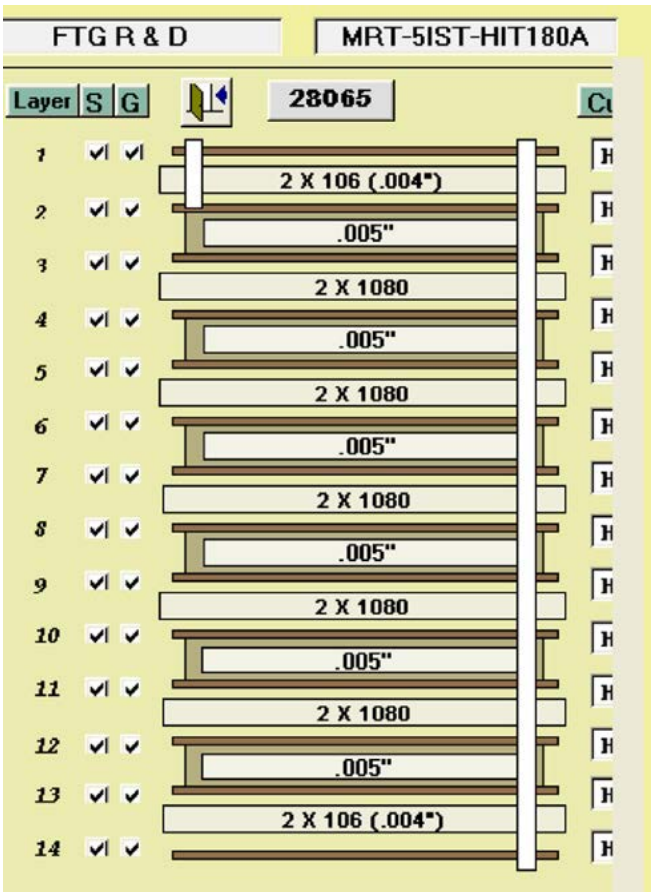


Figure 1: Stackup for modified HDPUG design (as shown in Figure 2).

manageable, thermal cycling and water absorption coupons were not tested. However, HATS coupons were added to the panel design. The stackup used is shown in Figure 1.

Material for test was supplied free of cost by each material supplier. Materials were given a code name for the study. Each material supplier will have cross reference to their material only. Table 1 gives the detail of the material properties as published on technical data sheets. All material tested are rated by their manufacturers as lead-free assembly compatible material. Materials ranged from a Dk of 3.7–4.7 and were in T_g range of 1700–2100°C.

All samples were produced using the same equipment and within a close time frame window. No process abnormalities were seen during processing period.

Test parameters selected are given below.

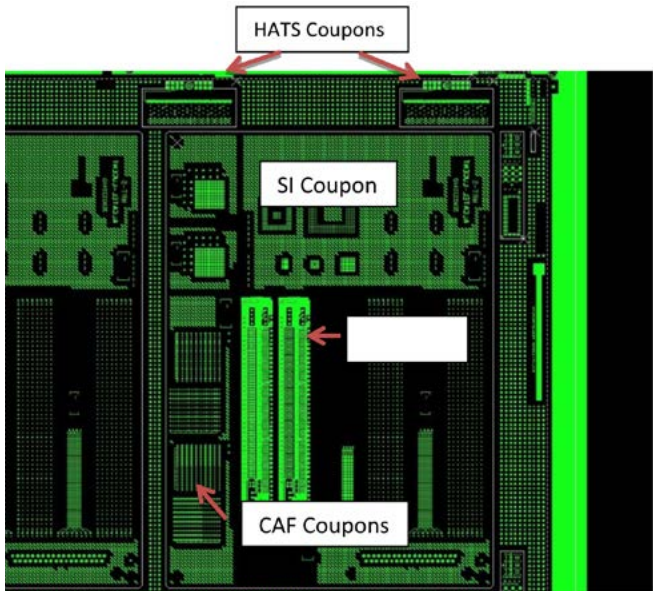


Figure 2: Modified HDPUG design.

HATS Preconditioning and Test Parameters

Test Conditions

- Six coupons for each material type to be cycled through 6x @ 260°C assy. simulation
- Test temperatures for cycling to be -40°C temperature to 145°C, 15 minutes @ temperature and transition time is 30 seconds
- Test cycles to be 1,000. Cycles or a change of 10% in resistance, whichever comes first
- Testing done by Integrated Reliability Test Systems, Inc. (IRTS)

HATS Test Analysis

All coupons showed no signs of delamination after preconditioning. During HATS testing all materials met the set criteria of 1,000 cycles without the exception of material 'RA' which had an average of 941 cycles for net 2 and 900 cycles for net 4. Material 'B' had an anomaly where there were spikes of 6% change in resistance between 600 and 800 cycles and after that the coupon went back to less than 0.2% change. Below are the charts for material 'A' (showing change in resistance for a typical good coupon), material 'RA' and material 'B'.

R& D NEW MATERIAL TESTS				
MATERIAL	**TG – ^{0}C**	**Dk**	**Df**	CTE 'z' PPM / ^{0}C
A	170	4.0	0.010	34
B	171	4.4	0.010	33
C	170	4.7	0.018	50
D	200	3.7	0.008	40
E	180	4.0	0.012	50
RA	200	3.7	0.009	55
RB	210	3.7	0.009	65

Table 1.

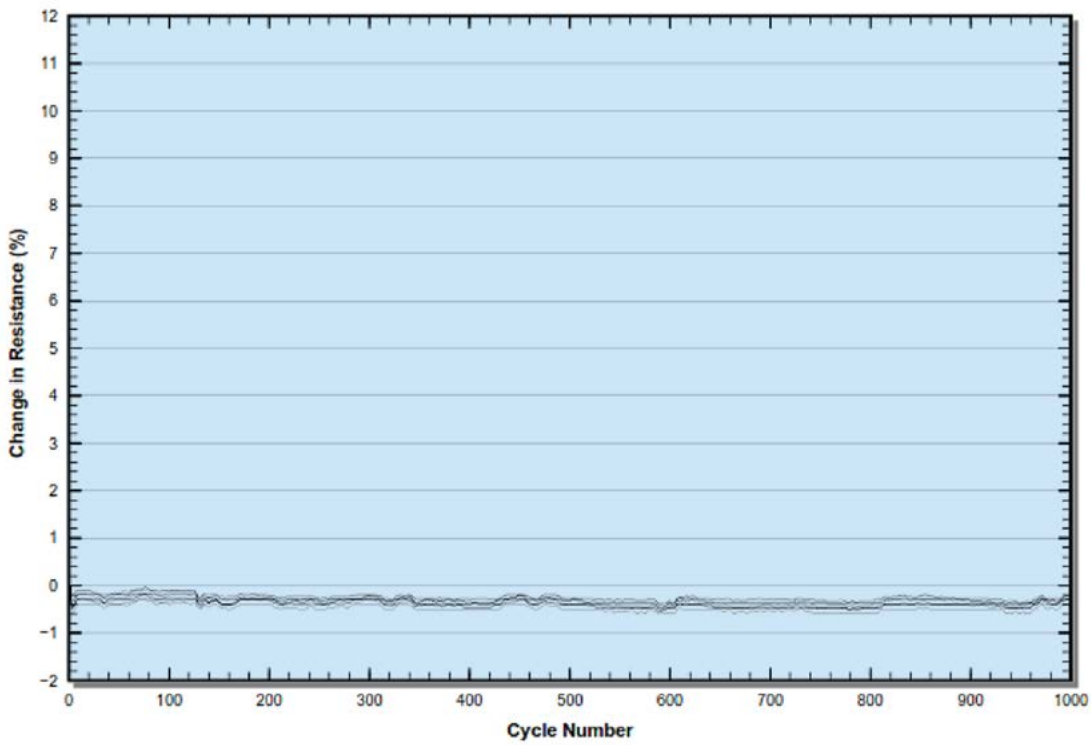


Figure 3: Material 'A.'

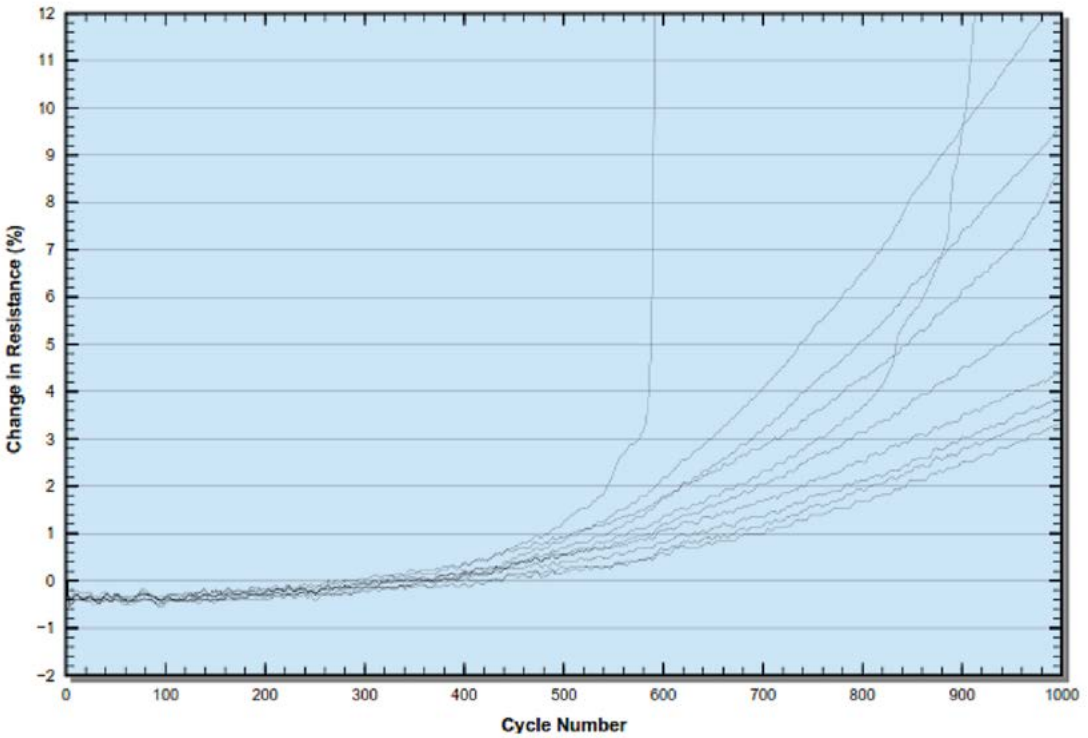


Figure 4: Material 'RA.'

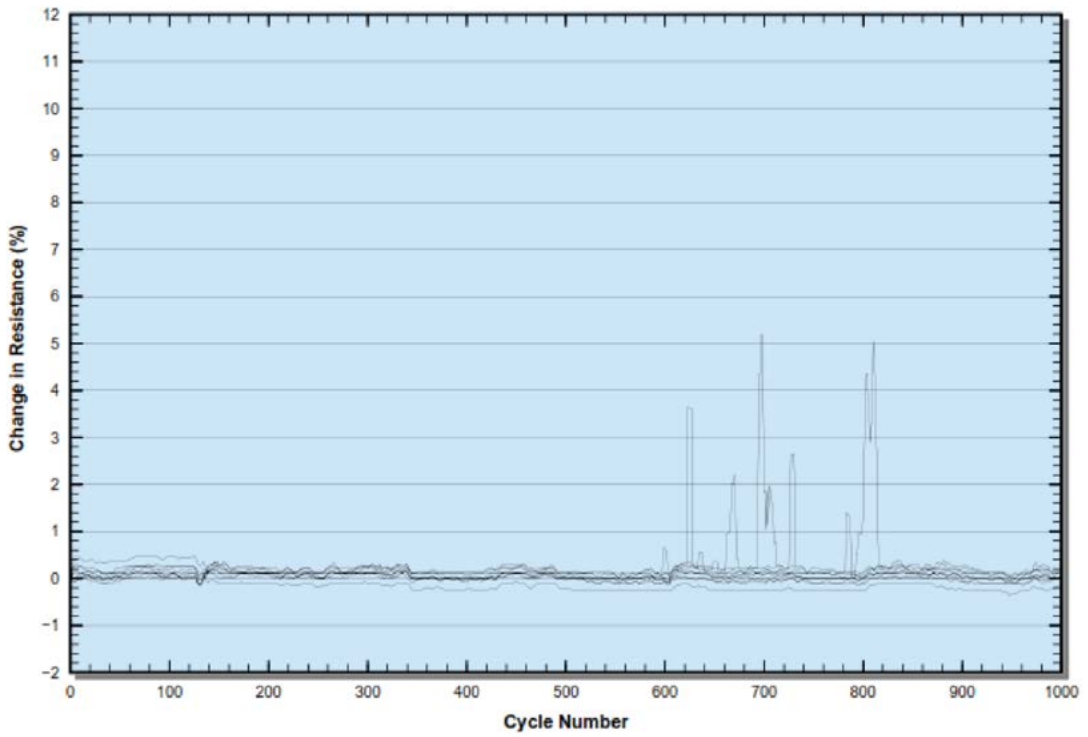


Figure 5: Material 'B.'

IST Testing

Preconditioning & Test Conditions

- Six coupons for each material type will be cycled through 6X @ 260°C assy.
- Test the coupons for failure, any failure to be recorded
- Capacitance readings will be taken before preconditioning, after preconditioning and at the end of cycling
- Any change in capacitance > -6.5% will be considered a failure
- Test temperatures cycling will be room temperature to 150°C in 3 minutes +/- 5 seconds and cooling in approximately 2 minutes
- Test cycles will be 1,000. Cycles or a change of 10% in resistance, whichever comes first
- Testing done at PWB Interconnect Solutions

Test Results

Capacitance Analysis

Six sections for each of the seven materials tested showed various degree of % change in capacitance value. Material 'A' & 'B' showed excellent results with a maximum of -4.13% and -3.46% change in capacitance. Results for material 'C' and 'D' had a maximum of -5.40% and -5.05% change, which is still considered acceptable below the maximum allowable percentage change of -6.5%. Material 'RA' showed signs that material degradation had started but percentage change was still below the maximum allowable range. However, material 'E' and 'RB' were at -7.02% and -8.59%. In both of these cases material damage was observed. See Table 2 for typical capacitance results for 0.8 mm (0.032") test coupon.

It was observed that if test coupons have retained moisture then we will see an improve-

% Capacitance Change in Picofarads - Group A .032" / 0.8mm after 6x260°C							
Layer	A	B	C	D	E	RA	RB
2/4	-4.13%	-2.84%	-5.40%	-5.05%	-7.02%	-6.26%	-6.59%
4/6	-2.67%	-2.59%	-4.08%	-3.89%	-7.02%	-5.50%	-7.13%
6/7	-1.61%	-1.60%	-2.98%	-3.13%	-6.70%	-4.15%	-6.10%
7/8	-1.69%	-1.92%	-2.84%	-3.14%	-5.71%	-4.52%	-8.59%
8/9	-1.57%	-1.64%	-2.92%	-3.18%	-6.67%	-4.20%	-6.04%
9/11	-2.78%	-2.66%	-4.11%	-3.60%	-7.05%	-5.57%	-7.08%
11/13	-3.98%	-3.46%	-4.95%	-4.00%	-6.74%	-5.82%	-5.99%

Table 2.

% Capacitance Change in Picofarads - Group A -1.0mm (0.040") after 6x260°C							
Layer	A	B	C	D	E	RA	RB
2/4	-5.02%	-4.56%	-6.01%	-1.89%	-7.33%	-6.48%	-3.62%
4/6	-3.24%	-3.90%	-4.46%	-2.51%	-6.77%	-6.20%	-3.68%
6/7	-1.98%	-1.96%	-3.17%	-2.46%	-5.46%	-4.81%	-3.62%
7/8	-1.96%	-2.49%	-3.07%	-2.86%	-5.66%	-5.26%	-3.59%
8/9	-1.82%	-1.95%	-3.12%	-2.71%	-5.43%	-4.83%	-3.49%
9/11	-3.20%	-3.64%	-4.47%	-2.50%	-6.79%	-6.06%	-3.67%
11/13	-4.85%	-4.62%	-5.73%	-1.51%	-7.00%	-5.93%	-3.69%

Table 3.

.032" / 0.8mm Via to Via Spacing							
Type	A	B	C	D	E	RA	RB
1	3000	3000	1162	1587	1847	232	1108
2	3000	3000	1738	839	2847	355	981
3	3000	3000	1329	1074	731	149	1313
4	3000	3000	487	1042	1573	160	482
5	3000	3000	1437	792	2557	151	804
6	3000	3000	1793	1078		241	
Mean	3000	3000	1324	1069	1911	215	892
Std Dev	0	0	476	282	837	80	315
Min	3000	3000	487	792	731	149	482
Max	3000	3000	1793	1587	2847	355	1313

Table 4.

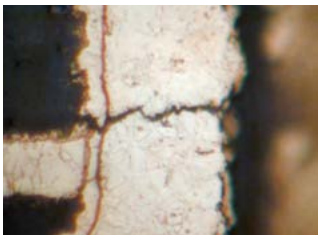
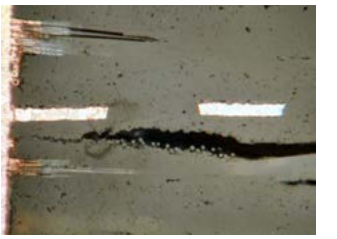


Figure 6.

Figure 7.



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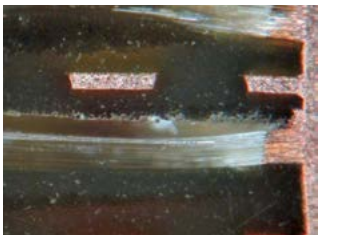


Figure 9.

ment in capacitance value for the outer layers as the test progresses. This was particularly evident in case of material 'E' which showed an improvement in capacitance value between 6x260°C and at the end of test measurements. Since all materials were stored under the same conditions, it leads us to believe that material is more hydroscopic. Also, 0.8 mm pitch showed early capacitance failure for material 'RA' indicating that either the material bond was compromised during drilling or that the material bond strength was not the best.

IST Test Analysis

A summary of test results is shown in Table 4. The data shown is cycles to failure for six coupons of each material type. Any failure that was process related has been taken out.

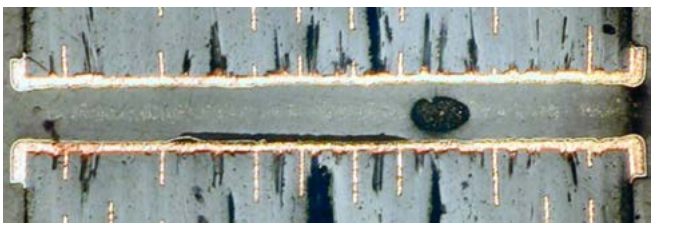


Figure 10.

In our IST results, material 'RB' showed good cycles to failure but when sectioned we saw the extent of damage to the material in Figures 6–9. The degree of delamination seen in Figure 10 agrees with the results seen in capacitance measurements of these coupons. The material had degraded to a stage where further cycling would not have had any further degradation.

Material	Hole wall to Hole wall 20mil				Hole wall to Hole Wall 16mil			
	Coupons tested	Coupons failed	Min. Hrs.	Max. Hrs	Coupons tested	Coupons failed	Min. Hrs.	Max. Hrs
B	3	1*	120	>500	3	1**	24	>500
C	3	2**	24	>500	3	2	24	>500
E	3	0	>500	>500	3	2	24	>500
RA	3	3	24	48	3	3	24	24
RB	3	3	24	24	3	3	24	48

* - Failure due to surface contamination, see Fig. 11
** - Failure mode could not be found for one 'B' and one 'C' material.

Table 5.

Figure 11, 12 and 13: Failure due to surface contamination.

CAF Preconditioning and Test Parameters

Test Methods

1. Testing was carried out in accordance with IPC-TM-650 Method 2.6.25, Conductive Anodic Filament (CAF) Test.

2. 100 volts DC bias was applied to each circuit through a 1 mega-ohm series resistor. Voltage drop across the resistor was measured daily in each sample with a high-impedance voltmeter, without removing or altering the applied bias.

3. The test method allows for two humidity levels. The more aggressive environmental condition option of 85°C (+/-2°C) and 87% (+3/-2%) relative humidity was chosen for this test.

In all, 30 coupons were tested. No coupons were tested for material 'A' and 'D'. For materials 'B', 'C', 'E', 'RA' and 'RB' three coupons each for grid size 40 mm (16 mil) and 50 mm (20) were tested in accordance with IPC-TM-650, method 2.3.25. Below is a summary of the results for the 30 coupons tested.

Figures 12 and 13 show the typical CAF failures seen on failed coupons.

This CAF data shows that the CAF failures increase as the pitch reduces. Coupons at 16 mil pitch had 16% more failures than those 20 mil pitch. The failure rate is influenced by both the material and the drilling process. Since this exercise was to compare different materials under the same manufacturing conditions, we evalu-

ated the degree of failures for each material. It is also important to see that materials 'E', 'RA' and 'RB' had 100% failures. These results are in line with IST and capacitance results. Those materials which had poor performance for IST and capacitance also showed poor results for CAF.

Signal Integrity (overall insertion loss)

Test Conditions:

- Conductor length: 5 inches
- Impedance: 50 ohms
- Materials: RA, RB, A, B, C, D and E
- Equipment used: Agilent VNA N5230
- Testing done at ITEQ labs

Test Results

Insertion Losses for Microstrip Line

Figure 14 shows a clear separation is seen between materials as the frequency increases from 10GHz to 20GHz. Material 'RB' still has the lowest Df value at -1.894dB/inch at 20GHz. Percentage change for material 'RB' was the lowest at 66%. Material 'C' had the highest percentage change at 79%.

The same was true for the stripline. Material 'RB' had the lowest Df value at -1.939dB/inch and material 'C' had the highest Dk loss at -3.376dB/inch. Materials 'A' and 'RB' had the lowest percentage change at 87%. Materials 'E' and 'RA' had the highest percentage change at 94%.

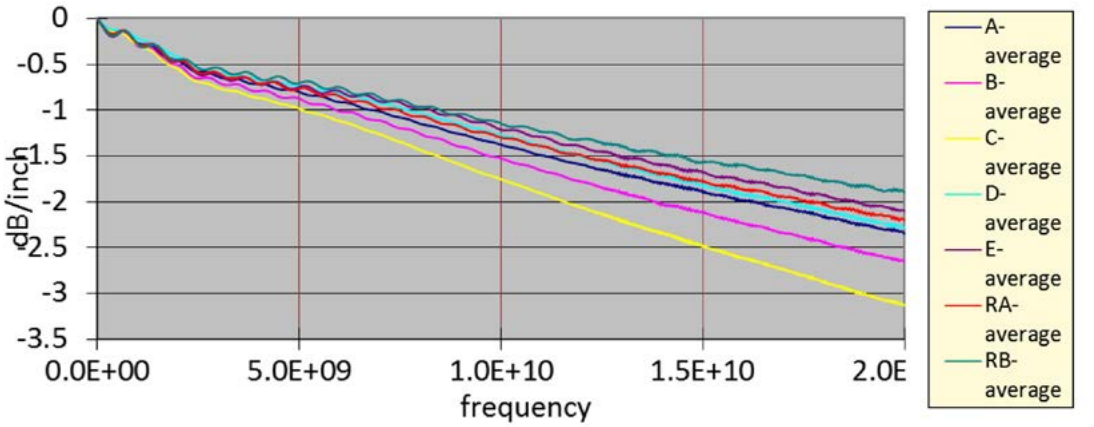


Figure 14.

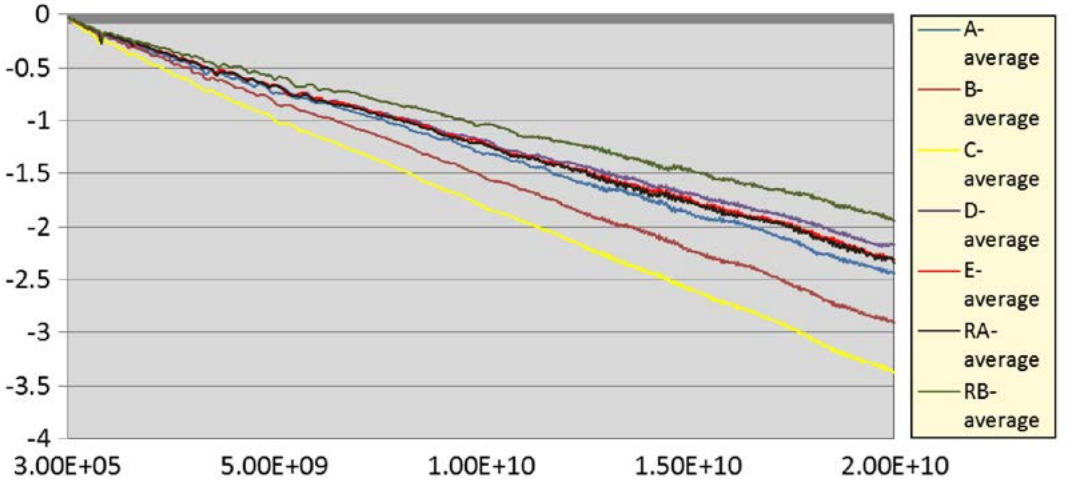


Figure 15.

Insertion Losses for Stripline

Observations Based on SI Data:

1. Published and actual Df and Dk values were found to be very close.

2. Insertion losses for both stripline and microstrip materials tested are in a small band width below 10GHz. However, the gap widens as we move towards 20GHz.

3. Percentage change in Df value ranged from 7.3% for material 'C' to 17.9% for material 'RA' as the frequency increases from 10GHz to 20GHz.

4. Percentage change in Dk values for materials is below 1.5% as the frequency increases from 10GHz to 20GHz.

5. There is a direct relationship between Dk and delay time. Material 'RB' with a Dk value of 3.7 has the lowest delay time.

Materials	Delay time @ 10GHz (ps)	
	Micro-strip line	Strip-line
A	706	878
B	700	858
C	707	855
D	673	801
E	671	813
RA	672	810
RB	658	797

Table 6.

SI Results Conclusion

1. By the insertion loss measurement, material 'RB' has the best signal integrity. We can classify these materials as below:

-- signal integrity (overall insertion loss):
RB (the best) > RA~E~D > A > B >C

2. Evaluation based upon delay time and Dk and Df extraction, the material (in order of Dk and Df value) are:

Dk -- RB (the lowest) < RA~E~D < A~B~C
Df -- RB (the lowest) < D < RA~E < A < B< C

Project Summary

Table 7 gives a summary of all the test results. It should be noted that some of the values

Material	HATS Cycles	% Change in Capacitance	IST Cycles	CAF Cycles		Dk @20GHz	Df @ 20GHz
				0.5mm	0.4mm		
A	1,000	(-)2.25	3,000	Data Not Available		4.24	0.0155
B	1,000	(-)2.38	3,000	500	1 out of 3 below 500	4.09	0.0207
C	1,000	(-)3.89	1,324	1 out of 3 below 500	2 out of 3 below 500	4.04	0.025
D	1,000	(-)3.71	1,069	Data Not Available		3.57	0.0130
E	1,000	(-)6.70	1,911	500	2 out of 3 below 500	3.68	0.0145
RA	960	(-)5.15	215	24	24	3.62	0.0151
RB	1,000	(-)6.79	892	24	24	3.53	0.0109

Table 7.

are averaged for ease of data review. However, this is still representative of actual test results. Based on the test data available, a suitable material can be selected to fit individual needs.

Data has shown that, among the materials tested, materials that had least insertion losses performed poorly for reliability. The materials selection process should take all aspects of material performances into account when selecting a material. With that in mind, material 'D' would be the best performing material in Dk range of 3.57, @ 20GHz, followed closely by material 'B' with Dk of 4.09 and material 'A' at 4.24 Dk. However if a variation of 0.52in Dk value, @ 20GHz, can be compensated by design, then material 'B' becomes the best overall choice.

Similar studies are planned for polyimide, RF and thermally conductive materials. **PCB**

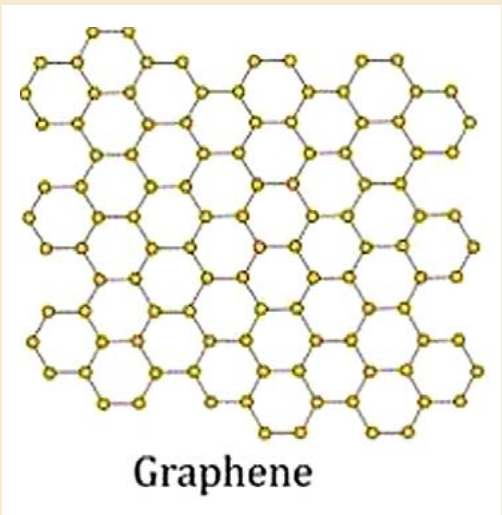
Hardeep S. Heer is vice president of engineering and CTO at Firan Technology Group.

Artificial Graphene a New Breed of Ultra-thin Super-material

A new breed of ultra thin super-material has the potential to cause a technological revolution. Artificial graphene should lead to faster, smaller, and lighter electronic and optical devices of all kinds, including higher performance photovoltaic cells, lasers, or LED lighting.

For the first time, scientists have been able to produce and analyse artificial graphene from traditional semiconductor materials. Such is the scientific importance of this breakthrough, in findings published recently in one of the world's leading physics journals, Physical Review X. A researcher from the University of Luxembourg played an important role in this highly innovative work.

Graphene (derived from graphite) is a one atom thick honeycomb lattice of carbon atoms. This strong, flexible, conducting, and transparent material has huge scientific and technological potential. Just recently discovered in 2004, there is a major global push to understand its potential uses. Artificial graphene has the same honeycomb structure, but in this case, instead of carbon atoms, nanometer-thick semiconductor crystals are used. Changing the size, shape and chemical nature of the nano-crystals makes it possible to tailor the material to each specific task.



Graphene

The University of Luxembourg is heavily involved in cross-border, multidisciplinary research projects. In this case it partnered with the Institute for Electronics, Microelectronics, and Nanotechnology (IEMN) in Lille, France, the Debye Institute for Nanomaterials Science and the Institute for Theoretical Physics of the University of Utrecht, Netherlands and the Max Planck Institute for the Physics of Complex Systems in Dresden, Germany.

University of Luxembourg researcher Dr. Efterpi Kalesaki, from the Physics and Materials Science Research Unit is the first author of the article appearing in the Physical Review X. Dr. Kalesaki said, "These self-assembled semi-conducting nano-crystals with a honeycomb structure are emerging as a new class of systems with great potential." Professor Ludger Wirtz, head of the Theoretical Solid-State Physics group at the University of Luxembourg, added, "Artificial graphene opens the door to a wide variety of materials with variable nano-geometry and 'tunable' properties."

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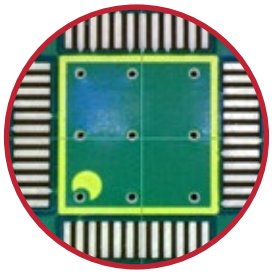

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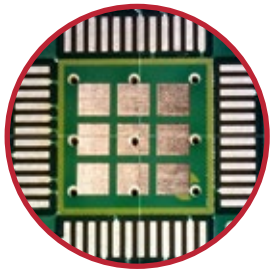

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Welcome to the 2014 IPC APEX EXPO Show Guide

APEX EXPO IPC

CONFERENCE & EXHIBITION March 25-27, 2014
MEETINGS & EDUCATION March 23-27, 2014
Mandalay Bay Resort & Convention Center
Las Vegas, Nevada

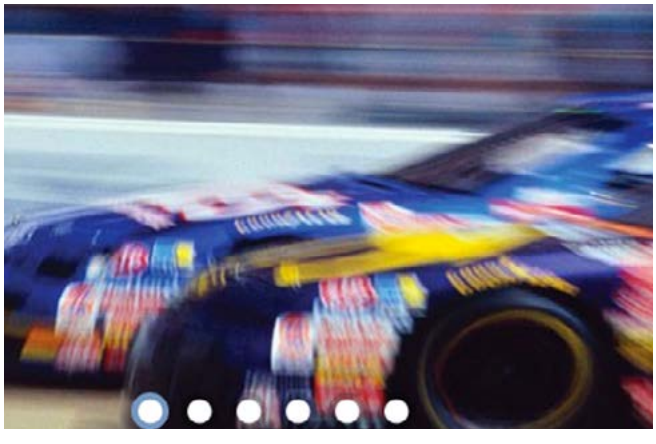
This year, the Mandalay Bay Hotel and Convention Center is the site for the industry's premier event, featuring 430 exhibitors from more than 50 countries. Featuring advanced and emerging technologies in printed board design and manufacturing, electronics assembly, test and printed electronics, APEX is a great place to find new suppliers with new solutions and connect with colleagues from around the world. Plenty of free offerings are on hand—follow these links for a complete online show brochure or event schedule.

Here are a few highlights of what attendees may expect include:

- 430 exhibitors showing equipment, materials and services for printed boards and electronics manufacturing—plus printed electronics! There›s no better place to see and compare.
- The largest technical conference for our industry in the world. Highly selective, the conference presents new research and innovations from experts in the fields of electronics assembly, test and board fabrication and design.
- FREE! Industry poster sessions—Catch up on the latest research and meet the authors.
- Professional development courses provide comprehensive updates on pressing industry concerns.
- Standards development meetings that help shape the future of our industry.
- IPC International Hand Soldering Grand Championship—Compete in or watch the excitement on the show floor.
- Other happenings on the show floor include the Show Floor Welcome Reception on Tuesday and a display of cutting-edge products and services in the New Product Corridor. There are also plenty of informational resources at the IPC Bookstore.
- Networking opportunities including an International Reception, First-Timers' Welcome, IPC Tech Talk, Women in Electronics Networking Meeting, and IPC Government Relations Committee Open Forum allow attendees to meet colleagues, get updates on key issues and share ideas.

To register to attend IPC APEX EXPO 2014, click here.

For an inside look at the show and in-depth interviews with industry insiders directly from the show floor, be sure to visit I-Connect007's Real Time With… site during the show. We're the only publication posting interviews and events in real time!



Free Keynote Addresses All Three Days!

APEX EXPO IPC

Opening Keynote Address:
Tuesday, March 25, 2014
8:30–9:30 a.m.

Peter Diamandis, M.D.
Creating a World of Abundance

Peter Diamandis, M.D., is a dynamic inspirational speaker and tech entrepreneur who will share his insights about how breakthroughs in exponentially growing technologies like artificial intelligence, nanomaterials, 3D printing, robotics and digital medicine will re-engineer products, companies, industries—and even society—over the next 20 years. Diamandis will explain how human society has evolved from "local and linear" to "global and exponential," and how this change has not only spawned the creation of new billion dollar start-ups out of nowhere, but also led to the demise of 50-year-old billion-dollar companies overnight.

Through his work as chairman and co-founder of Singularity University and chairman/CEO of X PRIZE, Diamandis has proven the transformational power that exponentially growing technology has on companies, governments and humanity—and on "do-it-yourself" technologists and small companies who can now achieve what only governments or large corporations could do before.

Day Two Keynote Address:
Wednesday, March 26, 2014
9–10:00 a.m.

James McLurkin
Swarm Robotics and the Toys, Movies and Insects that Made it all Possible

They will flock. They will swarm. And they will tackle the dangerous, dirty and dull jobs for which humans are inherently ill-suited. They're multirobot systems—and one day they will become the norm, according to roboticist, inventor, researcher and teacher, James McLurkin. Inspired by the complex group behaviors found in ants, bees, wasps and termites, McLurkin's work focuses on developing software and programming techniques for groups of autonomous robots with populations ranging from 10 to 10,000.

As a child, McLurkin was constantly playing with Star Wars® toys and building with LEGO® bricks, cardboard boxes and any other materials he could access. Today, armed with degrees in electrical engineering and computer science from M.I.T. and University of California, Berkeley, McLurkin continues to harness his inventiveness to develop the robot swarms that will one day perform jobs ranging from warehouse operations to search-and-rescue missions to Mars exploration. Don't miss this fascinating look at the future of robotics and the technology that is making it happen.

Day Three Keynote Address:
Thursday, March 27, 2014
9–10:00 a.m.

Diandra Leslie-Pelecky, Ph.D.
The Physics of NASCAR

How do you design and manufacture a car that will move at speeds in the neighborhood of 200 mph (321 km/h), yet handle with precision and, most important, keep the driver alive? What technology makes a NASCAR car different from the vehicles you see on the highway?

In a presentation based on her book, "The Physics of NASCAR," physicist and researcher Diandra Leslie-Pelecky, Ph.D., will take you behind the scenes of America's most popular spectator sport—and explain the feats of engineering that make NASCAR work. Drawing on her extensive access to NASCAR race shops, drivers, crew chiefs, engine builders and pit crews, Dr. Leslie-Pelecky will trace the lifecycle of a racecar, from its creation at leading race shops to competing in the action of the NASCAR series.

IPC APEX EXPO 2014

Free IPC APEX EXPO BUZZ sessions

Eight free BUZZ sessions will be offered at IPC APEX EXPO this year. The industry's top technical experts on subjects ranging from automotive and new technologies to conflict minerals, export controls and technology roadmaps will provide insights into timely issues. Admission to the BUZZ sessions and the exhibit hall is free to pre-registrants, a savings of $25 on-site. Click the link above for BUZZ session times and a complete schedule.

This year's BUZZ session topics:

- Underwriters Laboratories: Updates
- Advanced Fabrication Instruction Exchange Between Design and Manufacturing: The IPC-2581B Model
- Promoting Excellence: New IPC Standards for Reliability and Quality, and IPC Validation Services Program
- Forbidden by the Government: Electronics' Materials Restrictions
- INEMI Sustainability Forum
- Counterfeit Components
- What's Coming in 2015 in Electronic Technology Roadmaps

IPC PCB Supply Chain Leadership Meeting

Monday, March 24
8:00 a.m.–5:00 p.m. (includes networking breakfast, lunch and dinner)

A learning and networking forum exclusively for senior-level executives of PCB fabricators and their suppliers, this meeting focuses on issues related to executive decision making in the industry, such as market trends, customer requirements and the economy. Hear from noted industry experts and find out how your peers are addressing common challenges. To view the full agenda, click here.

IPC APEX EXPO 2014 Technical Conference

The IPC APEX EXPO technical conference is known worldwide as one of the finest and most selective in the world. Learn about new research and innovations from key industry players in the areas of board fabrication and design and electronics assembly.

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IPC APEX EXPO 2014

Professional Development Courses

Sunday and Monday, March 23–24
Thursday, March 27

This year, 29 professional development courses are being offered, with each three-hour course focusing on a critical issue within nine specialized areas, including: assembly processes for lead free and tin-lead soldering; cleaning, coating and contamination; design; emerging technologies; environmental issues and compliance; PCB fabrication and materials; printed electronics; quality, reliability and test; and supply chain/business issues. Course attendees will receive an instructional handbook to reinforce key information and use as a reference when they return to work.

Among the instructors leading the courses are Rainer Thueringer, Ph.D., Technische Hochschule Mittelhessen; S. Manian Ramkumar, Ph.D., Rochester Institute of Technology; Phil Zarrow, ITM Consulting Inc.; Jennie Hwang, Ph.D., Sc.D., H-Technologies Group; Ray Prasad, Ray Prasad Consultancy Group; Gerjan Diepstraten, Vitronics Soltec; and Mike Bixenman, DBA, Kyzen.

Click here for a complete list of professional development courses and instructors.

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Drop by the I-Connect007 booth to see for yourself how easy it is to find a fabricator, or create a Showcase listing!

Real Time with... Interviews and Panel Discussions

This year, I-Connect007 and the Real Time with... program returns to Las Vegas, Nevada to bring you complete video coverage of IPC APEX EXPO 2014. Last year, we brought you more than 150 interviews—and this year promises to be just as prolific.

The Real Time with… team of editors, guest editors, and videographers will be working throughout this seminal event to capture the keynotes and bring you one-on-one interviews and panel discussions with the industry's top technologists, engineers, and business leaders as it happens!

Visit Real Time with... for updated information about IPC APEX EXPO 2014.

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LUTHER & MAELZER

Make The Most of High-Frequency Laminates with Resistive Foil

by John Coonrod
ROGERS CORPORATION,
ADVANCED CIRCUIT MATERIALS DIVISION

Resistive foils have been part of PCB laminates for some time and for a wide range of applications. They allow significant savings in space on a PCB in contrast to the use of discrete resistors, even compared to tiny SMT resistors. Some applications even use resistive foils to minimize or eliminate the inductive reactance of an SMT resistive device. Resistive foils can reduce the discrete component device count, free up real estate on a PCB, and even improve circuit board assembly processes. Many high-frequency circuit applications rely on resistive foils as termination resistors for transmission lines or matching resistors for power dividers. Regardless of the application, planar resistor technology has been well defined and established over the years and offers many advantages compared to alternative resistor technologies.

Consistency of resistance values was often an issue during the early days of planar or buried resistors based on resistive foils. Some of the inconsistencies stemmed from how the resistive foils were incorporated into the circuit laminate materials and some issues resulted from how certain circuit fabrication processes impacted the properties of the resistive material. Fortunately, as resistive foil technology has matured, present-day circuit laminate materials with planar resistors achieve consistent resistor values, with minimal changes in those values when subjected to laminate and circuit fabrication processes.

Resistive foils have long been characterized in terms of their nominal surface resistance (R_S) values, or the amount of resistance exhibited by a nominal surface area of the material, such as ohm/square. Common R_S values for resistive foils include 25, 50, and 100 ohm/square, and, in some cases, 10 and 250 ohm/square. When designing circuits with these resistive foils, a simple relationship can be applied to determine the design resistance value of a planar resistor: the length is divided by the width and then multiplied by the surface resistance of the resistive foil material, where the length and the

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width are the dimensions of the planar resistor used in a design. Other details concerning these resistive foils and how they translate into resistors can be found by visiting the website for suppliers of resistive foils, such as Ohmega Technologies and Ticer Technologies. Ticer offers a close look at its embedded resistor-conductor material and how the reliability and consistency of such materials have been applied to many critical electronic applications, including in many medical electronic devices, with good results.

Using PCB materials with resistive foils to fabricate circuits with planar resistors is fairly straightforward. A circuit pattern is first imaged and etched on the PCB material. In areas where conductive copper has been etched away from the PCB, resistive foil material will be exposed at the surface. This exposed resistive material is then chemically removed. Next, a photoresist is applied to protect the circuit pattern and to have selective openings imaged in the photoresist to define resistors. The copper is then etched in the selectively open areas of the photoresist to expose the resistive material in just those areas. The photoresist layer is then removed so that planar resistors remain formed between copper conductors, as shown by the illustration in Figure 1.

The nominal resistive values of these resistive foils tend to shift somewhat predictably during the process of manufacturing a PCB laminate, and designers should be aware that nominal values for the material may be somewhat different than the actual design values. For example, for a common RF/microwave circuit material with resistive foil that is based on polytetrafluoroethylene (PTFE), the nominal values of the foil change from 25, 50, and 100 ohm/square to 27, 60, and 157 ohm/square, respectively. A circuit designer should consult their material supplier to ensure they are aware of the effective resistive values to use for a given circuit material with planar resistors. Depending upon how a laminate is made, there may be very little difference between the nominal and the design resistive values, although the safe design strategy is to check with the material supplier.

Resistance tolerance for resistors formed from these resistive films can be well controlled, although there are some dependencies in achieving tight tolerance. For example, the physical size of the resistor will have an impact on resistance tolerance, with larger resistors formed from resistive films typically being capable of attaining much tighter resistance tolerance than smaller resistors formed from resistive films. In a study evaluating planar resistors of different sizes based on the commercial PTFE-based circuit material noted earlier, extremely good tolerance results were achieved with medium to large planar resistors from re-

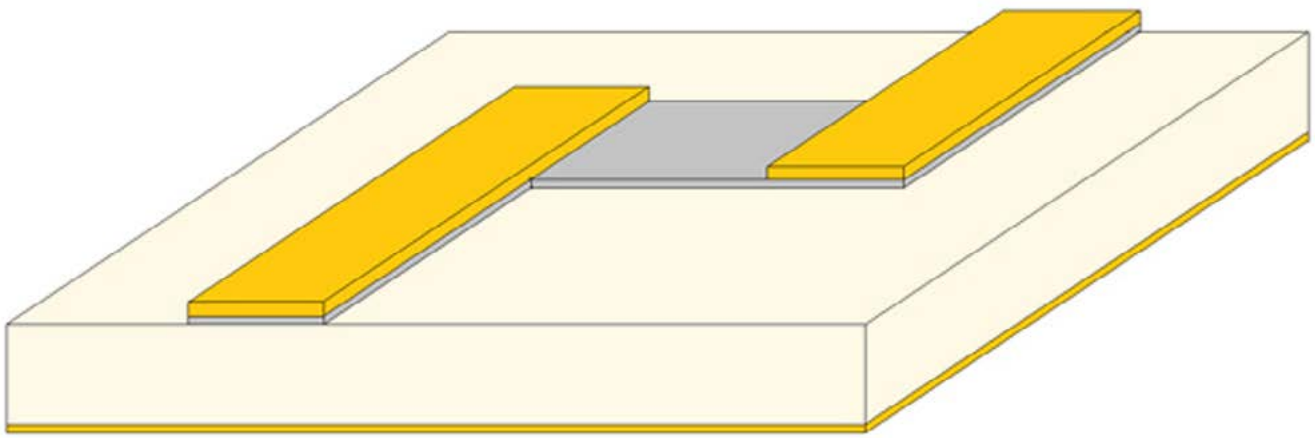

Figure 1: A portion of a PCB shows how planar resistor technology is used to form a resistor (the grey material) between copper conductors.

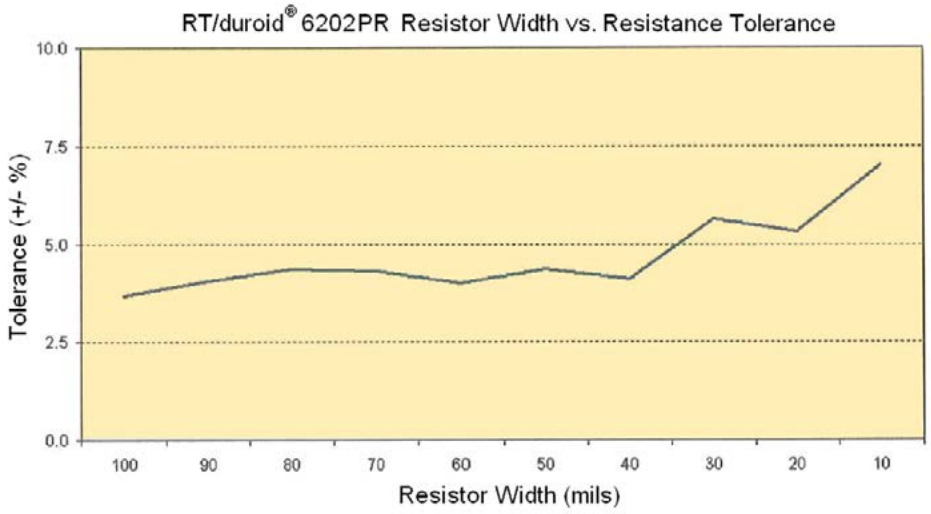

Figure 2: Common PTFE-based high-frequency laminate with planar resistors formed of resistive film show the tight resistor tolerances that are possible.

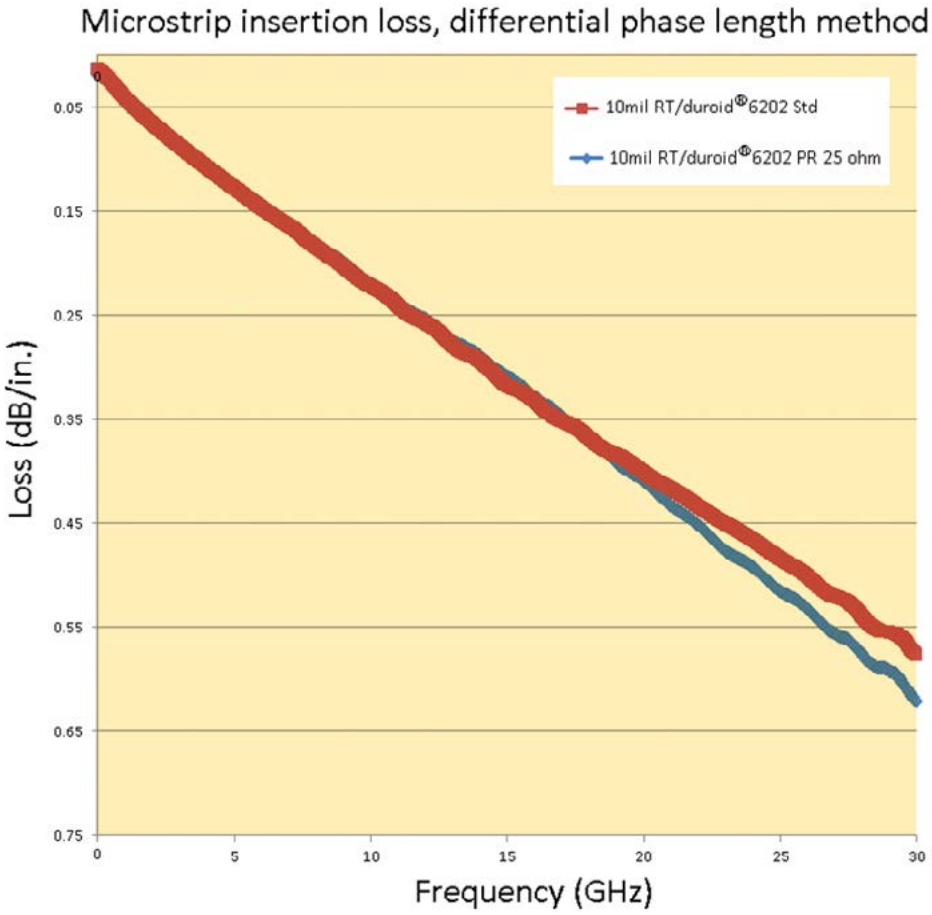

Figure 3: Plots comparing the insertion loss of similar microstrip circuits fabricated on PTFE-based laminates with and without planar resistors.

sistive film and good tolerance results were obtained with relatively small resistors. Figure 2 shows the results of this study for the PTFE-based laminate with resistive film, with values for resistance tolerance plotted as a function of resistor width.

The resistor tolerance values shown in Figure 2 are considered quite good. Surface-mount resistors commonly used in the industry typically have a resistor tolerance of ±10% while higher-quality discrete resistors typically have a resistor tolerance of ±5%.

Insertion loss is often a concern with high-frequency circuit laminates, in particular for laminates with resistive films and planar resistors. Such laminates with resistive films are often used in fabricating RF/microwave power dividers/combiners and such circuits must minimize insertion loss, especially when called upon to handle high signal power levels. Excessive insertion loss in high-frequency circuits that handle high power levels will result in unwanted temperature rises within the power divider/combiner circuit, which can be a destructive mechanism for the circuit.

To better understand the impact of planar resistor technology on the insertion-loss performance of high-frequency circuit materials, insertion-loss testing was recently performed on a standard PTFE-based high-frequency circuit laminate with and without the resistive film and the planar resistors. The materials were evaluated by means of a simple microstrip transmission-line circuit pattern using the differential length test method. Figure 3 shows the results, using laminates with the same copper conductor material and with and without the resistive film and the planar resistors. As the plots of loss versus frequency show, the insertion-loss characteristics are quite similar for the 10-mil circuit laminates, whether or not they include the resistive film and the planar resistors, leading to the conclusion that the resistive layer does not have a significant impact on the circuit material's insertion loss.

Low-loss, high-frequency circuit materials with planar resistor technology have at times been plagued by differences in insertion-loss performance for parts within a circuit build, with some parts showing significantly higher insertion loss than others. Because this did not occur on a regular basis, the cause for deviations in insertion-loss performance was not found for some time.

One theory proposed that if a circuit panel was relatively thin, any mishandling of the circuit laminate could cause microfractures in the laminate's resistive layer and copper, but this was never proven. In another case, an event revealed some circuits with elevated insertion loss within a build of other circuits with normal insertion loss. After an investigation, it was discovered that poor etching quality could result in a significant difference in insertion loss.

When viewed as a cross-section, a copper conductor typically has a trapezoidal shape, due to the standard types of copper etching processes used as part of PCB fabrication. For most high-frequency designs, this trapezoidal shape typically has minimal impact on insertion-loss performance. However, for a circuit material with resistive foil, the trapezoidal shape may result in higher insertion loss than expected. To explore this concern, evaluations were performed by fabricating microstrip transmission lines on high-frequency laminates and pur-

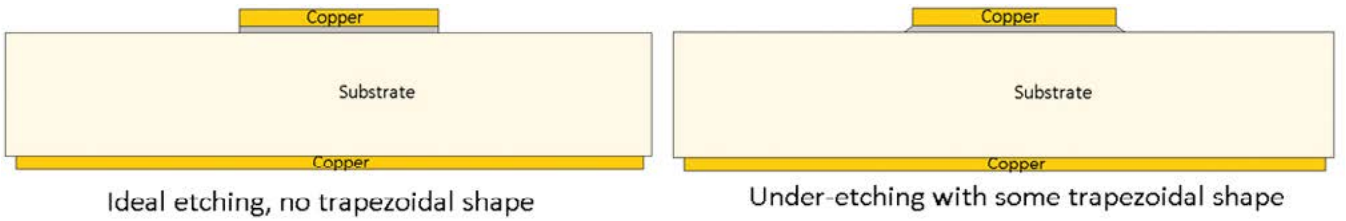

Figure 4: Cross-sectional views of microstrip circuits show where the etching is ideal (left) and where an underetched condition leads to severity in the trapezoidal shape (right).

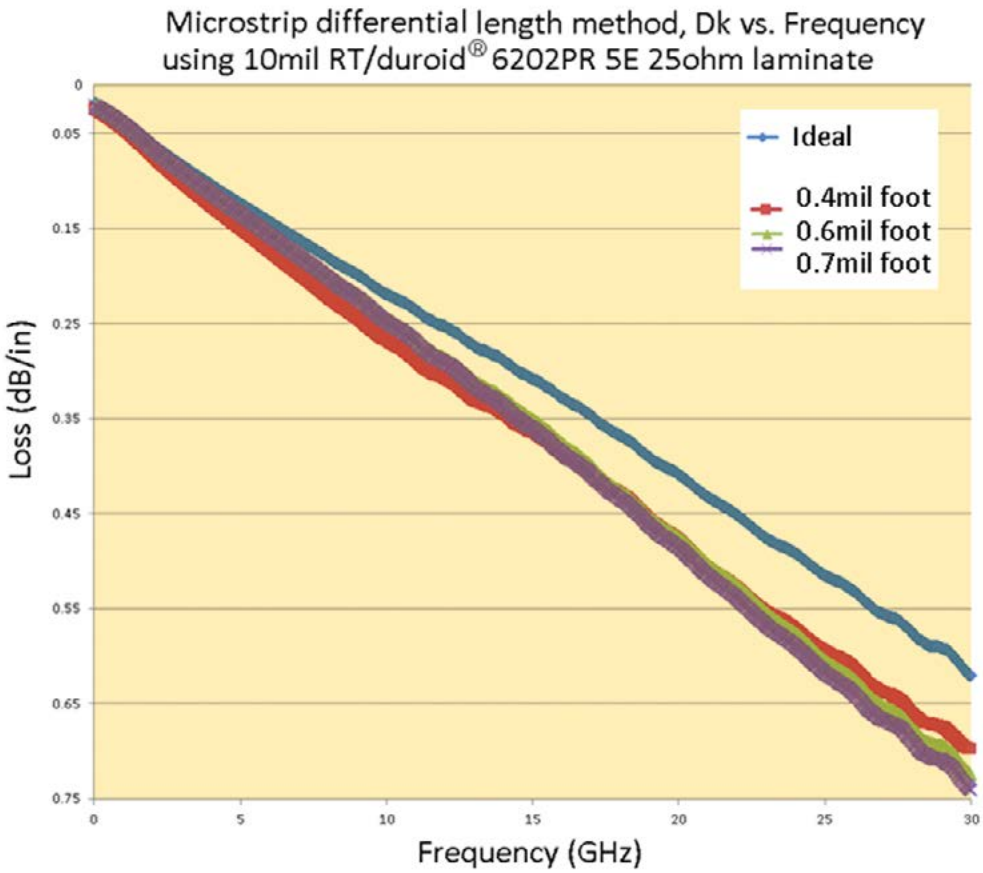

Figure 5: Microstrip insertion loss comparisons of circuits made on the same PTFE-based high-frequency materials with planar resistors and with varying etching quality.

posely underetching the conductors to cause different levels of severity in the trapezoidal shape, as shown in Figure 4.

These evaluations of the trapezoidal shapes involved a 10-mil-thick substrate, a high-frequency PTFE-based circuit material with a 25-ohm planar resistive layer. Circuits were processed under a number of different conditions, with the intent to create trapezoidal shapes with varying severity. Unfortunately, the differences in trapezoidal shapes were not large, and some circuits were found to be near ideal while others had trapezoidal shapes oversized by 0.4, 0.6, and 0.7 mils at the foot of the conductor on each side. As Figure 5 shows, these differences in trapezoidal shapes resulted in only small differences in insertion loss, notably when compared to the near-ideal circuits.

Although the trend in Figure 5 corresponds with the theory that a more severe trapezoidal shape would result in higher insertion loss, the differences in the trapezoidal shape were not significant and the insertion loss differences were also considered minor. In general, the study warns of the need for concern with etching quality when using laminate materials with resistive foils and planar resistors, but it is not clear how severe the etching quality must be affected before it impacts the insertion-loss performance of a circuit laminate with planar resistors. **PCB**

John Coonrod is a market development engineer for Rogers Corporation, Advanced Circuit Materials Division and a regular columnist for The PCB Design Magazine. To contact Coonrod, or read past columns, click here.

Key Factors Influencing Laminate Material Selection for Today's PCBs

by Steve Iketani and Brian Nelson
SANMINA-SCI

Ever greater miniaturization of electronic equipment and its circuitry, along with increasing data traffic rates, continuously pushes the PCB industry to improve performance. The compression of development cycle times has been ongoing for some time, but recently this has created a tsunami-like impact on PCB fabrication, especially in laminate materials. In order for design engineers to find solutions for increasing speed and signal integrity management in PCBs, they must keep up with the constant evolution of laminate materials, primarily on their loss performance attributes.

Today, we are seeing wave after wave of new materials that target improved cost as well as improved performance. Some efforts are in cost reductions at the current performance levels (Figure 1), and other entries are designed to improve performance while attempting to stay at par with existing price levels (Figure 2). These performance-enhanced issuances tend to fall into the spaces between traditional class groupings, creating a more continuous suite of laminate offerings. As a result, there are more tailored choice options for any specific design application, rather than having to select either an over or under laminate available for specification.

The source area for higher-speed materials has been rapidly widening. In the early 2000s, most higher-speed materials came from the U.S. and Japan. Today, materials are being sourced from Taiwan, Korea, Singapore, Hong Kong, and China. The companies and materials may not have the same maturity and application knowledge that the industry is accustomed to, depending upon the manufacturer, its experience, and the duration an offering has been in the market. Despite this general disadvantage, new laminate players continue to charge into the market, providing many materials of limited data and background. A large sampling of

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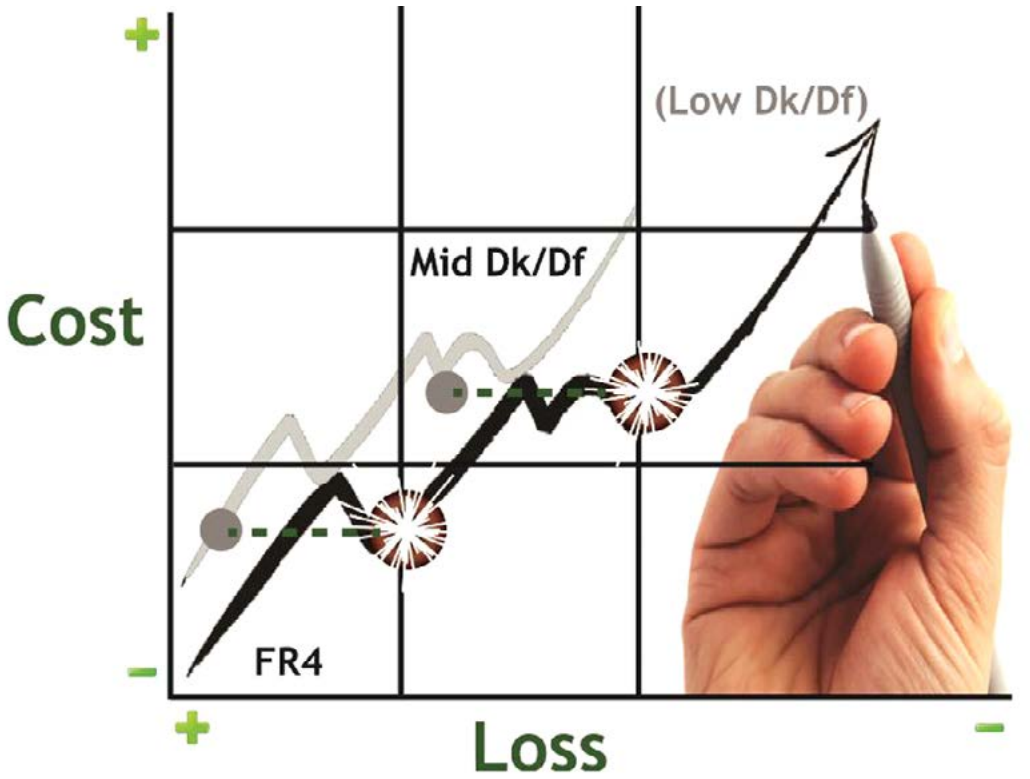

Figure 1: Some efforts address reducing costs at current performance levels.

laminates are plotted for S21 loss at 10GHz in Figure 3, which shows there are many competitive materials available with only incremental performance differences, and a nearly linear slope of options from top to bottom.

FR-4 Class Laminates

PCB material discussions often use FR-4 as a baseline for comparison of material behaviors and, especially, processability. FR-4 will continue to persist in product builds for both its thermal-mechanical strength (a valuable attribute for HDI fabs) and, of course, for its relative low cost. To continue to be in play, FR-4 also needs to provide at least acceptable limits of electrical performance coherent with transmission rates of interest. This has not been a great attribute of FR-4 historically, and our experience points to a maximum usable data rate of around 5–6 Gbps, depending on the design trace widths and routing lengths. The major impediment of using FR-4 is usually its loss tangent (Df). Yet, there have been some industry trends mitigating the loss aspect of FR-4, extending its potential use.

OEM pressure on laminate manufacturers, which began around the time of the then-new requirement to withstand lead-free assembly solder excursions, lead to some other concurrent enhancements and opened up a subclass within a class: FR-4 resins modified and/or blended in a manner that resulted in some achieving as much as 1/3 reductions in rated Df compared to traditional FR-4s. These select offerings continue in the market, as they present Df improvements at measurably less cost than mid-Dk/Df class entrants, although these modified FR-4s do not enjoy much, if any, of the dielectric constant enhancements of the mid-Dk/Df class.

Even more to this point is the impact of halogen-free on the Df of FR-4. The change is from brominated flame retardants to non-brominated replacements that incidentally require lower content within the resin for effectiveness, that being the ability to conform and certify to

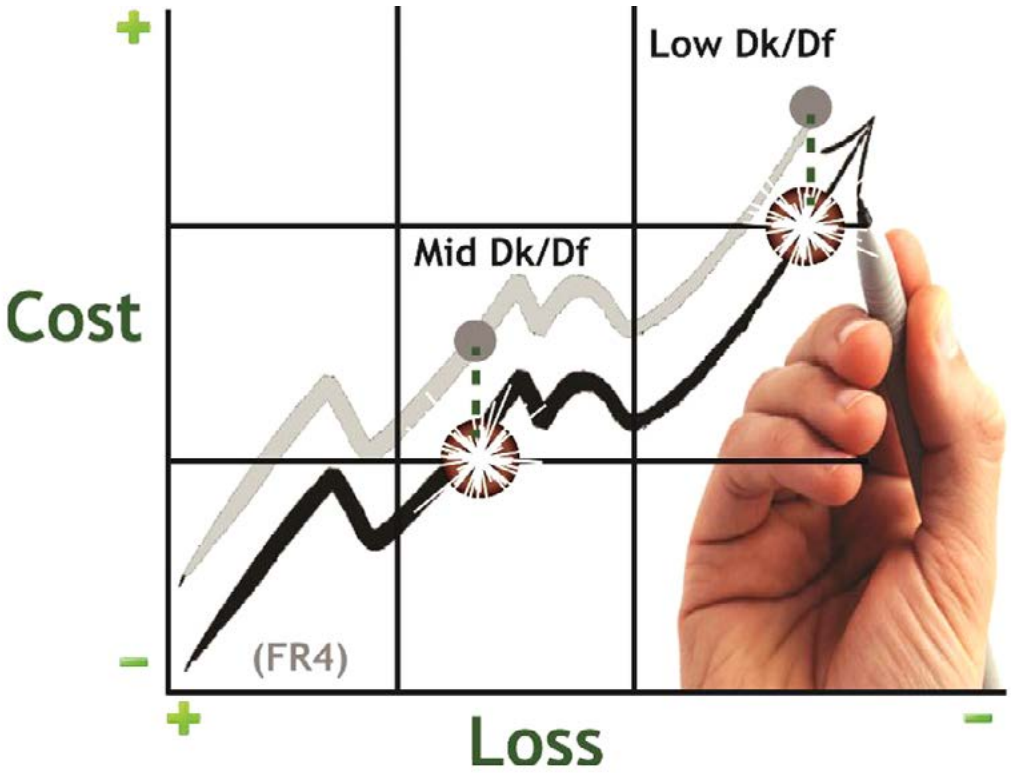

Figure 2: Other efforts focus on increasing performance while staying at today's price point.

UL94VO flame. This flame-retardant change has a measurable impact on Df. Many have taken note of halogen-free FR-4s, with Df ratings in the range of 0.010–0.016 and at measurably lower cost than many of the mid-Dk/Df class materials. Ultimately, the mid-Dk/Df materials have loss tangents available that are lower still, well down into the 0.008 range, but at an appreciable cost premium.

Financial budgets, as well as loss budgets, tend to dictate the want and feasibility of using lowered Df FR-4s as opposed to opting into a mid Dk/Df material. As cost is always a focal point, most designs opt for the least costly laminate that will deliver the performance attributes needed for that design application. Using over-engineered material for a design application is more often the fault of market offerings forcing designs to over-buy on unneeded attributes in order to acquire the needed ones. As the material market continues to fatten out its class offerings, using over-engineered materials becomes less necessary. This is further demonstrated by the limited but available option of acquiring select lead-free FR-4 items on spread weave glass styles. As the primary benefit of these styles has been mitigation of differential impedance timing skew, these FR-4 offerings are targeting a specific performance aspect, whereas before these premium glass styles were only available bundled with higher performance resin systems.

Lower-profile copper options, those smoother than reverse-treated foil (RTF), have not really appeared in FR-4s. We believe this is because greater trace loss benefit can be realized by investing in other lower-Df resin systems rather than using cost premiums to clad relatively lossy FR-4 with finely surfaced coppers. Lead-free FR-4s also enjoy regular use in high-speed applications as part of stackup hybridization, reducing cost by being relegated to power, ground, analog and other non-critical layers, while often improving the overall thermal-mechanical performance compared to all high-performance material stackups.

Mid-Dk/Df Class Laminates

There is even a more dynamic mid-Dk/Df market at present. Mid-Dk/Df is defined here as having a dielectric constant measurably lower than FR-4, meaning at or below 4.0 and a Df rating in the range of 0.007–0.013, with a number of entries rated at or below 0.010. This class of materials has existed since the issuance of GE's Getek circa 1988, which was followed by Park-Nelco's N4000-13 and its equivalent competitor materials. Nelco also added low-Dk/Df options to N4000-13, as did several of its competitors over time.

Changes to this class came fast once RoHS dictates were being adopted. These are highly modified epoxy-based systems, some blended with cyanate esters, PPEs, PPOs and other proprietary content to achieve their performance targets. These now long, complex molecules were not proving very adaptable to the elevated temperatures of lead-free assembly and their impact on CTE-Z. Modifications were again needed and established mid Dk/Df players did just that, but only incrementally to protect their existing resin UL qualifications, which would be lost and require a new qualification cycle if UL Labs were to determine that a resin had changed to the degree of designating it as a new system.

In many ways, this hamstrings the laminators in industry-critical efforts to improve resin systems. Once a resin system formula has been locked down, it takes about a year for a laminator to get that new product through laminate UL, and the multi-months-long fabricator UL qualification extends that time even further. So, pressures of time-to-market and return on investment can run very counter to the need to advance a resin system beyond some limited scope despite the need for a fuller reinvention.

The market was able to manage for a few years, but HDI has become more complicated, BGA pitches smaller, and plated over via-in-pad and sequentially laminated build-up boards' designs are much more prevalent today. The need to cross that UL line has been made evident and several laminate suppliers have responded with new, more robust and performance-improved systems. Not only have they been addressing the thermal-mechanical requirements, but they have also been able to chip away at bettering

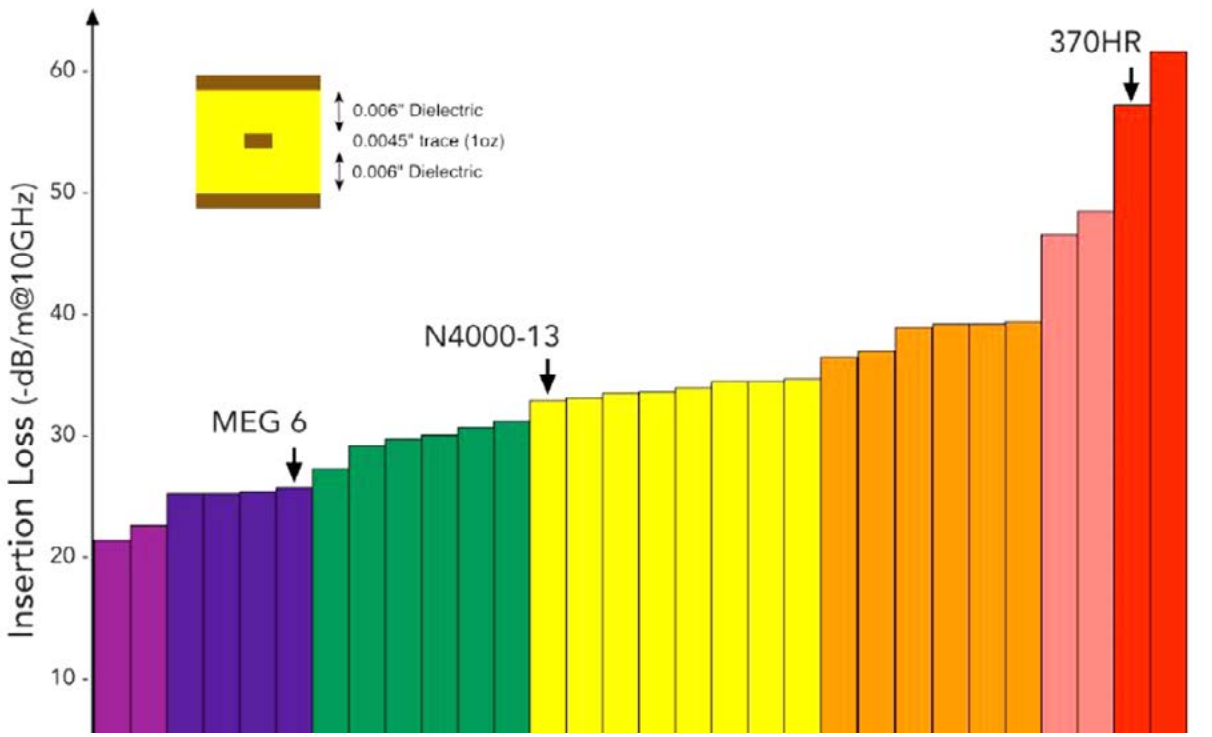

Figure 3: A variety of competitive materials are available, with only incremental differences.

Df values and have moved into more expansive options of spread weaves and copper smoothness offerings, as well as leveraging new supplier sources for lower Dk/Df glass types.

All these changes have enabled new class within a class, a spate of mid-Dk/Df materials measurably above the traditional ones but still situated below the cost and performance absolutes of the ultra-premium low-Dk/Df class. The traditional mid-Dk/Df materials were showing some good use in the 5–10 Gbps space, but running short of really supporting the upper end of that range, forcing some designs into over-specifying of materials until these new issues started appearing. The new mid-Dk/Df+ class is targeting use as fast as 12.5 Gbps depending on trace widths and routing lengths. This in turn has put pressure on the low-Dk/Df class of materials to either reduce their cost as-is or create better performance versions to satisfy the ramping development of 20–25 Gbps and faster designs. Not surprisingly, both actions are taking place now.

Low-Dk/Df Class Laminates

To better understand the low-Dk/Df class of materials, we define them as having Dk values at or below 3.7 and Df ratings at or below 0.005. A number of the mid-Dk/Df materials can easily make this Dk range if enhanced with low-Dk glass, but not while also in the range of Df. These two values together then define a distinct class. The present standard bearers are Panasonic's Megtron-6 and, to a lesser extent, the Rogers 4000 series of ceramic hydrocarbons. But there are more players today and many more in the queue and coming.

The thermal-mechanical behavior of these materials is always important as they are often relegated to very complex, HDI designs and so must be able to endure multiple lamination cycles at lead-free temperatures, which is quite challenging; it is very difficult for laminators to concoct complex molecules that deliver very high electrical performance while remaining mechanically stable and robust. All the materials of this class have proprietary resin formulations, so it is not possible for us to know their entire makeup, although at the farthest end, most have measurable content of PTFE (e.g., Rogers Duroids, Taconic, etc.).

Cost always plays a big part in any product design, so the PTFE-laden materials are still limited players, although we're seeing some very large platform boards experimenting with PTFE-based laminates for the sake of mitigating attenuation over traces on the order of about a meter. But these are 25+ Gbps R&D designs and not what is being built regularly today. Product in the 8–12.5 Gbps space has given Megtron-6 much of its market. Targeted transmission rates have been increasing toward 20–25+Gbps, thus driving the need for even lower-loss materials, most preferably ones that do not have the high cost and processing challenges of PTFEs.

A number of these have been introduced in recent quarters and are under evaluation. Performance claims are just that, always warranting independent testing and measurement. We are especially interested in seeing how any high-end materials behave, as testing clicks through frequencies of, 5, 10, 12.5 GHz or more and how well they survive the rigors of modern HDI fabrication and assembly processes. Also, former background testing is often front and center today, with requirements of CAF, insulation resistance and the like being demand items and significant filters of acceptance for a number of OEM industries.

Overall, as a fabricator, we are very encouraged to see such a huge flurry of new and promising laminates entering the market and are optimistic laminators will continue providing answers to our most pressing needs and demands of signal integrity and speed. **PCB**

This article originally appeared in the September 2013 issue of *The PCB Design Magazine*.

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Ultra-flat and Almost No Profile ED-Copper Foils for High-Speed Digital PCBs

by Julie Mouzon, Jérôme Petry and Laurence Vast
CIRCUIT FOIL LUXEMBOURG

Abstract

Copper surface roughness has become a significant factor that influences conductor loss in high-speed PCBs, particularly for signals above the 10 GHz range. Surface roughness is also an important consideration for etching very narrow-pitch HDI applications.

A new type of ED copper foil achieves a very smooth surface. Specific ultra-flat, zinc-free, arsenic-free treatments with the highest density and uniformity are being applied on such topographies. This significant increase in active contact surface provides secure bond strength to a large number of proprietary low- and very low-loss resin systems. The reduction of the foil's treatment profile has essential advantages, since insertion loss is improved, therefore allowing new opportunities in the antenna and high-speed digital arena.

Introduction

As our planet becomes more interconnected, the infrastructure needed to capture and work with increasing amounts of data must respond and deliver faster results to more users than ever before. Studies foresee that global data center traffic will increase four-fold over the next years and six-fold for global cloud traffic[1].

In order to cope with an increased demand for improved resin systems with better electrical properties, many new dielectrics have already been introduced to the market, and many others are at their final development stage.

BPA predicts for the period between 2012 and 2018[2] (Table 1).

Several publications have shown that with increasing frequencies, overall transmission losses will rise[3]. Microwave designers minimize conductor losses to achieve the required

Df @ 10 GHz	<0.010	<0.005	0.003<X<0.0010
	Tier 3&4	Tier 5&6	Tier 3-6
2012	9027	7639	16666
2015	11053	7810	18863
2018	13544	8090	21634

Table 1: Low-loss CCL surface in 1000 m².

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impedance by using wider conductors and larger gaps. In digital designs, limitations of line widths restrict this freedom of design[4].

When the depth of penetration, or "skin depth," of the electromagnetic field exceeds the root-mean-square roughness height, the influence of roughness on loss is minimal. With increasing frequency, the skin depth becomes smaller and currents flow near the surface, following the contour of that surface and thus resulting in an increased resistance because of the additional distance the currents must flow. At the highest frequencies, the depth of the penetration is much smaller than the roughness height and the additional loss caused by the roughness becomes almost independent of the frequency. At 10 GHz, the skin effect of copper is below 1 µm.

The reduction of the foil's treatment profile has essential advantages since conductor loss is widely reduced and therefore allowing new opportunities in the (very) high-speed sector.

Methodology and Results

IPC-4562 defines three major classes for roughness profiles, irrespective of the foil's thickness. Below 5.1 µm (200 µin) is defined as "very low profile." However, this definition is behind the industrial progress.

Another gap is found among definitions of Rz since Rz ISO is not identical to Rz JIS. For very low roughness, this difference is significant and close to 20–25%.

The smoother the roughness, the higher the risk for reaching erroneous conclusions by measuring with a contact profilometer, as required by IPC-4562. A standardized contactless measurement is needed.

Figure 1 illustrates the existing IPC classification together with our internal guideline including such smoother roughness profile types:

Copper foil surface roughness from microsections along with a digital translation into a pixel mapping for calculating the foil's profile is currently investigated[5].

In order to significantly reduce the foil's profile, a new ED copper foil type called BF foil was developed. Prior treatment, such foils have a roughness Rz (ISO) of ~1 µm and less than 2.5 µm after treatment, as shown by Figure 2.

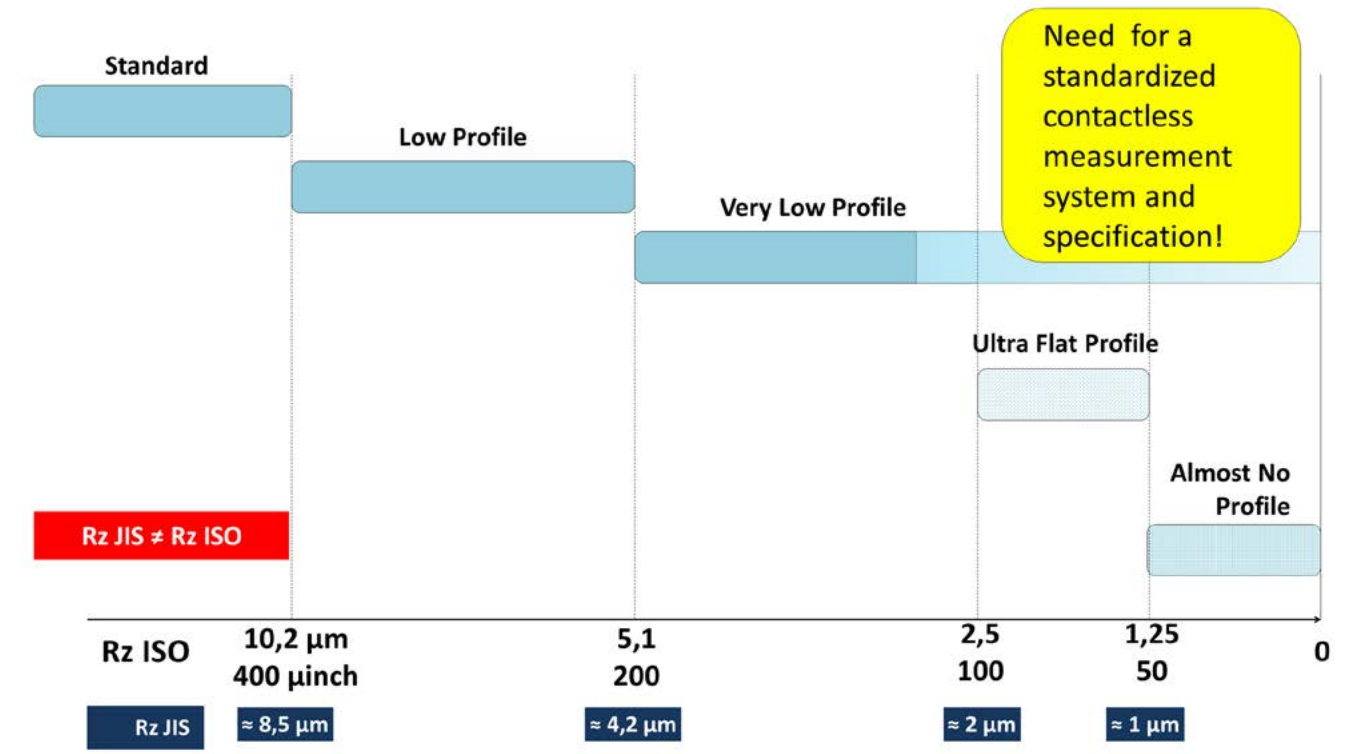

Figure 1: Roughness definitions and revised classification.

With an extremely dense and very uniform treatment, the new BF foil types offer a large contact area to the dielectrics. This is illustrated in Figure 3 by treatment imprints after copper etching.

From a mechanical point of view, this foil type behaves like any regular copper foil.

Such foils are produced down to 9 µm thickness (1/4 oz./ft²). Although this level of thickness is not yet needed for high-speed digital applications, it will likely be necessary for sequential build-up HDI boards for mobile devices and for IC packages.

A large number of new resin systems with low- to very low-loss properties (with Df data ranging from 0.003–0.010 @ 10 GHz) have been introduced in the last few months. Since their requirements and limitations are very different in view of their final application, Figure 4 illustrates an internal classification and suggestions for the market, along with the treated foil's side roughness and its name.

With several highly filled resin systems, mechanical anchorage of the treatment dendrites is the leading factor for bonding securely. With the new BF foil type, the reduced roughness profile compensates the mechanical anchorage by a much higher contact area. This is also improved because of a much higher uniformity of the fine dendritic treatment. Figure 5 documents typical peel strength ranges on a certain number of copper clad laminates.

A further reduction of the foil's roughness profile is currently investigated with so-called almost no profile foils (BF-ANP foil).

In order to maintain secure bond strength, such ANP (or profile-free Cu-foils) are combined with a very thin high TG primer coating layer. This potentially next generation for very high-speed applications is illustrated by Figure 6.

The cross-section of Figure 6 illustrates the absence of the typical nodular treated side. By combining with a proprietary halogen-free epoxy-based primer coating, peel strength could

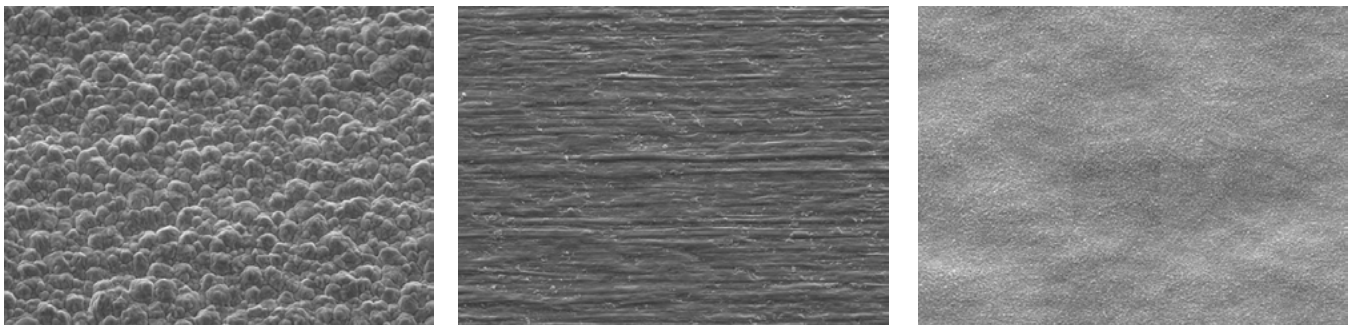

Figure 2: Surface comparison prior treatment. Left: Matte side: Rz ~ 7 µ. Middle: Reverse (shiny) side: Rz ~ 2.5 µ. Right: New flat profile type (BF foil) with Rz ~ 1 µ.

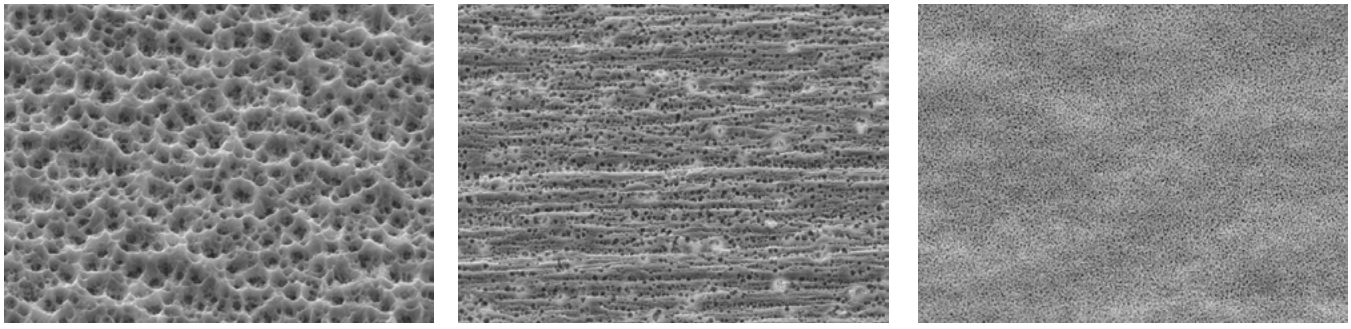

Figure 3: Treatment imprints after etching. Left: Matte side: Rz ~ 7 µ. Middle: Reverse (shiny) side: Rz ~ 4 µ. Right: New flat profile type (BF) foil with Rz ~ 2 µ.

			Lower frequencies (> 10 GHz)			Higher frequencies (> 10 GHz)		
Df @ 10 GHz	Resin type	Application	Recommended Cu foil type	Rz (ISO)	Product Name	Recommended Cu foil type	Rz (ISO)	Product Name
<0.003	PTFE and hydrocarbon resins	RF/Microwave Antenna	Low Profile	6µ	HFZ-LP	Reverse Treated Flat Profile	4µ 2µ	HFZ-B BF-HFZ
0.003 - 0.005	Very Low Loss	High Speed Digital	Flat Profile	2µ 2µ	BF-HFI-LP2 BF-TZA	Flat Profile	2µ 2µ 1.2µ	BF-HFI-LP2 BF-TZA **BF-ANP+PA**
0.005 - 0.007	Low Loss	High Speed Digital	Flat Profile	2µ	BF-TZA	Flat Profile	2µ 1.2µ	BF-TZA **BF-ANP+PA**
0.007 - 0.010	Mid Loss	Lower speed applications	Reverse Treated	4µ	TZA-B	Not applicable		

Figure 4: Low-loss resins and common applications.

Flat foil thickness		CCL1	CCL2	CCL3	CCL4	CCL5	CCL6	CCL7
	Df @ 10 GHz	0.007 - 0.010		0.005 – 0.007			< 0.005	
12µ (3/8 oz./ft²)	N/mm				0.49		0.55	
	(lb/in)				(~2.8)		(~3.2)	
18µ (1/2 oz./ft²)	N/mm	0.55	0.67	0.55	0.56	0.57	0.61	
	(lb/in)	(~3.15)	(~3.8)	(~3.15)	(~3.2)	(~3.25)	(~3.5)	
35µ (1 oz./ft²)	N/mm			0.63	0.70	0.65	0.55	~0.67
	(lb/in)			(~3.6)	(~4.0)	(~3.7)	(~3.15)	(~3.8)

Heat Resistance @ 288° C and 20s dip Condition A: PASS
POT-5h: PASS

Figure 5: Peel strength of ultra-flat foils on various low-loss laminates.

be significantly increased on a certain number of low- and very low-loss resins.

Studies and Results

In a first study carried out by Isola, the 18 µm (1/2 oz./ft²) thick ultra flat profile foil BF-TZA (Rz ISO ~2 µm) was compared to an 18 µm (1/2 oz./ft²) thick typical reverse treated TZA-B foil having a normal very low profile (Rz ISO ~ 4 µm).

Insertion loss (SET2DIL method) at 4 GHz and 8 GHz was measured and shown in Figure 8.

For very low-loss resin systems, the flat profile foil BF-TZA generates significantly lower conductor losses compared to a reverse treated foil.

The roughness profile on the bonding side of the copper foil is not the only contributing factor for conductor losses. By applying a regular innerlayer bonding treatment on the foil's shiny side, it becomes evident that gains in conductor losses from a flat profile foil are strongly attenuated by the innerlayer oxide treatment's roughness (Figure 9).

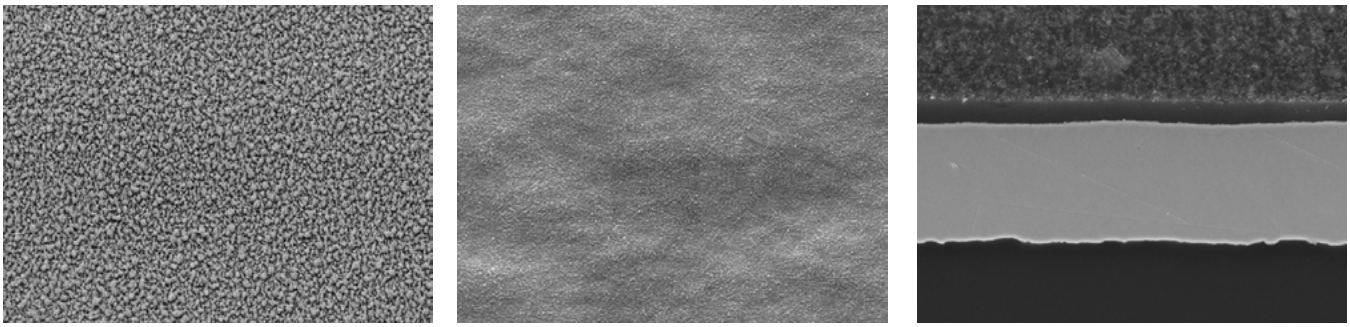

Figure 6: Almost no profile foil as next step flat profile BF foil (l); almost no-profile BF-ANP foil (center); combined with 4µ proprietary primer coating (r).

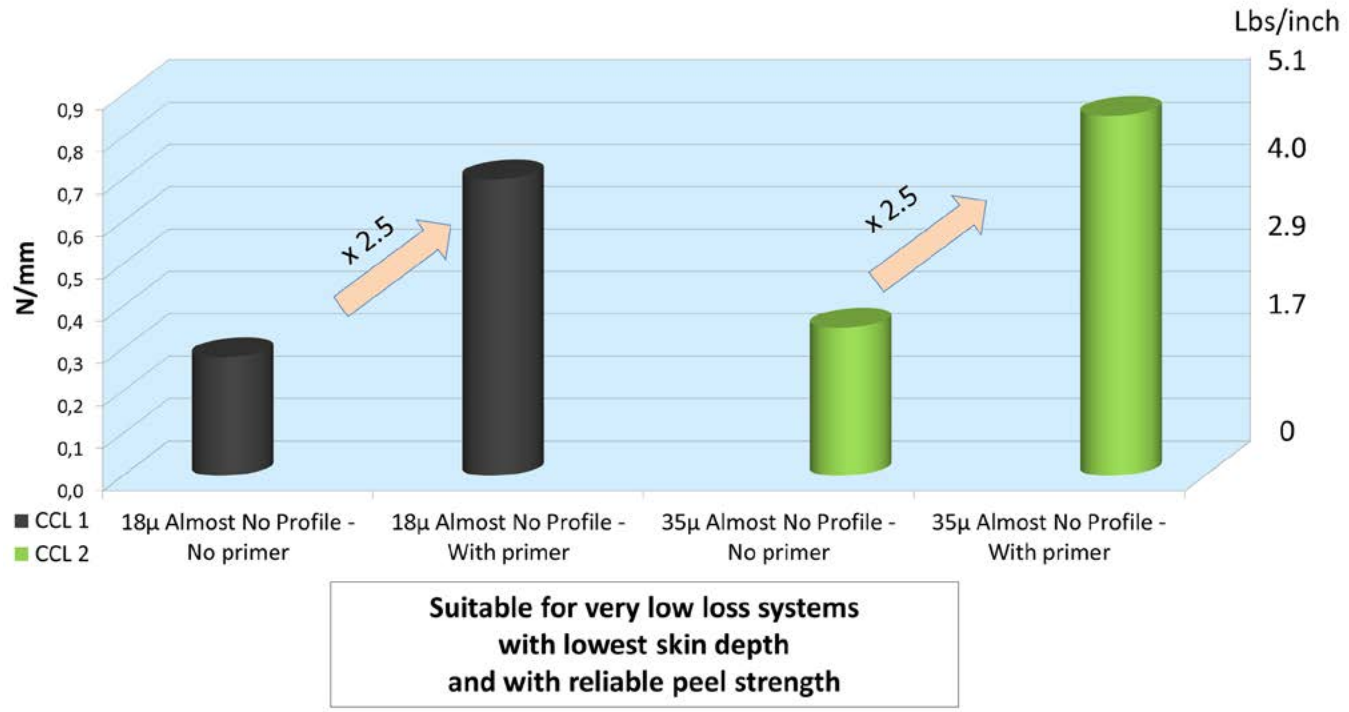

Figure 7: Peel strength of BF-ANP (almost no profile) foils combined with a primer coating.

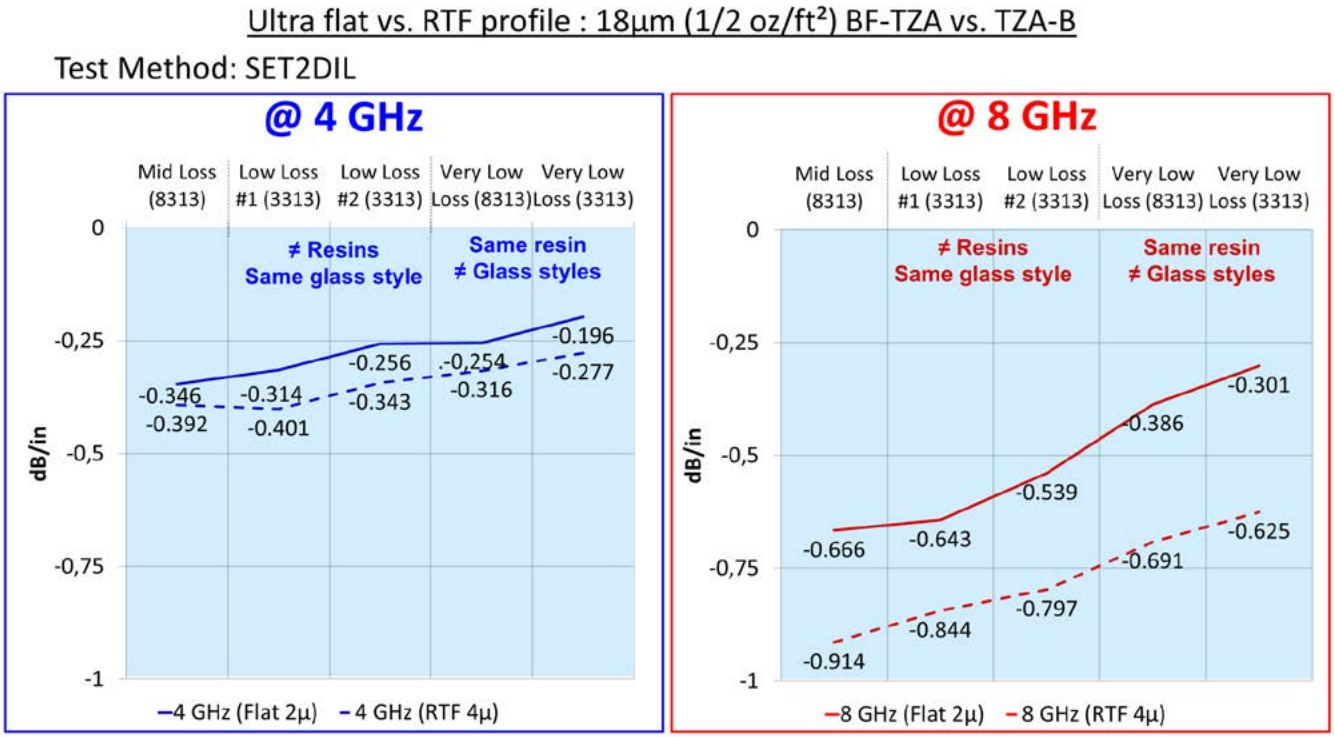

Figure 8: Insertion loss study #1.

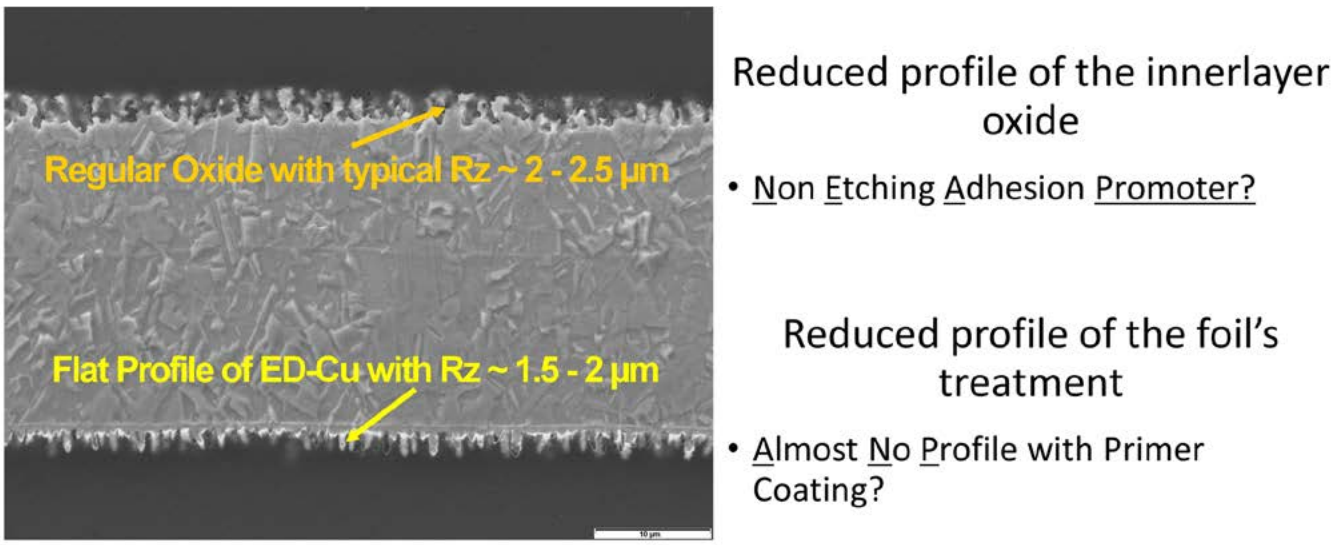

Figure 9: Innerlayer oxide on a flat profile foil.

A second study measured the impact of a flat innerlayer treatment with an 18 µm (1/2 oz./ft²) thick ultra-flat BF-HFI-LP2 foil, almost no profile copper foil with the primer coating (BF-ANP-PA) and thick reverse treated foil HFZ-B on the insertion loss.

The study was using a very low-loss resin system (Panasonic Megtron 6) for high-end applications. Details of this study are shown in Figure 10.

Based on a reference board designed by Cisco, all measurements using the Cisco S3 meth-

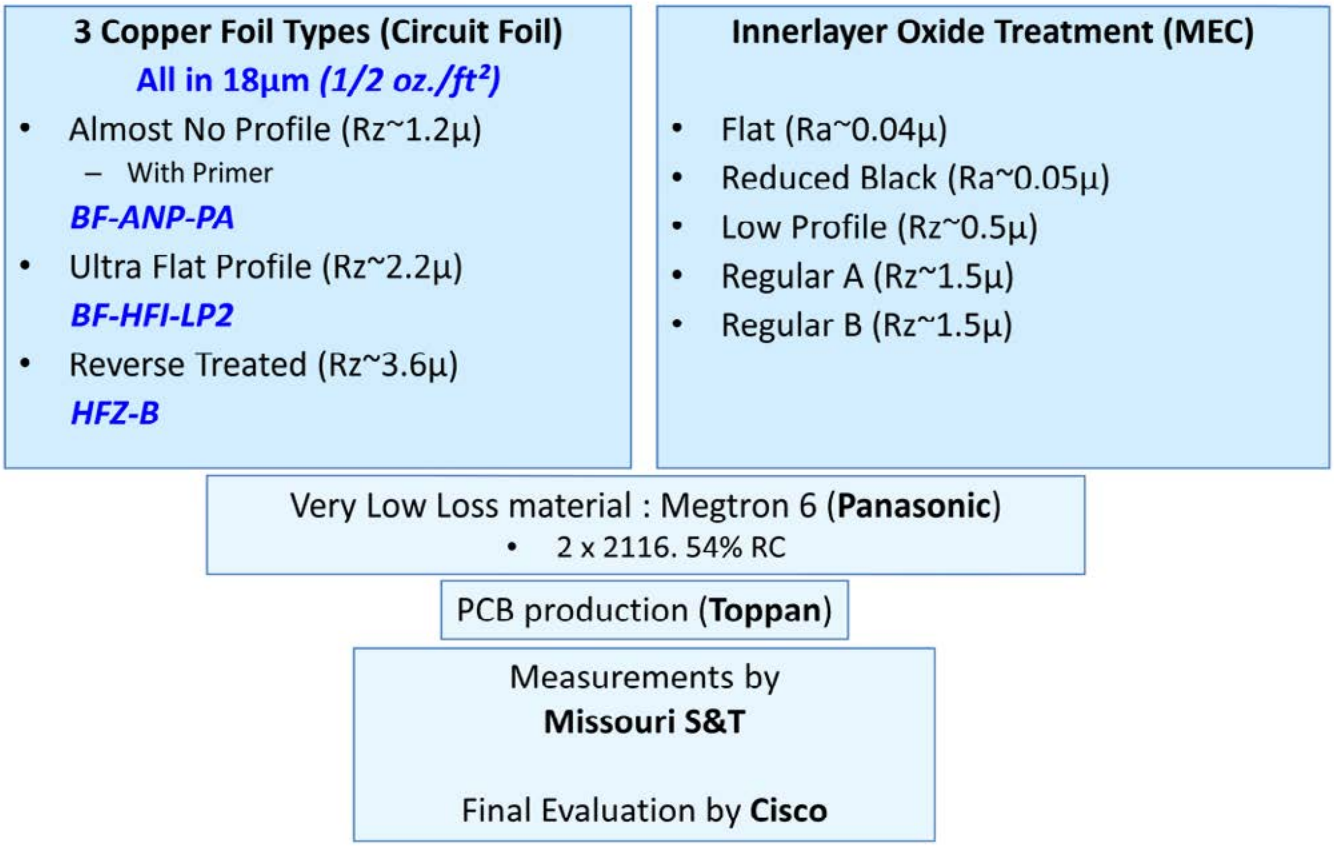

Figure 10: Insertion loss study #2.

od up to 25 GHz compare the three different copper foil profiles (Rz between ~1–1.2µ and ~3.6–4µ) and five different innerlayer oxide treatments from MEC generating significantly different roughness on the foil's shiny side.

50Ω single-ended striplines and 16-inch striplines produced the following results:

While using the same innerlayer treatment, a significant difference is measured between an ultra-flat profile foil and a conventional reverse treated copper foil.

By using the same ultra-flat copper foil, the innerlayer treatment producing a Ra of only 0.04 µm generates up to 11% lower insertion losses compared to a conventional oxide treatment with a Rz of 1.5 µm.

The losses for the primer coated ANP copper foil type were very close to the ultra-flat BF-HFI-LP2 foil, but presented higher peel strength compared to the other foil types.

Summary and Conclusions

For high-end applications using very low-loss resin chemistries, the usage of ultra-flat profile BF style copper foils is highly recommended for taking entire advantage of much lower conductor losses.

In the near future, a primer-coated, almost no profile foil (BF-ANP-PA) may contribute to higher peel strength without impacting dielectric loss.

For mid-loss resin systems, the relationship of required performance to cost is very likely the leading decision factor. **PCB**

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50 Ω single-ended stripline / Lines of 16 inches / Network Analyzer: Agilent E8364B

Same Cu - Foil

- Flat Profile Foil

Insertion Loss in dB for 16" Test Lines			
Loss	Cu	I/L Treatment	S21 @ 10 GHz (*)
Lowest	Flat Profile *BF-HFI-LP2*	Flat Oxide	- 6.81
		Red. B.O.	- 6.95
		Low Profile	- 7.01
		Reg. A	- 7.23
Highest		Reg. B	- 7.24

Same Innerlayer - Treatment

- Flat Oxide

Insertion Loss in dB for 16" Test Lines			
Loss	Cu – Foil	I/L Treat.	S21 @ 10 GHz (*)
Lowest	Flat Profile *BF-HFI-LP2*	Flat Oxide	- 6.81
	Almost No Profile *BF-ANP-PA*		- 6.96
Highest	Reverse Treated *HFZ-B*		-7. 41

(*) Average of 3 tests

Figure 11: Insertion loss results S21 @ 10 GHz.

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Breakthrough in Rechargeable Battery Technology

Researchers at the Materials and Surface Science Institute (MSSI), University of Limerick, Ireland, have made a significant breakthrough in rechargeable battery technology. An ever-increasing demand for portable electronic devices and improved technology for battery life and stability is a vital factor in device performance. The combined value of the rechargeable battery technology market is set to grow from $11.8 billion in 2010 to $53.7 billion in 2020. A research team at UL has developed a technology that more than doubles and retains the capacity of lithium-ion battery anodes even after being charged and discharged over 1,000 times.

RAINBOW TECHNOLOGY OPEN FOR BUSINESS IN THE USA IPC APEX EXPO 2014-BOOTH 1849

After successfully securing beta sites with leading electronics manufacturers in Europe and Asia for its revolutionary PCB manufacturing system, the Rainbow Process Line, Rainbow Technology Systems is seeking development partners in America.

The Rainbow Process Line

Developed over six years, the Rainbow process represents a breakthrough for the electronics industry by incorporating coating, imaging and developing of PCBs in one compact, automated unit which promises to make board production faster, easier and more profitable. One of the key advantages of the system is its ability to print fine line detail producing track and gap of 20 microns and under. As the industry drives towards increasingly finer levels of detail, the Rainbow process is already capable.

The completely self-contained unit takes up less than 20 sq.m of floor space and comes complete with its own environmentally controlled enclosure, which helps to maximize potential yields. The process is automatic, requiring minimal operator intervention and is capable of delivering up to 3 double-sided panels per minute at up to 24" x 22" standard size, ready for etching.

Central to the success of the Rainbow process is the proprietary solvent-free liquid etch resist which does not require pre-drying before imaging. Using a wet resist offers a much better adhesion to the copper than can be achieved with traditional dry film methods. Rainbow will be speaking to potential U.S. partners at this year's IPC APEX EXPO.

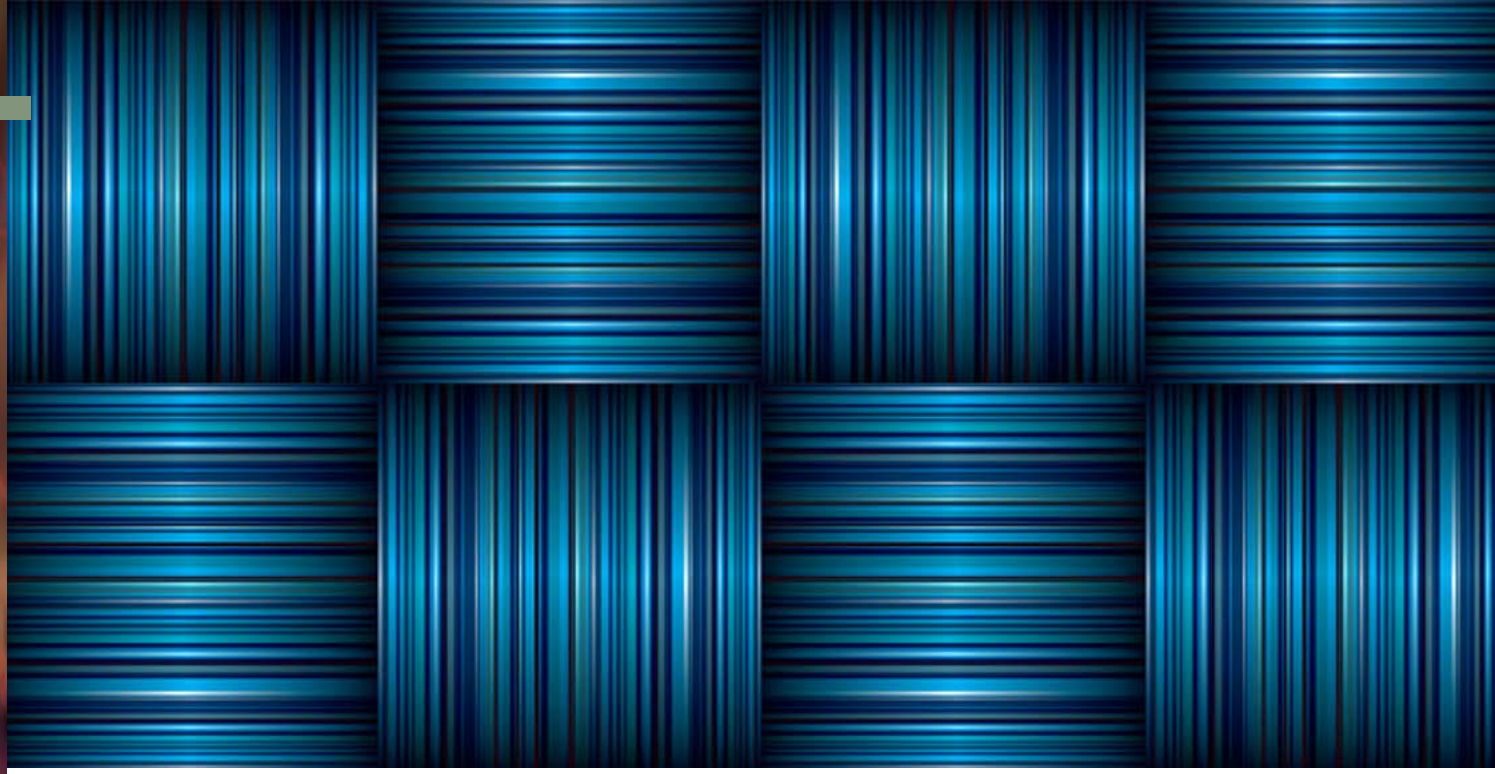
Chris O'Brien, Sales and Marketing Manager, explains: "The Rainbow Process has now evolved from the prototype stage to the building of fully functioning equipment designed for full scale production. 2014 will be a key year for us as we put the first machines through their paces in full production mode on customer's sites in Asia and Europe.


Panda Coater


Desktop Coater

In addition to the Rainbow Process Line, we are also establishing global sales of other innovative coating equipment, such as our **Panda Coater**, which puts UV curable liquid coatings onto phototools, stabilizing them and extending their useful life. We will have a Panda Coater on our stand at the show alongside our **Desktop Coater**, which can carry out the Rainbow process on a smaller scale."

For further information about the Rainbow process please visit www.rainbow-technology.com or call +44(0)141 892 3320.



Developments in Glass Yarns and Fabric Constructions

by Alun Morgan
ISOLA GROUP EUROPE

Glass fibres are nothing new; the ancient Egyptians reportedly drew coarse fibres from heat softened glass. Modern usage, however, began in the 1930s with the founding of the Owens-Corning Fiberglas Corporation and the granting in 1938 of a patent covering their commercial manufacturing process.

Fibres exhibit markedly different properties to those of their bulk parent materials. Glass fibres can exhibit tensile strengths up to 5 GPa, which is around 100x higher than that of bulk glass, the difference being attributable to the reduction of the effect of surface defects, the control of which remains an important performance parameter.

The use of woven glass fibres in PCB substrates dates back to the 1960s where they were used as a high performance replacement for paper reinforcements. Woven glass fibre provided an ideal reinforcement to complement the properties of epoxy resin systems which were being rapidly deployed in electronics by adding high tensile strength and dimensional stability to the composite material forming the substrate.

Glass fibres brought not only the properties of high tensile strength and dimensional stability but also high thermal resistance, good chemical resistance, insensitivity to moisture and of course that of being a good electrical insulator.

The process of glass fibre production remained largely unchanged over 50 years, however there have been a number of recent important developments that have enabled substrates made with woven glass fabrics to adapt to the changing requirements of circuit design. In particular changes have been necessary to accommodate microvia technology requirements, improving CAF (conductive anodic filamentation) requirements and very importantly to extending the usable frequency range of glass reinforced substrates.

To understand the developments it is useful to review the process by which woven glass fabrics are made. The process begins with a glass formulation which is tailored for a particular application. Glass is formulated mainly of sili-

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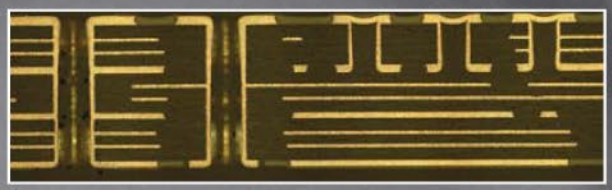

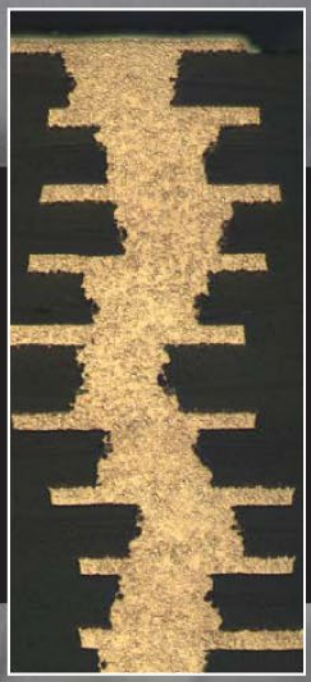

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Oxide	E-Glass	D-Glass	C-Glass	S-Glass
SiO_2	52 - 56	72 - 75	64 - 69	64 - 66
CaO	16 - 25	0 - 1	11 - 15	0 - 0.2
Al_2O_3	12 - 16	0 - 1	3 - 5	24 - 25
B_2O_3	5 - 10	21 - 24	4 - 6	0
MgO	0 - 5	0	2 - 4	9.5 - 10
$Na_2O + K_2O$	0 - 2	0 - 4	7 - 10	0 - 0.2

Table 1: Glass composition—main ingredients, by weight%.

con dioxide (Silica, SiO_2), to which varying proportions of principally metal oxides are added (Table 1).

Glass fibre reinforcements are named according to the properties imparted by these formulations, the letter designation being taken from a characteristic property: E-glass is electrical grade and has a low alkali content. It exhibits excellent electrical insulation and low moisture absorption. E-glass accounts for the majority of glass fibre production used for reinforcement. D-glass has a low dielectric constant (Dk), however its mechanical properties are not so good as E- or S-glass. C-glass is chemical glass, having very high chemical resistance and S-glass is a high-strength glass having a much higher tensile strength than that of E-glass. This list is not exhaustive and there have been recent variants having similar properties to D-glass which will be discussed later.

The glass formulation is melted in a furnace and the molten glass is then mechanically drawn into single filaments through small holes in a platinum/rhodium alloy bushing. The filaments are next gathered into bundles called strands and are then coiled onto bobbins to form a yarn (Figure 1). During the strand forming process a size is applied in order to protect the glass surface to avoid the formation of defects that would weaken the fibres.

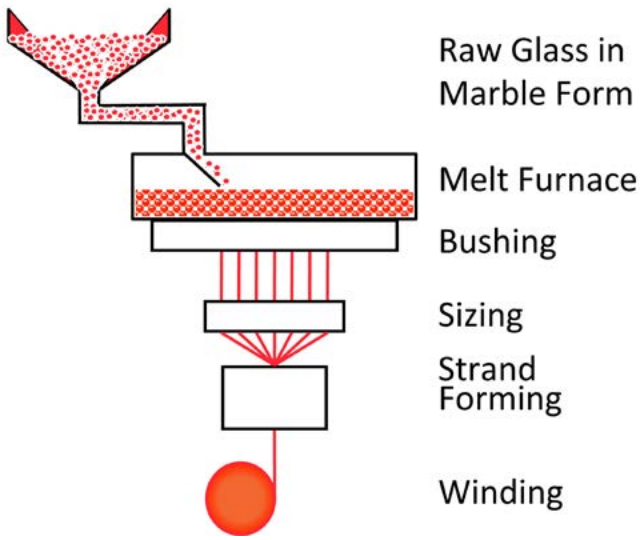


Figure 1: Glass yarn production.

The individual filaments for PCB substrate use are commonly between 5 and 9 microns in diameter and are gathered together into stands of between 204 and 408 filaments to form a yarn, see Table 2. It is interesting to note that 1 square foot of 0.062" glass fibre reinforced PCB laminate contains over 500 miles of individual glass filaments. The yarns have individual designations, shown in Figure 2.

Yarn Designation	Filament Diameter	Filaments per Strand
EC9 68 Tex	9 Microns	408
EC7 22 Tex	7 Microns	225
EC6 34 Tex	6 Microns	408
EC5 22 Tex	5 Microns	408
EC5 11 Tex	5 Microns	204

Table 2: Glass yarn common types.

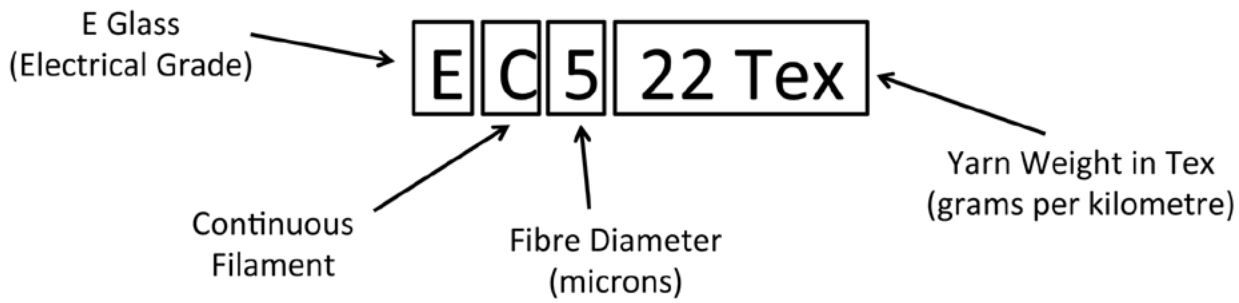


Figure 2: Glass yarn designation.

The first part of the weaving process is called warping, which is the operation through which the yarn on the bobbins is transferred to section beams at the required spacing to form the warp threads which run in the machine direction and are up to 3 kilometres in length. Depending on the total number of threads required for a given type of glass weave (style), several sectional beams are produced and consolidated in a group called a set which is the input for the slashing process where additional size is added to protect the fibres from breakage through the weaving process.

Once the loom beam is installed on the weaving loom, fabric is formed by interlacing filling yarns (picks, weft threads) orthogonal to warp threads (ends) (Figure 3); the most common interlacing of fill and warp ends (weave pattern) is plain weave although others such as basket, twill and satin are available. The woven fabric is wound onto a roll for subsequent heat cleaning to remove the size and then onto finishing operations.

In order to provide maximum adhesion of the fabric to the various resins matrices, a coupling agent (finish) is applied to the fabric by impregnating in a "finish bath"; additionally proprietary fibre spreading treatments can also be applied at this stage. The resultant plain weave fabric is shown in Figure 4.

Different yarns are combined in different combinations to weave the variety of "styles" that are subsequently used for PCB substrate production. Table 3 shows the composition of the traditional styles available.

Photographs courtesy of Isola Fabrics

Figure 3: Glass weaving process.

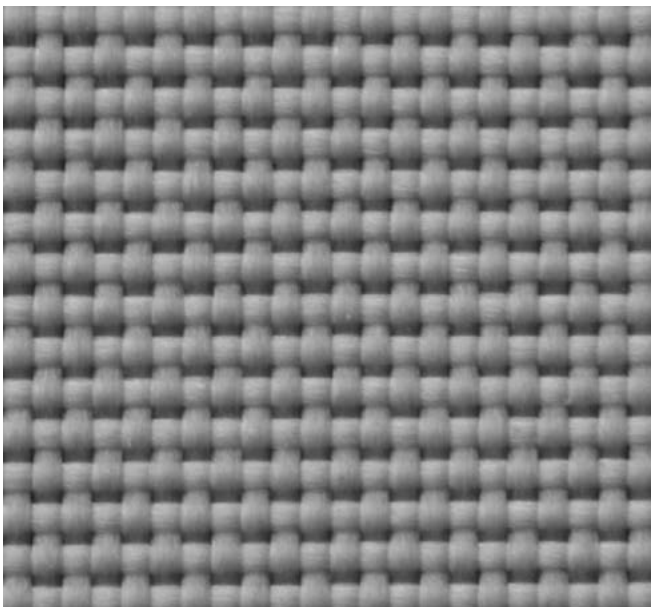


Figure 4: Plain weave fabric.

Next, we must look in detail at the woven glass fabric and to consider the inherent limitations placed on PCB performance and design. The traditional glass cloth styles and their composition were originally chosen with thickness yield, ease of manufacture and mechanical properties as the primary drivers. There was little concern at the time to consider the effects of inhomogeneity in the resultant PCB substrates, indeed this did not matter greatly in terms of the PCB technology of the day.

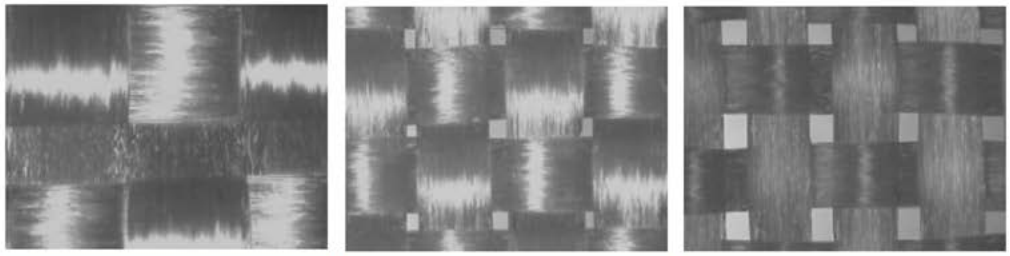
Considering that the PCB substrate is a composite material comprising a resin system and a woven glass reinforcement it is necessary to understand how the properties of the component parts affect the behaviour of the whole, bearing in mind that the macro and micro behaviour may also differ. Referring to Figures 5 and 6, the reducing density of the glass fibre matrix with decreasing thickness can be clearly seen. The picture of 106 style glass fabric in Figure 6 demonstrates that for this style over 40% of the available area is occupied with gaps in the glass fibres which will be filled with resin in the resulting substrate. The issue we must explore is the interaction of a signal transmitted on the conductive layer with the micro structure of the substrate underneath.

With conductive feature sizes decreasing these are now of the same order as the features arising from the weave pattern leading therefore to opportunities of interaction. The speed of the electrical signal, which is actually the speed of the associated electromagnetic wave, can be considered by calculating the velocity factor which is the speed at which a signal passes through the medium relative to the speed of light. The velocity factor is expressed as the reciprocal of the square root of the dielectric constant of the transmission medium.

The dielectric constant of E-glass is around 6.6, whereas the dielectric constant of a typical epoxy resin is around 3.5. From these figures we

Style	Glass Thickness (mm)	Weight (gsm)	Threads per cm	Yarn
7628	0.17	203	17.3 x 12.2	EC9 68/EC9 68
2116	0.095	104	23.6 x 22.8	EC7 22/EC7 22
2125	0.09	87	15.7 x 15.4	EC7 22/EC9 34
2113	0.079	78	23.6 x 22.0	EC7 22/EC5 11
1080	0.05	47	23.6 x 18.5	EC5 11/EC5 11
106	0.033	24	22.0 x 22.0	EC5 5.5 /EC5 5.5

Table 3: Traditional woven glass fabric styles.

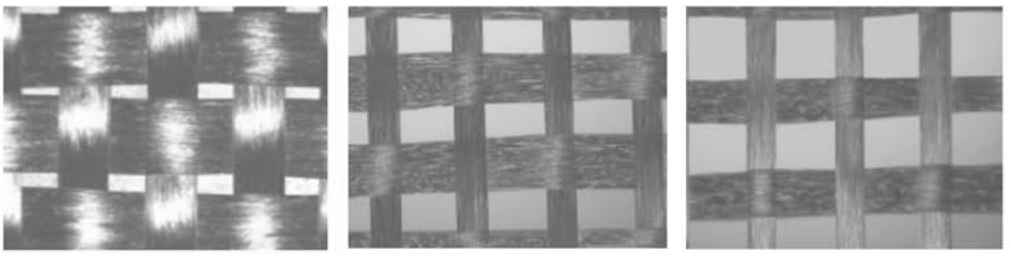


Glass Style	7628	2116	2113
Weight (grams/sq.m)	203	104	78
Thread count	17.3 x 12.2	23.6 x 22.8	23.6 x 22.0
Yarn (warp/weft)	EC9 68/EC9 68	EC7 22/EC7 22	EC7 22/EC5 11
Glass thickness (mm)	0.17	0.095	0.079
Pressed thickness* (mm)	0.18 - 0.22	0.110 - 0.125	0.085 - 0.10

* Approximate thickness yield range dependant on design, resin content and resin type.

Figure 5: Glass fabric images.

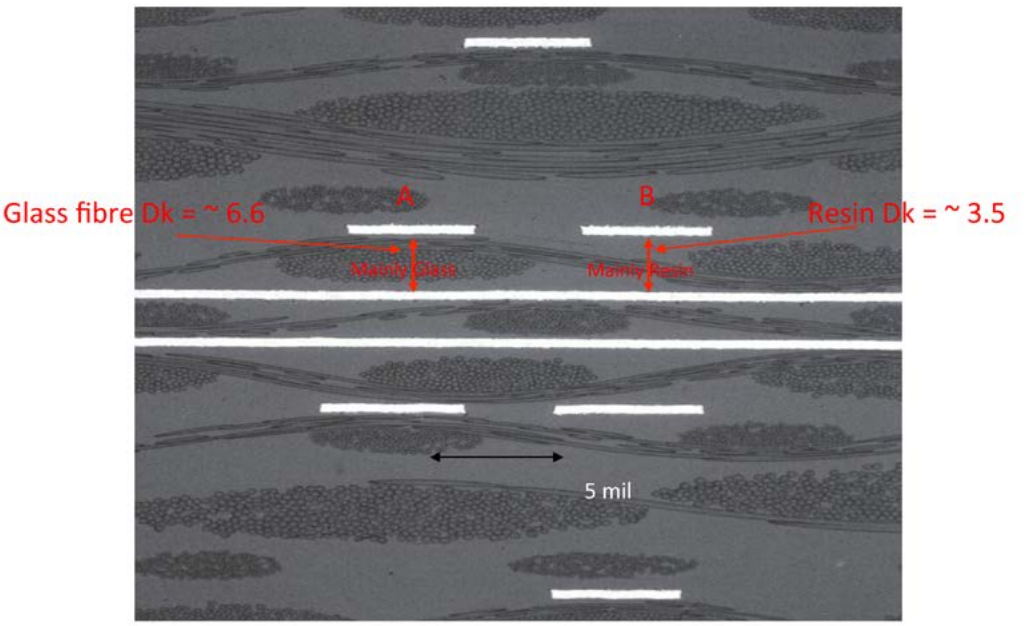
can now calculate the velocity factor for a conductor placed directly over a glass fibre yarn as 0.39x the speed of light and that of a conductor placed in area containing only resin as 0.53x the speed of light. These values represent the extremes, however the difference is massive. The use of differential pairs in signalling is very common in order to eliminate common electromagnetic noise, the transmitted information being the difference between the traces which contain equal amplitude but opposite polarity signals. It is easy to visualise the effect of the velocity factor



Glass Style	2125	1080	106
Weight (grams/sq.m)	87	47	24
Thread count	15.7 x 15.4	23.6 x 18.5	22.0 x 22.0
Yarn (warp/weft)	EC7 22/EC9 34	EC5 11/EC5 11	EC5 5.5/EC5 5.5
Glass thickness (mm)	0.09	0.05	0.033
Pressed thickness* (mm)	0.10 - 0.12	0.065 - 0.080	0.048 - 0.060

* Approximate thickness yield range dependant on design, resin content and resin type.

Figure 6: Glass fabric images.



Photomicrograph courtesy of Polar Instruments

Figure 7: Micro Dk effect on differential pair.

differences explained above on differential pairs; Figure 7 show a differential pair marked "A" and "B", the "A" trace runs directly over a glass fibre, whereas trace "B" runs over a resin rich area. The consequent signal velocities mean that these two traces cannot behave as intended as the resultant signals will arrive at their destination skewed, or out of sync. Figure 8 shows the signal from a

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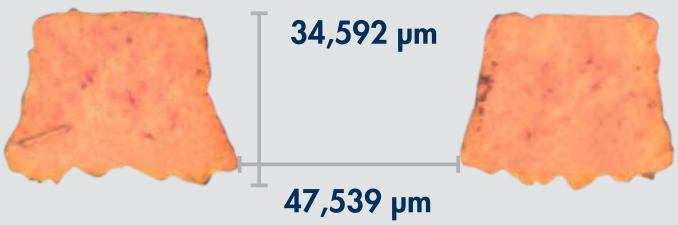

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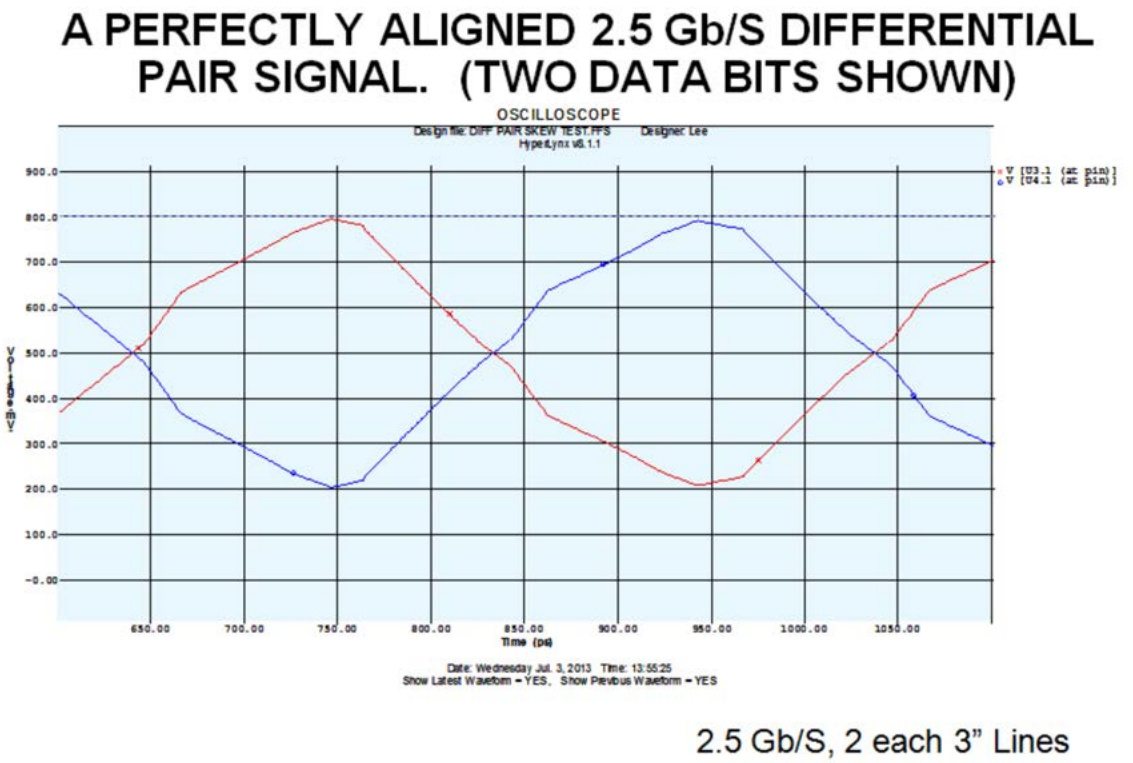


Figure 8: Eye pattern of perfectly aligned differential pair.

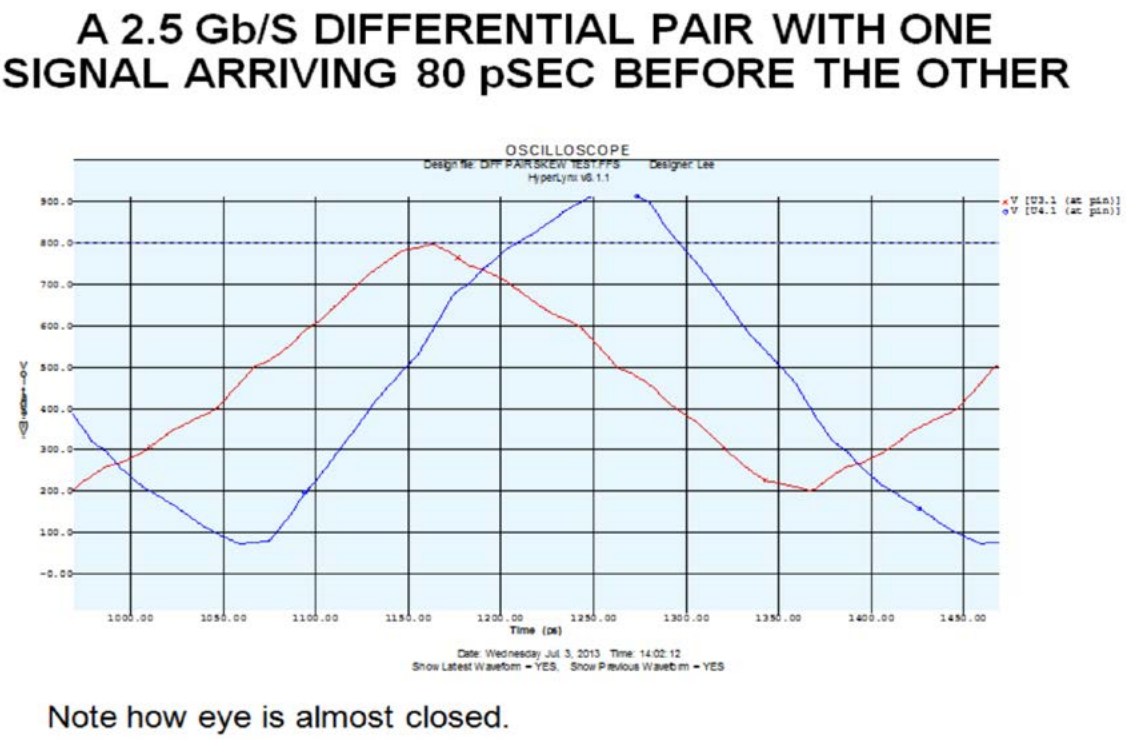


Figure 9: Eye pattern with 80 pico second skew.

perfectly aligned differential pair, Figure 9 shows the effect of only 80ps of skew to the signal, the reader can see that the eye is almost completely closed leading to a loss of signal integrity.

Early efforts to mitigate this effect relied on rotating the circuitry relative to the weave pattern in order to provide an equal path constitution for both parts of the differential pair. However this proved to be an expensive solution as it resulted in large amounts of material wastage in panelisation inefficiency.

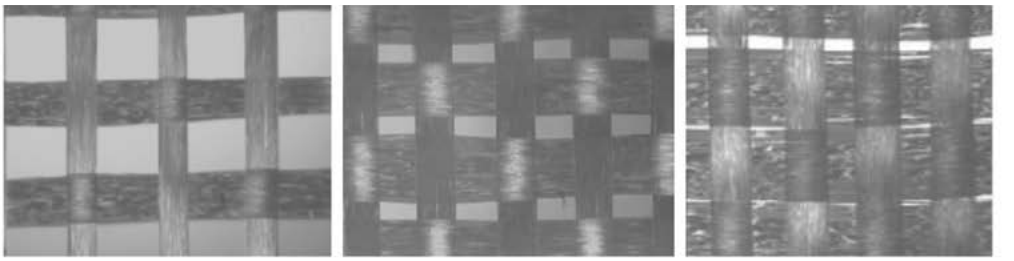
There are a number of techniques directly related to the glass fabric that can be used to mitigate and even completely eliminate this effect. The first relies on altering the glass fabric construction in order to close up the gaps between the glass yarns. The effect is to present the conductor with a more homogeneous substrate over which to pass thus minimising the micro Dk effects described above. In recent years a number of traditional glass cloth styles have been substituted by a "square weave" alternative. The square weave alternative adds additional glass yarns and balances up the warp and weft directions so that they have the same, or nearly the same, thread count in the warp and weft direction. Table 4 shows the construction of some popular square weave glass cloth styles.

There are further techniques that effectively spread the glass fibres out so that they lay flatter and no longer remain in tightly twisted threads thus distributing the available fibres into the gaps between the threads. A number of methods have been employed in recent years to produce this effect; some rely on a change to the yarn production and weaving process, some to an additional post weaving process and some to a combination of techniques. Figure 10 shows photomicrographs of standard 106 style glass, the square weave version 1067 and finally a spread glass version of 1067. The reader can clearly see how the large gaps in the standard 106 glass fabric have been all but eliminated in the spread glass version.

There is now also a novel solution by which skew can be all but eliminated. Isola's newly developed GigaSync™ product offers laminates and prepregs with engineered glass weaves having the same dielectric constant as the resin system. Matching the Dk of both component parts of the composite substrate means the elimination of the skew effect as the micro composition of the substrate can no longer introduce variability to the signal path. This applies to all combinations of glass styles used in a stack-up as the resin content no longer has an influence on the dielectric constant thus simplifying the electrical design. This innovation is an enabler to achieve data transmission rates of 100 Gbps and beyond.

Style	Glass Thickness (mm)	Weight (gsm)	Threads per cm	Yarn
3313	0.084	81	23.6 x 24.4	EC6 16.5/EC6 16.5
1086	0.054	54	23.6 x 23.6	EC5 11/EC5 11
1078	0.043	48	21.3 x 21.3	EC5 11/EC5 11
1067	0.035	31	27.6 x 27.6	EC5 5.5/EC5 5.5
1035	0.028	30	26.0 x 26.8	EC5 5.5/EC5 5.5

Table 4: Selected square-weave woven glass fabrics.



Glass Style	106	1067	1067 Spread **
Weight (grams/sq.m)	24	31	31
Thread count	22.0 x 22.0	27.6 x 27.6	27.6 x 27.6
Yarn (warp/weft)	EC5 5.5/EC5 5.5	EC5 5.5/EC5 5.5	EC5 5.5/EC5 5.5
Glass thickness (mm)	0.033	0.035	0.035
Pressed thickness* (mm)	0.050 - 0.060	0.054 - 0.064	0.054 - 0.064

* Approximate thickness yield range dependant on design, resin content and resin type.

** Courtesy of Isola Fabrics

Figure 10: Glass fabric development—standard weave→square weave→spread glass.

The use of spread glass has brought a number of other benefits which were alluded to earlier in this article. The use of lasers to form microvias in PCBs is commonplace. However the laser ablation rate of glass is significantly lower than that of the resin matrix. An early use of spread glass was to minimise the effect of this differential ablation rate by presenting the laser with a more homogeneous target thus reducing the number of laser pulses required and improving the quality of the hole.

Another significant improvement deriving from the use of spread glass is in the ability to better wet the fibres during the application of the finish which is used as a coupling agent to form a chemical bond between the glass reinforcement and the resin matrix. This benefit extends also to the impregnation process whereby the resin is coated onto the glass fabric to produce a prepreg. The use of traditional tightly bound bundles of glass fibres can lead to defects in the resin/glass interface that can compromise mechanical and chemical integrity. In some cases these defects lying along the fibres can present pathways for conductive anodic filamentation (CAF) to propagate leading to abrupt failure. The use of spread fibres greatly improves the accessibility of the individual fibres thus enabling improved wetting which along with advances in finish chemistry has led to greater reliability in service.

In the future PCB substrates will no doubt utilize even better fibres and resins and will incorporate entirely new materials, including those on the nano scale. We are indebted to the researchers and developers worldwide who continue to advance our knowledge and produce ever more advanced and functional materials to transform the designers' dreams into reality. **PCB**

Alun Morgan is director of OEM marketing, Isola Group Europe.

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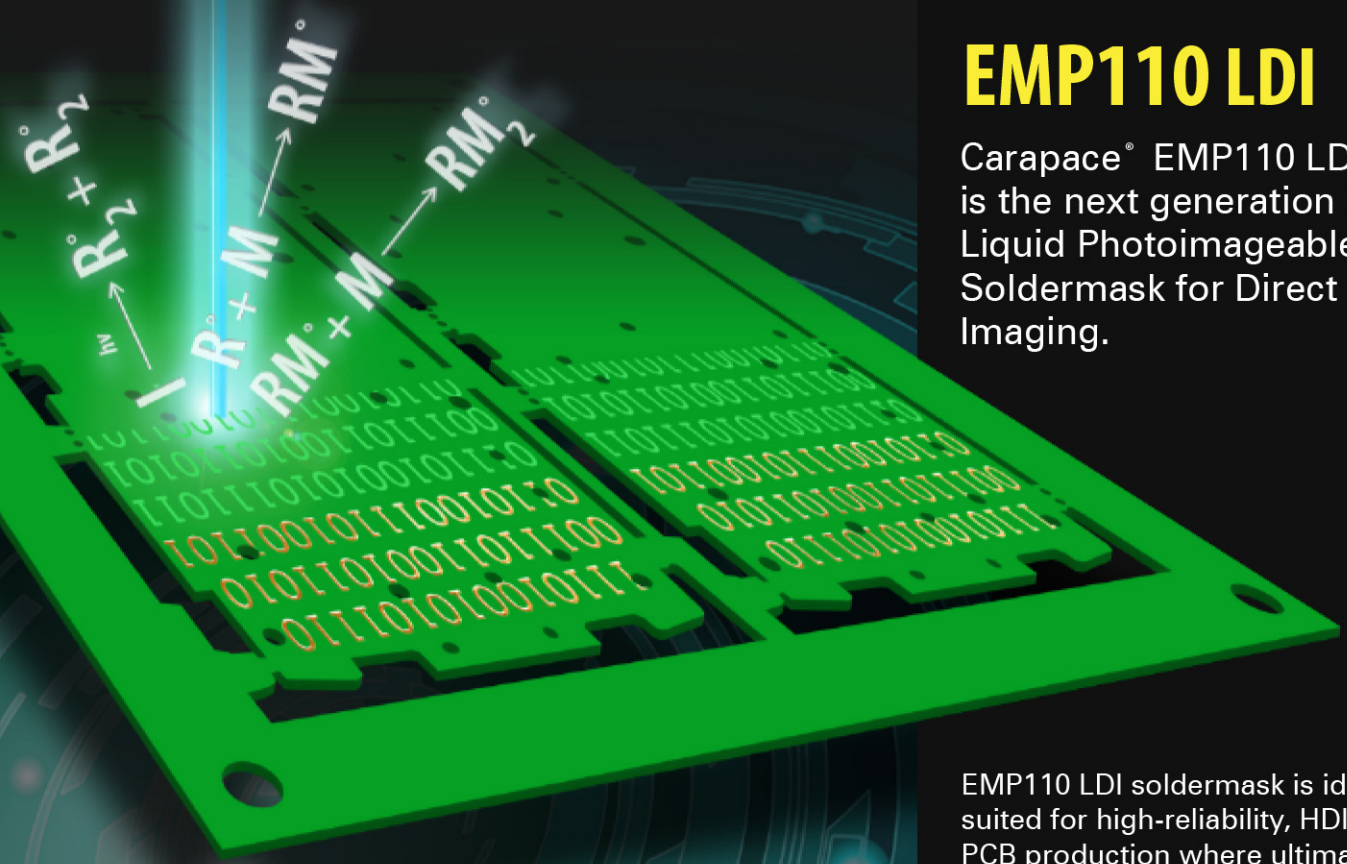

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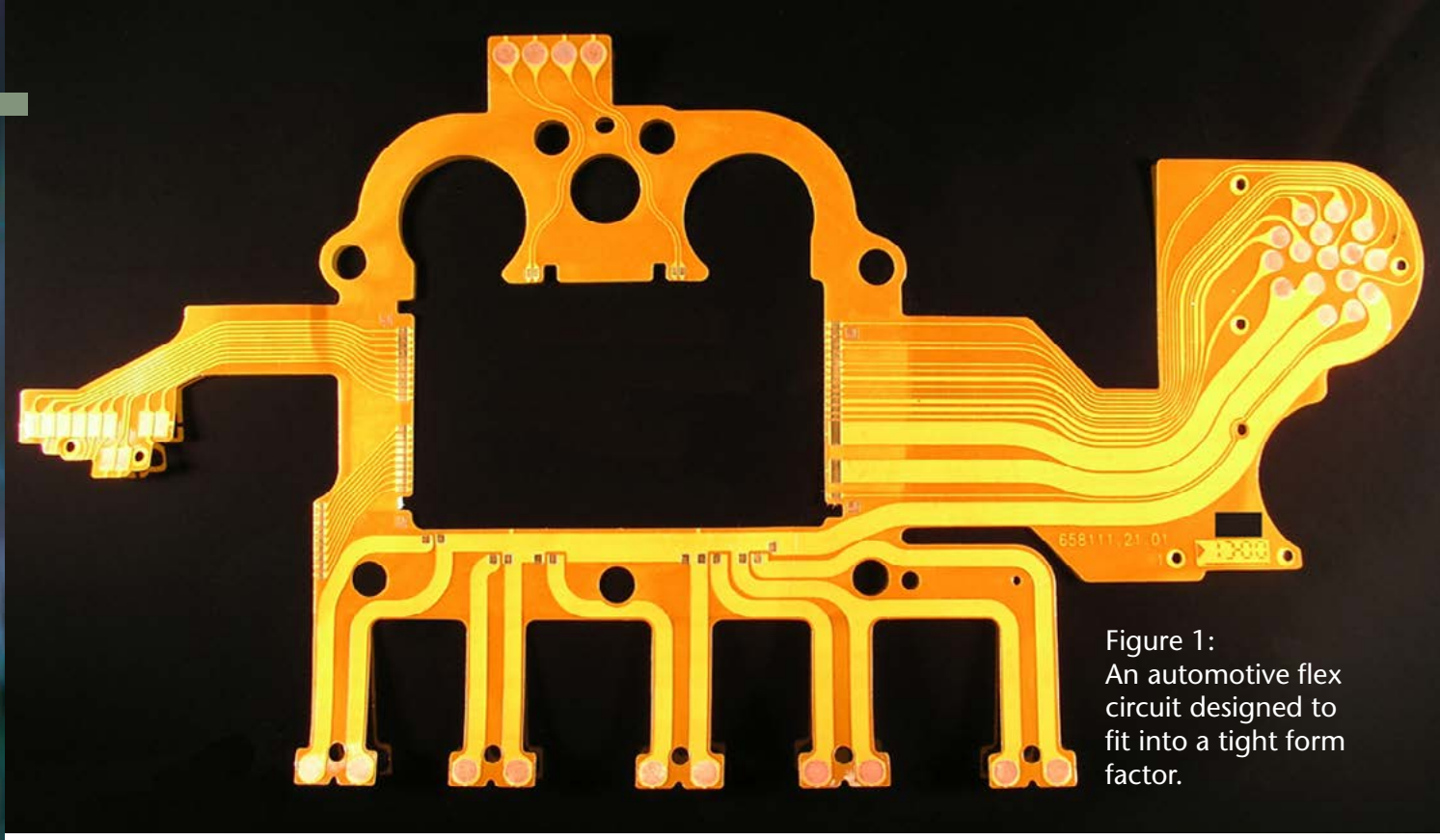

Figure 1:
An automotive flex circuit designed to fit into a tight form factor.

Using Flex in High-Speed Applications

by Glenn Oliver
DUPONT ELECTRONICS AND COMMUNICATIONS

Copper clad circuits in the printed circuit industry have evolved into four different classes, each having different sets of standards. For instance, IPC has separate sets of standards for rigid, flexible, high speed and high frequency, and HDI. Further, there are separate standards within these families for design, acceptance, and base materials. These standards provide logical organization to the design, process, and material considerations of each class of circuit[1]. In many applications, however, designs may utilize all four classes of boards in a single assembly. This presents significant challenges for the designers, fabricators, and materials suppliers because choices made using design rules from one type of board may significantly limit utilization of another type of board on the same assembly. For example, a designer may be forced to use a complex and bulky connector system to link two rigid boards together due to design choices, instead of utilizing a small interconnect utilizing a rigid-flex circuit. The result could be that the assembly does not fit into the assigned form factor. This article will focus on flexible circuit technology and specifically, on the material properties that account for the broader use of flexible circuits in high frequency and high-speed applications.

How Flex and Rigid Materials Differ

Of the four types of circuits mentioned, flex suffers from being the least understood in the design community. There are many reasons for this, but this is mainly due to the fact that flexible circuits comprise a much smaller market than do rigid circuits. In addition, flex designs generally have to fit into a pre-defined form factor which means that very few flex designs look alike. These realities make it a significant challenge for standard design tools to adequately plug flex into their design flow. Figure 1 shows an example of a flex circuit design driven primarily by the form factor in which it must fit. The traditional deployment of flex in these applications facilitates the need for fundamental differences in flex materials from typical rigid

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PCB materials. One fundamental difference about flex materials is that the base dielectric generally does not contain glass reinforcement. Most flexible circuits contain various grades of polyimide as the dielectric to provide both mechanical integrity and flexibility. Some may refer to this polyimide by the DuPont brand name Kapton. The flexible copper clad laminate, or flex core, provides the "backbone" to the circuit and usually is made with Advanced Kapton that has higher elastic modulus. Another fundamental of flex is that soldermask is generally not used to cover the outer layers of the circuit. This is because soldermask is usually very brittle and will crack when flexed. Instead of soldermask, adhesive is coated on one side of a thin, conformable, elastic standard Kapton layer. This is called a coverlay to distinguish it from soldermask, since it is processed differently. In a similar way, a layer used to bond copper clad flex cores together with adhesive coated on both sides of a polyimide layer is called a bondply instead of a prepreg. This is because the polyimide in the center does not flow. Only the adhesive coated to the polyimide flows.

Not only are the dielectrics that go into flex circuits made of different materials than are rigid, but the processes used to make the base dielectrics are also significantly different. Some insight into this difference can be seen in the cross-sections of 50 ohm controlled impedance lines in Figure 2. Most rigid copper clad laminates are made by impregnating resin into a glass cloth. This means that the composite dielectric is created at the same time it is laminated. This is not the case for flex materials. Flex dielectrics are manufactured on large rolls of coated film and laminated to copper as a separate step. The advantage of this manufacturing method is that the thickness of these cast films are very consistent. This additional process step makes it less efficient to make constructions more than 100 um thick. While 100 um thick dielectric layers are considered to be "very thin" and thus challenging to make consistently using a glass/resin lamination process, this thickness range is considered to be "thick" for flexible circuit designs and by comparison relatively easy to manufacture.

Significant differences also exist between the copper typically used in flex and in rigid circuits. Electrodeposited (ED) copper is by far the most common type of copper used for rigid circuits. This type of copper is made by "growing" copper on a large electrified drum that rotates in a solution. The result is very consistent, but with fine copper grains when viewed microscopically. Another way to make copper foil is to start with a large ingot and run it through successively closer rolls. This rolling process anneals the copper making it more ductile by creating relatively large copper grains, leading to

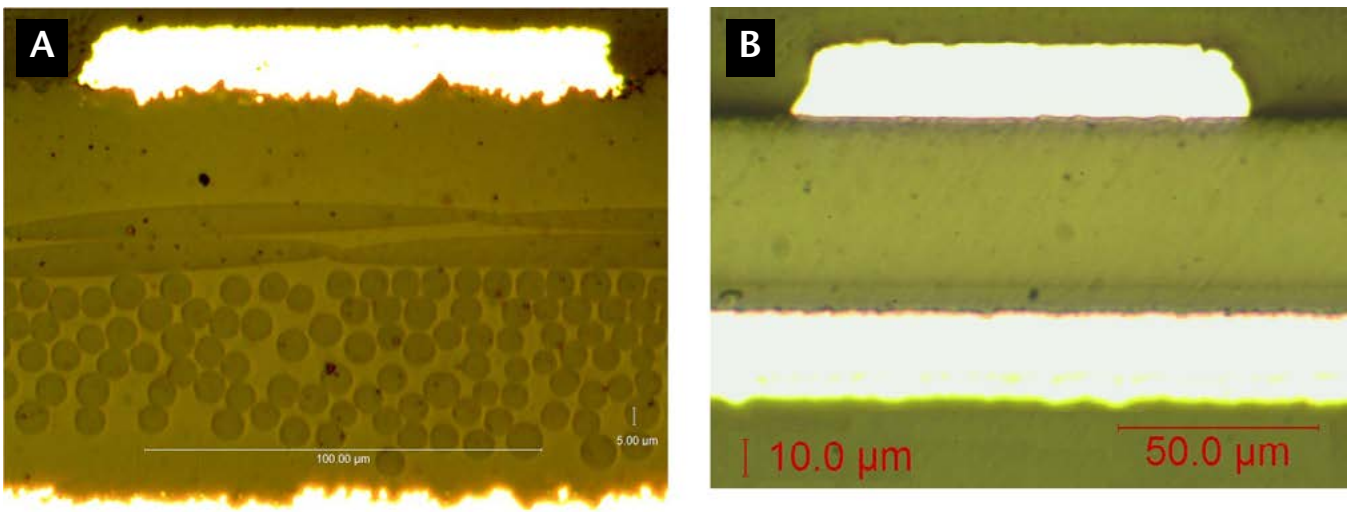

Figure 2: 50 ohm signal lines with rigid (A) and flex (B) materials.

the name rolled-annealed (RA). The improved ductility and larger copper grains make the copper more and less likely to crack due to bending. For this reason, many flexible circuits utilize RA copper instead of ED copper. Another difference between RA and ED copper is how the surface finish must be considered with respect to design and fabrication. Figure 3 shows a low magnification visual microscopic view of the outer copper surface of ED and RA copper clad laminates. Note that there is directionality in the RA copper which is why flex fabricators must always consider the machine direction (MD) in line with the rolls and the orthogonal transverse direction (TD). If one refers back to Figure 2, the impact of this directionality can be seen in the copper profile. The ED copper in Figure 2 (A) is much rougher while the telltale grooves of the smooth RA copper can be seen in Figure 2 (B).

Behavior of Flex Materials at High Frequencies

Traditionally, the electrical properties of flex materials were not considered to be critical since flexibility and copper adhesion were of paramount concern. The dramatic increase in bandwidth requirements and the miniaturization of devices has brought properties like dielectric constant and loss tangent to the forefront of concern. Higher frequencies and speeds require tight control of impedance with very small loss budgets. These current applications require consistent dielectric thickness, low dielectric constant and low dielectric loss.

Dielectric Constant and Loss Tangent

At frequencies above 1 GHz, the term "dielectric constant" is actually a misnomer. This property is not constant with frequency in this region for most organic materials used in printed circuits. The reason for this is that the molecules in these polymers vibrate when RF or microwave energy is applied. The property must be described with a complex quantity called relative permittivity. The real component most closely aligns to the concept dielectric constant and describes the energy stored in the dielectric by capacitance. The imaginary component describes the energy lost in the dielectric. If you take the tangent of the ratio of these two components, you get the loss tangent of the material. Materials with high loss not only are problematic since more energy is absorbed, but the relative permittivity will change a lot more with frequency. This phenomenon called dispersion is not unique to flex materials. Typical epoxies used in rigid circuits have very similar behavior electrically to the acrylic adhesives more typically used in flex circuits. Due to differences in processing preferences, epoxy is more commonly used as a flex adhesive in Asia while acrylic is more commonly used in North America and

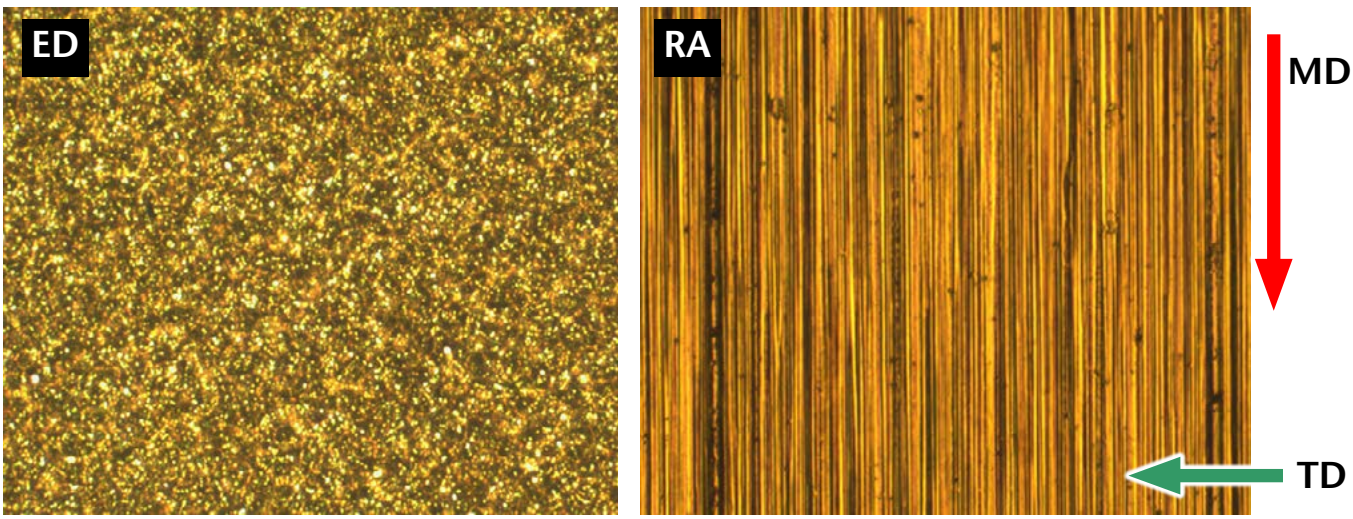

Figure 3: (l) Optical microscope images of electrodeposited and (r) rolled annealed copper.

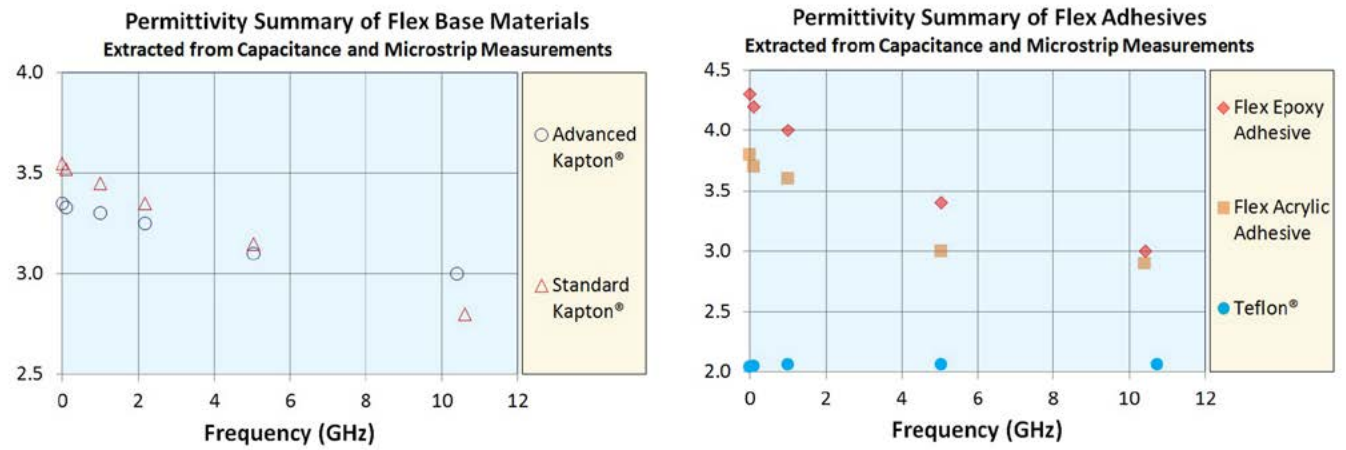

Figure 4: Relative permittivity versus frequency of flex dielectrics and adhesives.

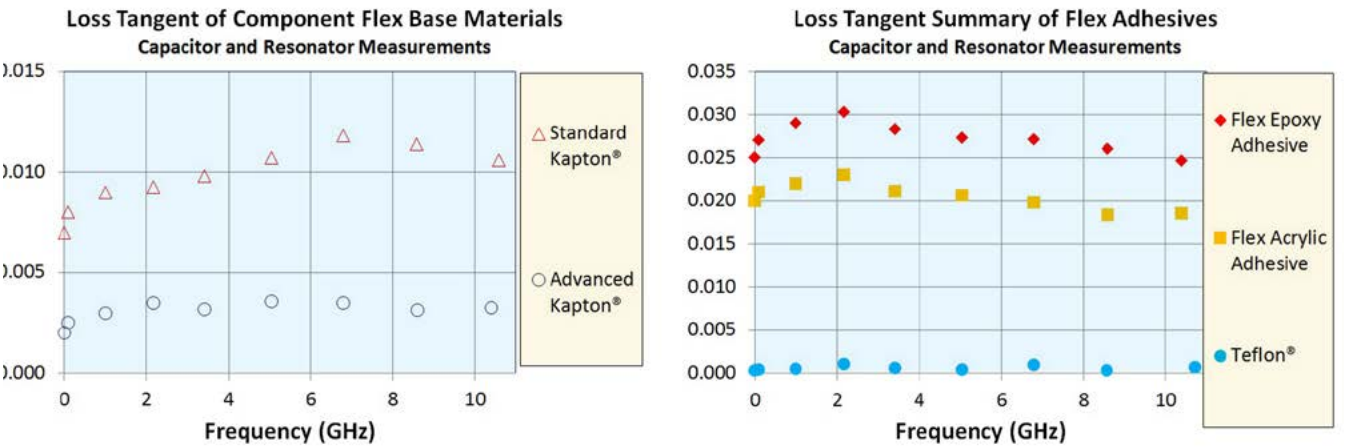

Figure 5: Loss tangent versus frequency of flex dielectrics and adhesives.

Europe. Figure 4 summarizes the relative permittivity versus frequency for Kapton®, Teflon® and the common adhesive materials used in flex circuits. Notice that Advanced Kapton used for high-frequency copper clad flexible laminates has lower dispersion compared to standard Kapton used for coverlay.

Loss tangent values for these same materials are also shown in Figure 5. When analyzed in concert with Figure 4, one will notice that the materials with the least amount of dispersion have the lowest loss tangent. Low loss and low dispersion are two of the primary reasons why Advanced Kapton and Teflon are used to maximize signal integrity for high-speed flexible circuits.

Lower Loss Copper

Not just the dielectric has a great impact on signal integrity. As thickness of layers reduces, the copper has an exponentially increasing impact on signal loss compared to the dielectric. If you suppose the air had dielectric loss at varying levels, then Figure 6 shows the signal loss of a stripline for a thick structure, a nominal structure, and a thin structure. Note that the loss is inherently larger due to the fundamental resistivity of copper for thin structures. For thick

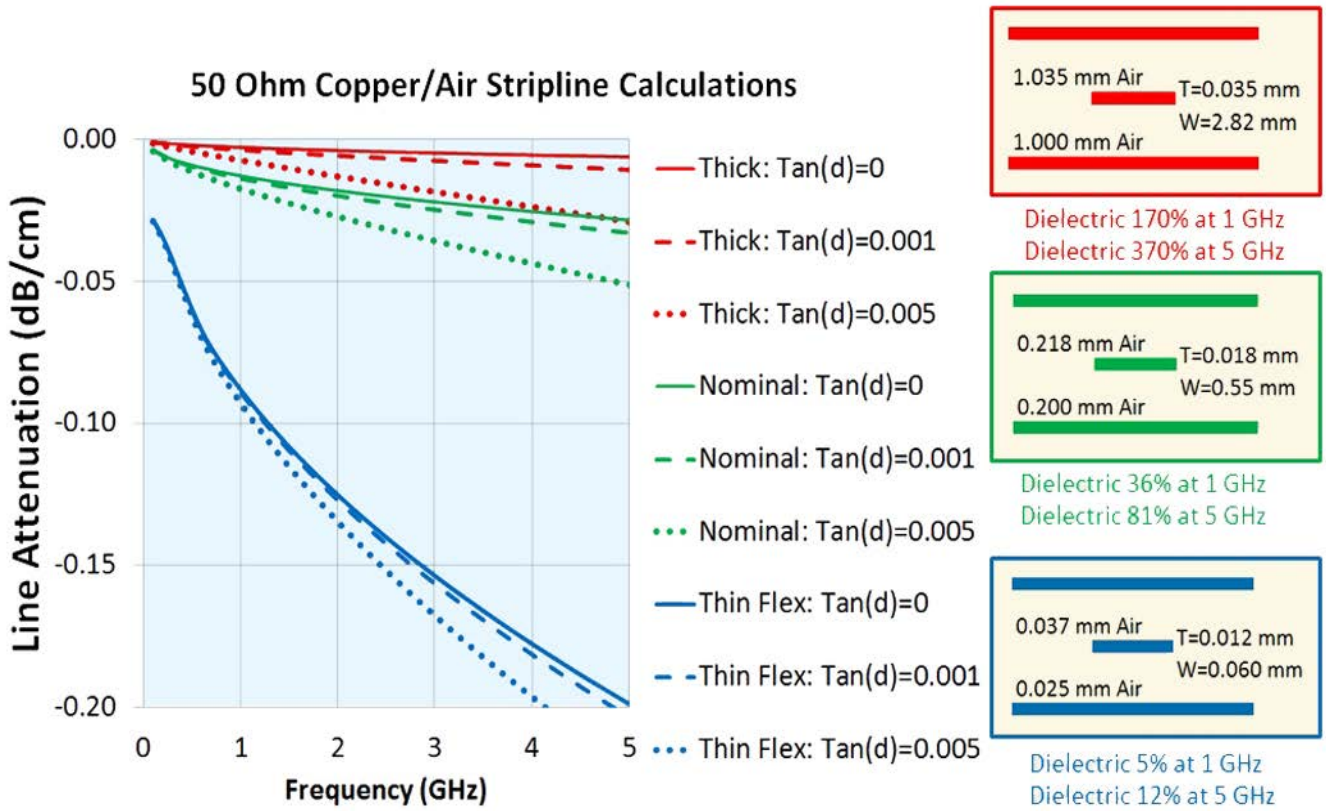

Figure 6: Calculated values from the effect of thickness and dielectric loss.

structures, decreasing the loss of the dielectric has a huge impact[2]. For thin structures the conductor accounts for most of the loss so lowering the dielectric loss only has a significant impact at high frequencies.

Signal Integrity Analysis Tools

One source of frustration for flex designers having to meet controlled impedance requirements is that using the known permittivity values of flex materials in field solvers to calculate line width can be off. The reason for this is that most of these field solvers assume the use of glass reinforced copper clad laminates like FR-4. The software is optimized and verified by use of relatively thick layers and wide conductor lines compared to flex. In general, the designer or fabricator must bias the dielectric constant lower than the actual values reported on data sheets to get consistent line width predictions.

Overall Impact on Loss Performance

It is possible to utilize Teflon and Advanced Kapton together to construct flexible circuit materials[3]. The low dispersion and low loss tangent of these materials shown in Figures 4 and 5 combine to make the optimum platform for high-speed signals in a flex circuit. Figure 7 summarizes measurements taken from microstrip transmission lines made at the same time. Common materials used in high-speed transmission (Meg4 and Meg6) are directly compared to a Teflon-Kapton composite (TK). As frequencies increase, the impact of the smoother RA copper becomes quite significant. The copper weight and type are denoted on the plot legend.

Summary Takeaways

- Flex circuits offer great advantages to designers, but there are big differences between flex materials and rigid materials. These include design, fabrication, and materials. Understand-

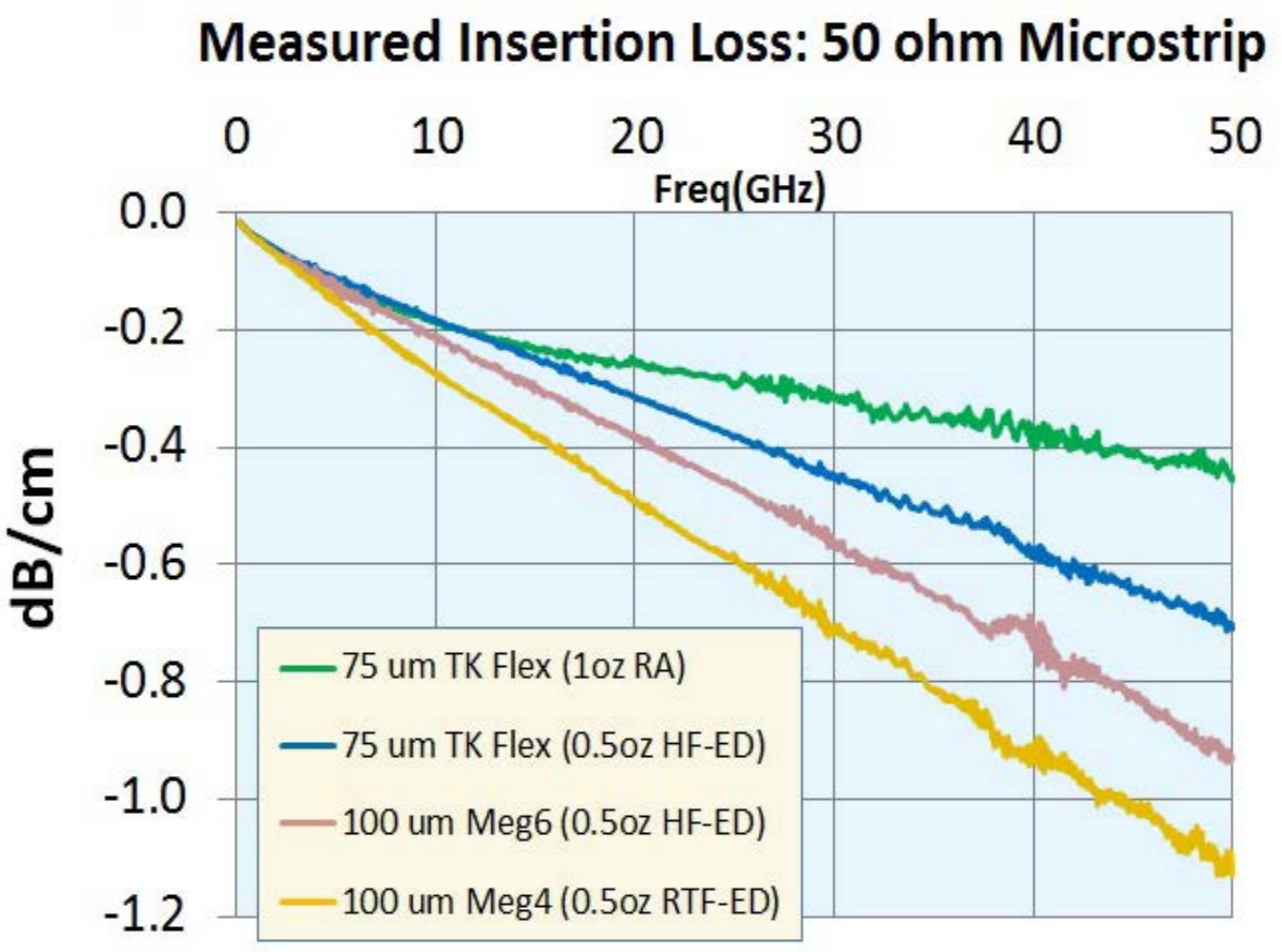

Figure 7: Comparison of high-speed flex to high-speed rigid microstrip lines.

ing the differences between the materials can help both fabricators and designers better utilize flex circuits to meet their goals.

• To utilize flex in high-speed and high frequency applications, the effect of the Kapton, adhesive must be understood in the same way that the effects of the glass and resin must be known for rigid designs.

• Not all Kapton are created equal. Advanced, high modulus Kapton has low loss and low dispersion compared to Kapton used for coverlay.

• As high-speed circuits get thinner, the more it makes sense to utilize flexible circuits in these designs because of the inherent properties of flex materials. **PCB**

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1. Specification Tree of Standards organized by IPC.

2. Oliver, G and Coonrod, J. Practical Measurements of Dielectric and Loss of PCB Materials at High Frequencies, DesignCon 2014.

3. More information on the composite materials can be found at www.pyralux.com/tk.

Glenn Oliver is a senior engineer at DuPont Electronics and Communications.

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Mil/Aero007 News Highlights

Pro-Tech Earns AS9100 Rev C Certification

The company has achieved full certification to AS9100C Quality Management Systems—Requirements for Aviation, Space and Defense Organizations. The successful completion of the requirements and the certification means that Pro-Tech Interconnect Solutions is now certified to AS9100C:2009, ISO 9001:2008 Quality Systems, ISO 13485:2003, MIL-PRF-31032/MIL-PRF-55110, along with ITAR registration.

FTG 4Q Sales Up 12%, 1% FY 2013

"As 2013 ended, FTG had achieved its strategic objective for both its Circuits and Aerospace businesses of establishing manufacturing footprints in Canada, our home base, the United States, the largest aerospace and defense market, and Asia, the fastest growing aerospace market," stated Brad Bourne, president and CEO.

DYCONEX Adds Ticer TCR-HF Foils

DYCONEX announced that it has added Ticer TCR-HF foils to its range of build-up materials. TCR-HF is a low insertion loss NiCr thin film embedded-resistor copper foil, designed especially for high-frequency telecommunications, aerospace, and defense applications.

Schweizer Certified to EN 9100 Certification

"By obtaining certificates we have independent parties confirm that our products are manufactured based on internationally determined quality standards and that—related to environment, labour, and health protection—we do more than required by law," stresses Nicolas Schweizer, chief commercial officer.

UAV Market to Hit $114.7B by 2023

A new report says the global UAV market size can be expected to grow to $8,351.11 million by 2018. (HALE/MALE/SUAV) market has the highest business potential throughout the study period whereas the U.S. and Israel will be the maximum revenue generator, among the countries manufacturing UAVs.

Global Comm Sat Imaging Market Sees Demand Increase

According to a new market report "Commercial Satellite Imaging Market—Global Industry Analysis, Size, Share, Growth, Trends, and Forecast, 2013-2019," published by Transparency Market Research, the market for commercial satellite imaging globally is forecast to reach U.S. $5,018.6 million by 2019.

Asia Pacific Takes 36% of World's New Airplane Deliveries

Boeing says strong economic and passenger growth will be main drivers of new airplane demand in the Asia Pacific region. The company estimates the region's airlines will need an additional 12,820 airplanes valued at $1.9 trillion, representing 36% of the world's new airplane deliveries over the next 20 years.

Report: Stretchable Electronics on the Rise

The report provides an examination of how stretchable technology fits into the printed electronics and allied scenes, the materials, and applications that look most promising and the lessons of success and failure.

Carbon Nanotube Fibers Outperform Copper

On a pound-per-pound basis, carbon nanotube-based fibers invented at Rice University have greater capacity to carry electrical current than copper cables of the same mass, according to new research.

Smart Weapons Market Forecasts & Opportunities Report

Smart weapons range from precision-guided artillery rounds and bombs to stand-off missiles. Anti-armor weapons comprise of anti-tank and anti-structure missiles.

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Oxide vs. Oxide Alternative Chemistry for High-Performance Resin Systems, Part 2

by Michael Carano
OMG ELECTRONIC CHEMICALS LLC

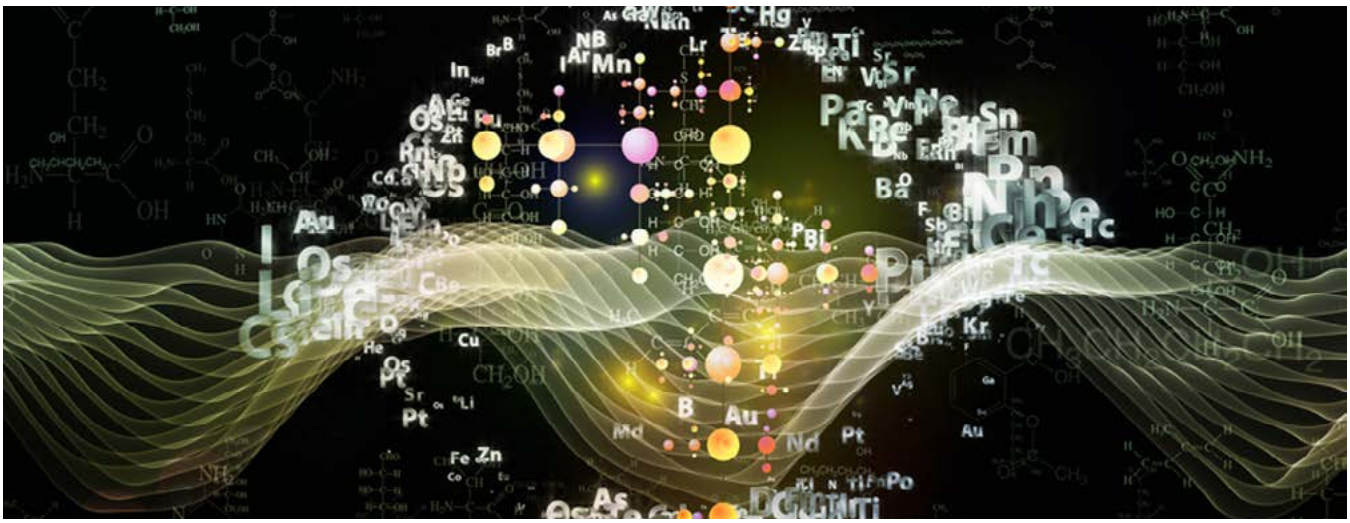
Introduction

In last month's column, I presented an overview of conventional oxide chemistry and the critical success factors of the process. In this column, we begin our review of the oxide alternative process that is often referred to as an organo-metallic coating process. The reason for this alternative name will be explained in this column.

With continued emphasis on long-term reliability and vastly improved electrical performance, manufacturers of high layer-count multilayer printed wiring boards are beginning to abandon the reduced oxide bonding process in favor of alternative methods. One such method, presented here as an organo-metallic adhesion promotion system, increases the bond strength of the resin to the copper by modifying the topography of the copper surface and simultaneously depositing an organic layer that acts as an adhesion promoter. The surface area or topography of the copper is enhanced by the selective micro-etching along the grain boundaries of the copper. (This mechanism will be discussed further below.) This is in contrast to the oxide-based chemical processes in that the oxide processes are designed to "grow a crystal structure" on the copper surface. The concern with oxide processes (even the formulations designed to give a denser shorter crystal structure) is that the higher pressures and temperatures of lamination required for higher performance laminate materials will fracture the oxide crystal structure reducing the bond strength. With that said, let's discuss oxide alternative or organo-metallic chemistry and how it all works.

Oxide Alternative Chemistry and the Theory of Bonding

Before presenting the particulars of alternative oxide chemistry, it would be a good idea to present multilayer bonding theory. There are two main factors involved in enhancing the bonding strength of copper to the prepreg for multilayer lamination of circuit boards. They are 1) the type and degree of roughness imparted to the copper surface and 2) the type and thickness of any coating that is applied to the copper surface[1].



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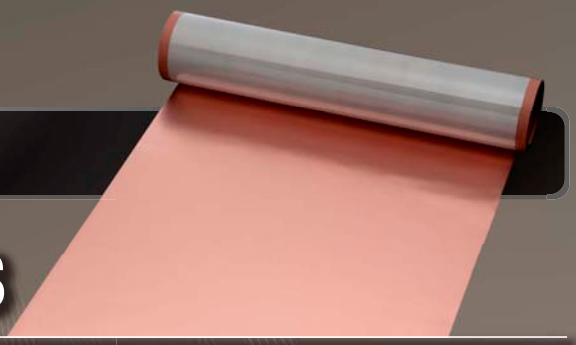
Flexible Materials



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Roughness: Current oxide coating processes impart micro-roughness to the copper surface that greatly exceeds the degree of roughness that is obtained with normal copper micro-etchants. In order to match or exceed the bond strength that oxide processes impart to the copper, these microetchants would need to be reformulated to greatly increase the degree of roughness[2]. Not all forms of roughness are the same. For example, sanding the copper surface would impart a great deal of roughness to the surface but the bonding strength would still be very low due to the fact that this roughness would be macro-roughness rather than micro-roughness. Good copper adhesion starts with imparting a micro-roughened surface to the copper. This roughness can only be seen with a SEM at powers of about 2000X or higher. A power of 5000X is commonly used. With such a photograph of the surface we see that a typical oxide process roughens the copper on the order of 0.1–0.5 microns peak-to-peak. Also, the peak-to-valley distance (perpendicular to the copper plane) is greater than the peak-to-peak distance (parallel to the copper plane). The type of micro-roughness (different peak-to-peak and peak-to-valley distances) will influence the bonding characteristics of the copper to the prepreg. Even shape (prism-like, jagged, round, bent, etc.) can influence the bonding characteristics[2]. The very same argument can be made with respect to photoresist adhesion to the copper surface. Shape of the peaks and the extent of the overall surface roughness will influence the ability of the resin to properly flow and adhere to the surface. Different prepregs will have different flow and wetting characteristics. It is possible that some prepregs will flow and wet out the entire micro-roughened surface from top to bottom. While other prepregs with low flow characteristics may not be able to flow all the way down to the bottom of the valley and may not completely wet out the micro-roughened copper. This leaves a micro-gap at the bottom of the valley where solution can leach into the coating and cause issues, maybe even pink ring (even though the peel strengths are high). So it is conceivable that some prepregs will like a certain type of micro-roughness, and other prepregs may do better with another type of micro-roughness[2]. This may explain the differences in interlaminar bond strengths achieved with oxide versus oxide alternatives.

Chemistry of Oxide Alternatives

The alternative process often referred to as an organo-metallic process, imparts a coating on the copper surface at the same time as etching/micro-roughening the surface. Unlike the inorganic oxide coating, the alternative coating is organic. (Often referred to as an organo-metallic, due to the nature of the organic coating forming on the copper.) During the oxidation of the copper, a metal/organic coordinate is formed that is insoluble in the process solution. This coating is a vital part of the bonding mechanism. Tests have shown that copper surfaces with equal or even greater degree of micro-roughening, but which do not contain a metal/organic coating, do not provide good bonding characteristics. This is especially true with respect to time to delamination. The organo-metallic coating increases the bond strength, especially at high temperature stress conditions such as solder immersion. This is due to chemical interaction between the copper and the coating (a coordination bond is formed), and the coating and the prepreg (a sharing of pi electrons occurs)[2].

Chemical Reaction: Organic metallic process is a peroxide-sulfuric based etching and coating solution that has been specially and uniquely formulated to impart micro-roughness to the copper surface that greatly exceeds normal etchants and at the same time forms a coating on the surface that promotes adhesion through chemical bonding. Peroxide etches copper by oxidizing Cu° to Cu^{2+}. The half-cell reactions are shown below:

$$Cu^0 \rightarrow Cu^{2+} + 2e^- \text{ (-0.3419 volts)}$$
$$H_2O_2 + 2H^+ + 2e^- \rightarrow 2H_2O \text{ (+1.776 volts)}$$

The net reaction is:

$$H_2O_2 + 2H^+ + Cu^0 \rightarrow Cu^{2+} + 2H_2O$$
(+1.4341 volts)

If sulfuric acid is used then we have:

$$H_2O_2 + H_2SO_4 + Cu^0 \rightarrow CuSO_4 + 2H_2O$$
(~+1.4341 volts)

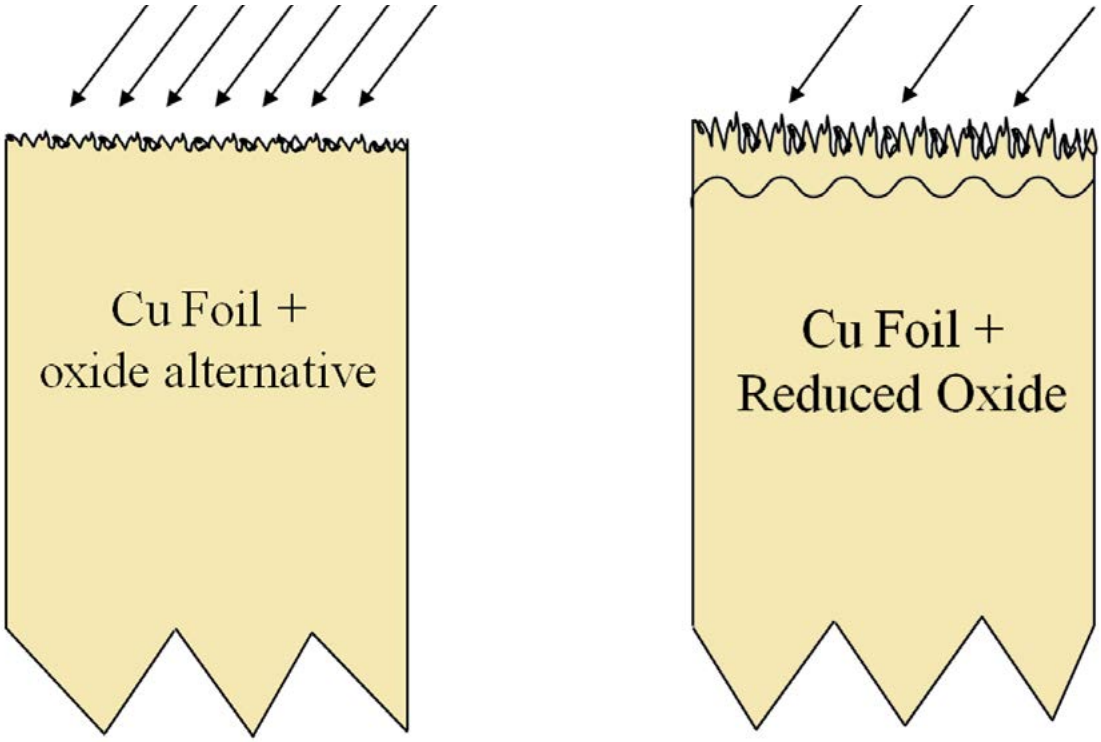

Figure 1: Comparison between oxide alternatives (left) and conventional reduced oxide (right).

This reaction consumes one mole of peroxide, one mole of sulfuric acid and one mole of copper metal and produces one mole of copper sulfate and two moles of water. The positive voltage indicates that this reaction is spontaneous and the relatively high voltage of this chemical system further indicates that virtually every molecular collision of peroxide with copper will result in a reaction (when the acid is in excess). This means that the number of collisions per second controls the reaction rate. So the higher the peroxide concentration, agitation, and temperature, the faster the reaction will go. The reaction above indicates that there is no gas produced by the reaction, yet when boards are etched with peroxide one can visually see gassing at the board surface. This means that the reaction is not 100% efficient and that some peroxide reacts at the surface by spontaneously breaking down. This is an important consideration when comparing the chemical usage of oxide alternatives with conventional oxide processes.

Figure 1 illustrates the differences in the two innerlayer treatment processing systems.

Oxide coatings bond by resin wet-out and encapsulation of surface topography—dependant on the resin flow. The resin as it cures then forms a bond between the resin treated copper surface. Organo-metallic component of oxide alternative facilitates resin wet-out of surface; in addition, chemical and mechanical bonding occurs.

In a future Trouble in Your Tank, we will explore the performance characteristics of oxide alternatives. **PCB**

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2. U.S. Patent # 5,691,130.

Michael Carano is with OMG Electronic Chemicals, a developer and provider of processes and materials for the electronics industry supply chain. To read past columns, or to contact the author, click here.

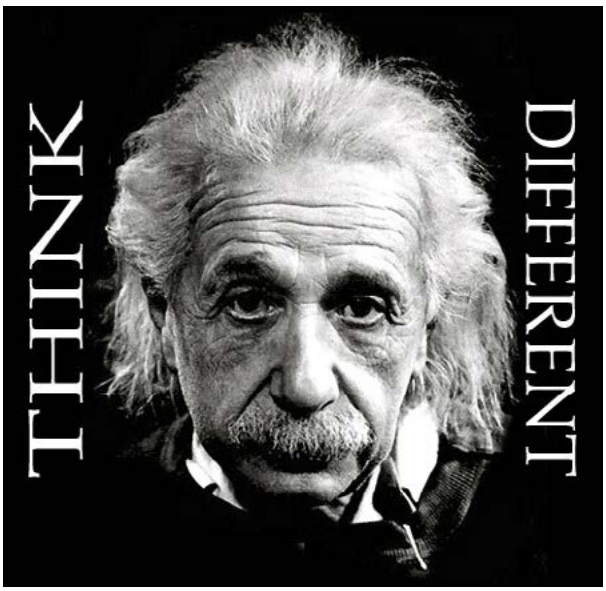
Do We Need to be More Innovative?

by Gray McQuarrie
GRAYROCK & ASSOCIATES

Vulnerability is the birthplace of innovation, creativity, and change.
—Brené Brown, author of Daring Greatly

Do we want, or even need, more innovation in the U.S. PCB industry? Many times when I try to bring up the topic of innovation I hear, "Do not talk to me about new ideas, models, new technology, or a creatively inspired work force; I need more sales. This is my reality."

There is a Latin saying, "castigat ridendo mores," which means, "one corrects customs by laughing at them." Should we laugh at those who practice the custom of not innovating while at the same time demanding higher sales?



I know of four board shops in the U.S. or Canada that don't have a sales problem. Yes, they do worry about their sales, of course, but they worry about it within the context of how to change and innovate in order to sustain and grow their sales. When I bring this up to other shops, the discussion is quickly shot down. The common response, "They have a niche business. We aren't interested in niche."

When used in this way, niche suggests an element of blind luck and irrelevance to the sales problem at hand. For example, Apple's Macintosh computer, still to this day, isn't considered a business computer. It's a computer that serves a specialized creative niche. In fact, this attitude is so pervasive that friends ask me when I am going to get rid of my Mac and buy a real computer! When Apple was brought back from the brink, their marketing campaign featured a large picture of Albert Einstein, with the caption, "Think Different." When I think of Albert Einstein I find myself remembering his definition of insanity: doing the same thing over and over again and expecting different results. Innovation—doing things differently and getting different results—was the tool Steve Jobs used to turn Apple around. Too many of Apple's competitors refused to change and still refuse to change today. The number one fear in the investment community concerning Apple is whether they lost their ability to innovate since losing Steve Jobs. Without Steve, there has yet to be a new groundbreaking innovative product released by them that has opened up a new (and for some, niche) market.

Our industry was once full of innovation. There was Shipley, PCK Technology, Rogers, Oak Industries, just to name a few of the most innovative companies of our past. I remember when Continental Circuits jumped into surface mount technology and their sales grew severalfold, seemingly overnight. Yes, at the start this was a niche business, but it defined what would become our mainstream business. I remember the microscopically small Cray-3 PCB production line in Chippewa Falls, Wisconsin, where an entire plating line could fit on a desk. This, of course, proved impractical for the long haul, but I would submit there are lessons we could all learn from this effort if we so chose. Some innovations worked, such as Shipley's 4000 bath, which produced fantastically reliable plated

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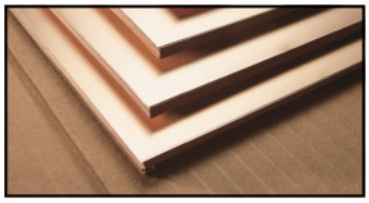

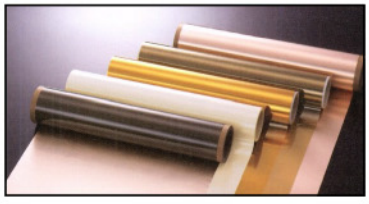

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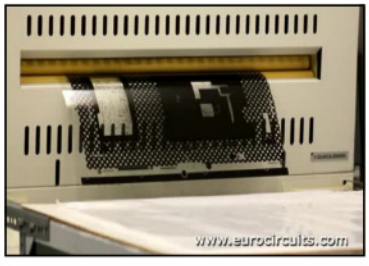

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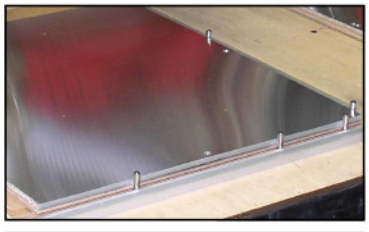

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through-holes and created for Shipley a huge market share shift in their favor. By the way, the reasons they did what they did had nothing to do with hole-wall reliability; it was something they just discovered after the fact. Yes, they were lucky, but this is what happens sometimes (not always) with innovative efforts. Some innovations were spectacular failures, such as PCK's multiwire process. In conversations I have had, this is often cited as the reason why creative types and their new ideas need to stay out of our industry. And usually when I hear about failures like this, there always seems to be some sort of derisive laughter. It's as if the failures from the innovative efforts are the bricks and the laughter coming from reminiscing about the foolish effort is the concrete, which taken together form a strong wall meant to keep all innovation out.

This behavior of shaming those that have failed with their innovations reinforces the status quo, so we as an entire block of companies become a stubborn, unmovable object. With no means of providing products that are leading edge, is it any wonder why so many of us struggle with our sales? We are a very easy one-dimensional target to hit. Just drive the price down until we quit. The problem isn't China. The problem is us! The problem exists within our four walls. By casting innovation as an anathema we have become our own worst enemy.

"This behavior of shaming those that have failed with their innovations reinforces the status quo, so we as an entire block of companies become a stubborn, unmovable object."

I remember in the early '90s, when a good friend and mentor of mine gave a presentation to a large audience at a conference, providing an update and technical review of Shipley's Eagle line. Sitting near the back, I could hear people a decade or older than me, snickering and telling Charlie Shipley jokes and saying, more or less, "I know it will fail, ha, ha, ha. What a fool that man is talking up there." When the Eagle technology eventually failed in the U.S. market, I will never forget the emotional pain and dejection this team went through. They were treated like lepers within the company. Nobody wanted to be a part of them and nobody wanted to do something that innovative and that risky again. Why?

At the time Shipley was being taken over by a professional and conservative management team. Their mission wasn't new products as much as it was to generate as much cash each quarter as possible to be fed back to what was emerging to be the new corporate owner. They saw the risk-taking that founder Charlie Shipley had instilled as a threat that needed to be contained. And to my utter disbelief I was amazed at how the new management began talking badly behind Shipley's back and encouraging others to laugh at him and his past inventions.

Unfortunately, I see this kind of behavior all of the time in too many board shops. And it doesn't have to be about anything particularly innovative, but it is all about having power over people in an environment that isn't about growth, but about scarcity. When people are afraid, bad behaviors are spawned all over the place. The good news about all of this unpleasantness is that there really is no greater way to improve your business, innovation level, and long-term sales prospects, than by completely eliminating bad behavior, even if it means firing top performers. If you want to know more about this, then I would encourage you to read Robert Sutton's The No Asshole Rule, which he summarizes in this video.

No, we are not done yet. There is an extremely important point to be made about innovation. Innovation is probably the single riskiest activity that any human can do. Pixar and Next nearly wiped out Steve Jobs' $100 million-plus fortune. At one point, it looked like a virtual certainty that both companies were going to fail. Instead, just weeks after the release of Toy Story, Jobs' net worth was $1.1 billion after Pixar went public. How many of us are willing to bet our homes, our kids' future, our professional reputation and credibility on ideas and

inventions that have never been tried? Would we make the bet, if there was a slight chance we could become a millionaire or even a billionaire? Would we still make the bet knowing there was also a chance we could lose everything? You could make the case that only an insane person would make such a bet.

And if they were crazy enough to do it, we might even be able to excuse them for acting like complete assholes sometimes—thus the important difference. If you are being an asshole because you want to have power over people, you are contributing to your company's demise. If you are being an asshole because you feel completely vulnerable and scared doing something innovative, well, maybe that is OK, and maybe even necessary. It's hard to stay rational when you feel vulnerable and scared. If you are interested in understanding more about the power that vulnerability has over us, I recommend you watch Brené Brown's talk on the Power of Vulnerability.

If you wonder why I suggested a video like this, then I ask you to review my example above concerning the Eagle team. Only by having a culture that encourages vulnerability and also encourages empathetic support of each other can an innovative culture be created and sustained. The question remains as to whether Apple's innovative culture is still there. The question for us is, should we and can we jump-start the innovative culture we use to have in the PCB industry?

I cover these concepts thoroughly in my latest book, You Have a DAM Problem. Click here for more information. **PCB**

Gray McQuarrie is president of Grayrock & Associates, a team of experts dedicated to building collaborative team environments that make companies maximally effective. To read past columns, or to contact McQuarrie, click here.

VIDEO INTERVIEW

High-Speed, High-Reliability, Halogen-Free!

by Real Time with...productronica 2013

Isola Director of OEM Marketing Alun Morgan explains how Isola has addressed the market for special-purpose laminates. He describes how high-speed performance can be achieved with high-reliability, halogen-free materials and discusses the latest developments in ultra-thin glass-reinforced laminates.

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Capturing Tribal Knowledge

by Steve Williams
STEVE WILLIAMS CONSULTING LLC

Elizabeth II, Queen of Great Britain and Northern Ireland, made the following salient proclamation more than 50 years ago: "It's all to do with the training: You can do a lot if you're properly trained." What has held true through the ages is not a secret; people perform better when properly trained.

Walk the Walk

Training is often an afterthought in many organizations, and the longer a company has been in business, the more this seems to apply. While assessing more than 1,000 companies over the past couple of decades, it has been amazing to observe that the biggest offenders of this component are the companies that overuse the sound bite "our most important asset is our people." When you really dig into the process and peel back the onion, it is clear that their commitment to training is not commensurate with that statement. No matter what you call it: training, coaching, mentoring, etc., what we are really talking about is turning people into a competitive advantage.

A keystone of any world-class organization is the depth and breadth of the training program. Training can be defined as learning that is provided in order to improve performance on the present job. A well-managed program in a printed circuit board fabricator can mean the difference between average and outstanding performance. Of course, this applies to every industry, but with up to 60 different possible processes, combined with the degree of difficulty required to produce today's PCBs, it takes on exponential importance.

Typical Scenario

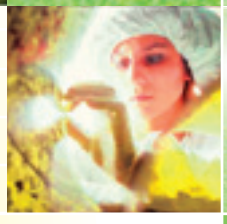
I've heard the following conversation repeated many times, so it may sound familiar:

Supplier: "This is Larry; he is our best plater and runs this department."

Customer: "Can I see his training file documenting that Larry is a certified operator for plating?"

Supplier: "Uh, we don't really have a certified operator program, but Larry IS the trainer for

The New CCMP



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plating and every operator is trained by Larry. He could make up every one of these baths from scratch."

Customer: "How do you know when an operator is ready to work on his or her own?

Supplier: "Larry says so. He also personally reviews and approves every single job that is released from plating to assure quality."

Customer: "What happens if one of my jobs is scheduled to be plated when Larry is on vacation or sick?"

Supplier: (Silence)

Customer: "Exactly."

In this scenario, both the company and its employees tend to view training negatively, even as an insult, as if it were some form of remediation. This perception couldn't be further from the truth! One of the greatest advantages of training in this situation is that it allows you to capture the tribal knowledge of the highly-skilled workforce. What I mean by tribal knowledge is the entirety of the expertise of people like Larry, tricks of the trade, and the idiosyncrasies of the job that have been learned over the last 30 years and probably not documented anywhere. Preserving this tribal knowledge and

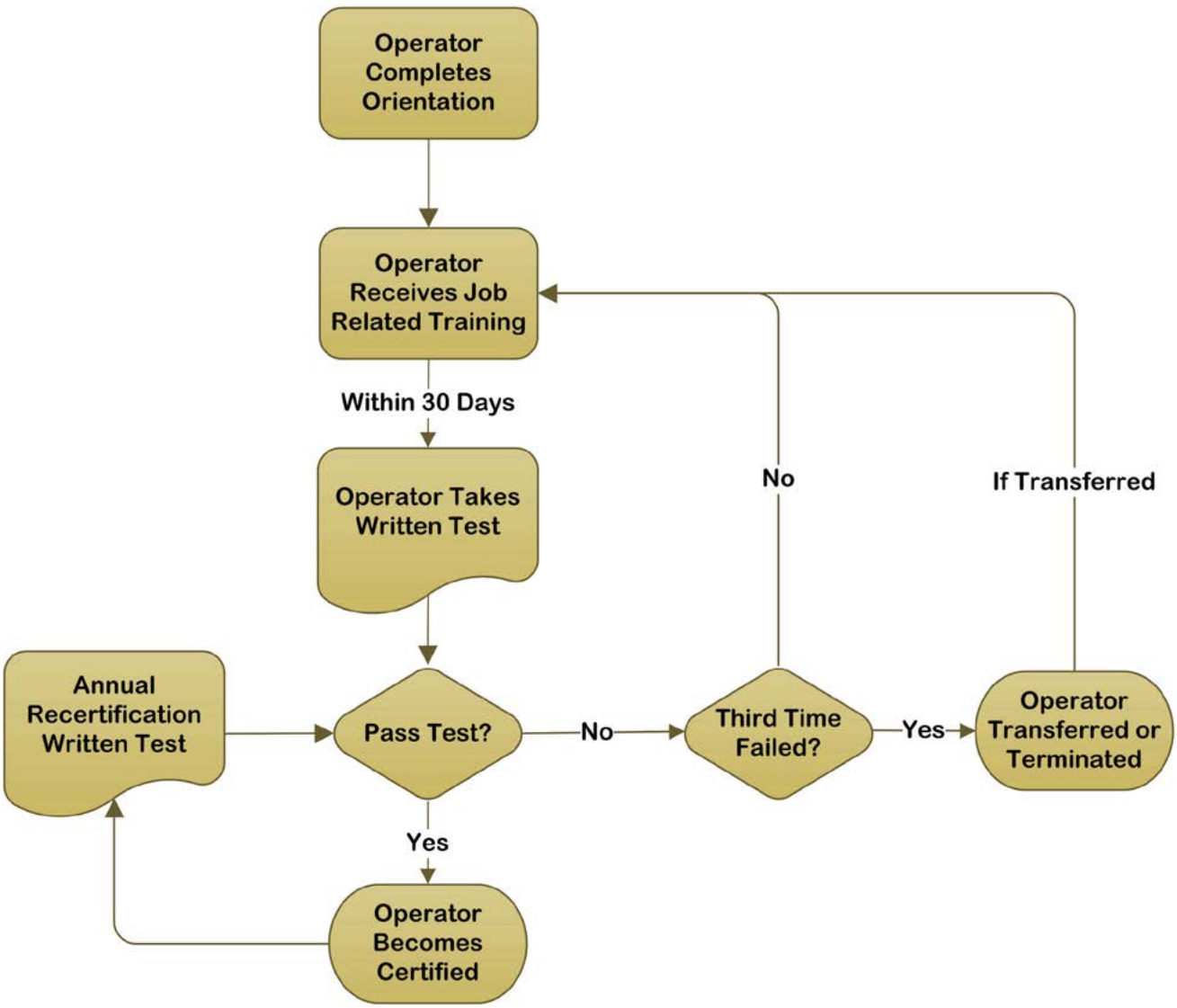

Figure 1: A certified operator process map.

turning it into a training competitive advantage is critical to a company's long-term survival.

This particular problem is compounded with high employee turnover during times of uncertain economic environments. This logic becomes fatal when long-term employees begin retiring and that tribal knowledge is lost forever. It has become all too common to witness companies, in an effort to cut costs, offering earlier retirement (or worse) to long-term experienced employees so that they can replace them with younger, inexpensive new employees. What these companies fail to realize, until it is too late, is that this strategy severely backfires as decades of experience and tribal knowledge walk out the door with the employees. Many of the businesses that have not survived the recent economic cycles were companies that had been successful for 30+ years, until several "Larrys" began to retire. Others that have survived have never fully captured all of the tribal knowledge that left with their best employees.

> ***What these companies fail to realize, until it is too late, is that this strategy severely backfires as decades of experience and tribal knowledge walk out the door with the employees.***

Training Records

Ironically, the companies that have the best-trained work force many times have the weakest system. Most PCB fabricators do a tremendous amount of training, but do not take credit for it. A common mantra I like to repeat in my columns is "If you can't prove it, it didn't happen!" If you take the time to flowchart your daily non-production processes, you will be surprised by the amount of informal training that takes place on a daily basis. Develop a simple method of documenting ALL training that takes place—a training record. Whether part of an elaborate electronic system, or a simple paper document, complete a training record at every opportunity. (Side note: as with any system in this business, the more complicated you make it, the higher the potential for failure.)

Every day is filled with training opportunities; be sure to take credit for these opportunities by documenting them. Every time that you sit down with an employee to discuss (written or verbal) a recent mistake, customer complaint, or simply work through a potential process improvement is a training opportunity. Take five extra minutes and record it.

Certified Operator Program

This is an integral part of the training program that is also often overlooked. It simply is not acceptable to a customer for a supplier to rely strictly on OTJ training. There needs to be some method of demonstrating your employees' understanding and competence as it relates to the job(s) they are performing. This is of particular importance when a company utilizes cross-training and moves people around between departments to adjust to workload fluctuations. Annual recertification is also a must; it simply is not very effective if the procedure has changed revision numerous times since the initial certification. There has to be a high level of confidence in workforce competency, and a certified operator program is the appropriate method. Figure 1 shows how a sample certified operator process map might look.

I will end this column as I began it, with another timeless quote. Perhaps Confucius was speaking about the importance of participative employee training when, 2,500 years ago, he stated, "What I hear, I forget. What I see, I remember. What I do, I understand." **PCB**

Steve Williams is the president of Steve Williams Consulting LLC and the former strategic sourcing manager for Plexus Corp. He is the author of the books, Quality 101 Handbook and Survival Is Not Mandatory: 10 Things Every CEO Should Know About Lean. To read past columns, or to contact Williams, click here.

PCB007 Supplier/New Product News Highlights

Camtek Sees $85.4 Million in Revenue

Revenues for the fourth quarter of 2013 were $23.3 million, a 7% increase from prior quarter revenues of $21.7 million and a 32% increase from fourth quarter 2012 revenues of $17.6 million. The increase is mainly related to a more favorable environment in the semiconductor market.

Isola Debuts Ultra-low Loss Materials

Tachyon laminates and prepregs are engineered to improve performance of high-speed digital designs by producing a very low dielectric constant and insertion loss. The product is specifically targeted for high-layer count backplanes for the growing 100 gigabit per second (Gbps) market with channel data rates in excess of 25 Gbps.

Invotec Wins Formal ESA Approval

The company is delighted to announce it has been formally awarded ESA approval—the first PCB supplier to achieve such approval in many years. Invotec already has a rich space heritage, manufacturing HDI and HDI flex-rigid boards for a variety of ESA and non-ESA space programmes to OEM specifications which, in many cases, go beyond current ESA approvals.

Excellon Installs COBRA System at Advanced Circuits

Excellon announces the installation of a COBRA Hybrid Laser Via System at Advanced Circuits, Inc. The Excellon COBRA Hybrid Laser System offers both UV and IR laser sources on one platform and a large work area of 31" x 25" for those companies running larger panel prototypes and production PCBs.

Rogers Intros COOLSPAN Adhesive Film

Rogers Corporation Advanced Circuit Materials Division launched COOLSPAN Thermally & Electrically Conductive Adhesive (TECA) Film, a thermosetting, epoxy-based, silver-filled adhesive film used to bond circuit boards to heavy metal backplanes, heat sink coins, and RF module housings.

Atotech Launches Green Electroless Copper Solution

With Atotech's new Ecoganth series, PCB and IC-substrate manufacturers are enabled to meet future technical, ecological, and legal requirements.

Agfa Reveals New Dealer Structure for N.A. PCB Market

Agfa's Specialty Products' management has revealed its new dealer structure for the North American PCB market. Under the new structure, Agfa's customers will be served by three dealers: Matrix Electronics Limited (Santa Ana, California/ Mississauga, Canada), Allen Woods & Associates (Arlington Heights, Illinois), and East Coast Electronic Material Supply LLC (Manchester, New Hampshire).

Enigma Interconnect Installs Acu-Gage Measuring System

Acu-Gage Systems has announced that Enigma Interconnect has installed an automated 24" x 24" Acu-Gage System at its corporate manufacturing operation in Burnaby, BC. The Acu-Gage is configured with automated edge detection, full 3-axis motion control, programmable illumination, auto focus, programmable zoom, and Windows-based programming software.

Sunshine Employs Frontline's InPlan Engineering System

Orbotech Pacific Ltd., the Asia Pacific subsidiary of Orbotech Ltd. has announced that Shenzhen Sunshine Circuits Technology Co., Ltd., a leading PCB producer in Shenzhen, China, has fully applied the InPlan engineering system developed by Frontline PCB Solutions.

Arlon Materials: Expanded Partnership with CCI-Eurolam

Arlon has expanded its long-term partnership with CCI-Eurolam to include distribution of Arlon's extensive microwave product Line in France. CCI has been a distributor for Arlon's Electronic Substrates products for more than 25 years.

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7 Tips for Choosing the Right Test Service

by Todd Kolmodin

Do you need to go outside your company for your testing service? Maybe you have temporary capacity issues, or maybe your own equipment is down, or maybe you just want to make sure you have an established back-up plan that will be there when you need it? Whatever the reason, it is very important to choose the right outside testing service, because ultimately, you are not just choosing an objective service provider; you are choosing a partner. And not just any partner, but one that represents your product and company in the best possible light.

Therefore, it is important to carefully and diligently select the service bureau that is going to best meet all of your needs. To help you do just that, here are seven things to consider:

1 How does the place look? Does it look professional, well managed, clean and organized? Does the equipment appear to be in good working order? Does the work look like it is organized? Are the panels properly stacked? How do they handle issues? This is the time to pay close attention to detail. I even check out the bathrooms to make sure they are clean; a quality auditor once told me that this is the first place that he looks when going into any facility to do an audit. He told me that nothing reflects the care and concern of an organization better than the way they keep their restrooms. These things should give you a pretty good preview of what the service bureau is really like.

2 Take a close look at their equipment. Is it modern and up-to-date? If not all new, is it well maintained? Has the equipment been calibrated recently? Do they perform preventive maintenance on their equipment? There is nothing worse than going to an outside service because your equipment is broken down, only to have their equipment break down. I mean, what's the point of a back-up, after all? Do they have traceability from the panels they have tested to the equipment it was tested on? This is critical!

3 Speaking of traceability, check out their record keeping and ask to take a look at it. This could be the most important part of your survey. Here's an important rule of thumb: Their record keeping should be better than yours. In fact, their entire test operation should be better than your test department. It should be; they are the experts and they are supposed to be better than the rest of us.

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4 Check out the staff. Do they have enough people, and are they properly trained? Find out what their training program is. Do they require a certification process for their test technicians? Speak to their technicians to get a feel for their level of professionalism.

5 What about certifications like ISO? It is important that your test partners are ISO-compliant; at least that way you know that they have written procedures that they follow on a regular basis. Check out their ITAR registration, if they have it. If they don't, then make sure that they are ITAR-compliant because, if they are not, then you are not, and that may result in a serious problem for you.

6 Determine their capability for getting your boards tested and back to you in a timely manner. What are their lead times? You don't want your boards to take longer than 24 hours to test. Ask to see their records to ensure they can deliver on their promises.

7 Finally, consider their attitude. As I said earlier, you are not hiring a service as much as you are engaging a partner. Choose carefully, and make sure these are people you are going to enjoy working with. They should be open and honest and give you a good feeling about them. This is critically important; you need to ask yourself if you can trust these people to go the extra mile for you when that time comes.

If you follow these guidelines when choosing your test service bureau, you will do fine, and in the end you will not only have a good test partner but you will actually have an extension of your own board house, in the form of an outside test department that complements your internal test department perfectly.

Try it out…put it to the test. **PCB**

Todd Kolmodin is the vice president of quality for Gardien Services USA, and an expert in electrical test and reliability issues. His new column, Testing Todd, now appears monthly in The PCB Magazine. To contact Kolmodin, click here.

Improving Electronic Devices Using Holograms

Researchers from the University of California, Riverside and Russian Academy of Science have demonstrated a new type of holographic memory device that could provide unprecedented data storage capacity and data processing capabilities in electronic devices.

The device uses spin waves, a collective oscillation of spins in magnetic materials, instead of the optical beams. Spin waves are advantageous because they are compatible with the conventional electronic devices and may operate at a much shorter wavelength than optical devices, allowing for smaller electronic devices that have greater storage capacity.

"The results open a new field of research, which may have tremendous impact on the development of new logic and memory devices," said lead researcher and UC Riverside Research Professor Alexander Khitun.

A paper, "Magnonic Holographic Memory," which describes the finding, has been submitted for publication in the journal Applied Physics Letters. An advance copy of the paper can be accessed here.

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BAE Systems
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MIL/AERO MARKETS

Foreign Military Sales: Back to the Future for Sales Opportunities

John Vaughan
CIRCUIT SOLUTIONS LLC.

Against a backdrop of depressed U.S. economic conditions across all industry sectors and a pullback in funding needed to grow our businesses since at least 2009, coupled with the offshoring of many circuit manufacturing opportunities, these are truly challenging times to operate a U.S.-based printed circuit board manufacturing or electronics contract manufacturing operation.

Over the past decade, the military/aerospace sector has transitioned from a period of accelerated DX-rated contract manufacturing in support of our country's multiple war efforts to a post-war period. We are currently in the midst of the attendant phased pull-out of troops, and have warily watched our inconsistent and at times recalcitrant Congress paralyzed by inaction. Those of us doing business in this sector have also navigated government funding shutdowns and tried to optimize our operations in advance of the looming indiscriminate sequestration defense budget cuts. Alas, we have now been presented with a $1 trillion omnibus spending bill that largely negates those cuts near term, and in fact provides funding greater than the Pentagon's sequestered budget request. Like me, your initial response may bring to mind the ubiquitous text response, "WTH?" But I would like to explore the current military circuit board business environment in a slightly more mature fashion and pose a key question for us all to consider.

As business executives, how do we operate, navigate and manage a military/aerospace-oriented circuit board shop or CEM operation in such an unstable and unpredictable environment?

The lifeblood of any circuit board or CEM, or any business for that matter, is a predictable and profitable sales backlog. Key to capturing and maintaining mil/aero customer and program opportunities, and thus providing a stable backlog that provides an opportunity to plan and to grow, is fully understanding the mil/aero market and the status of customers and their programs at a very intimate level. Equally important is to understand the DoD funding associated with each of the programs you support.

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A critical part of H&T Global Circuits' competitive advantage was the early development of a global manufacturing strategy. Production operations in both Germany and the Middle East provided the foundation for expansion in the world market.

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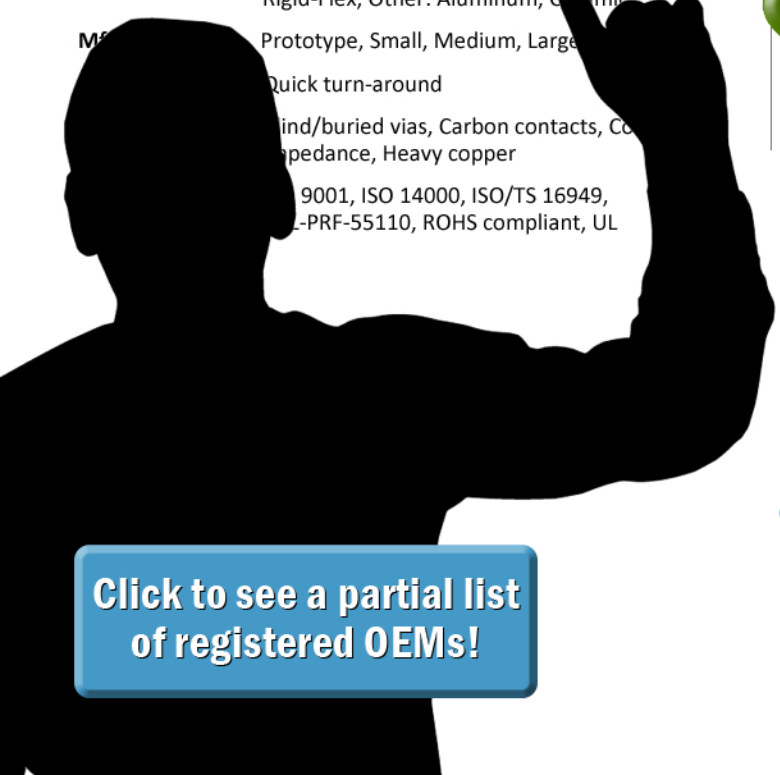

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It may surprise many to learn that the mil/aero prime contractors are actually prospering in the current environment, and in fact, the industry actually performed much better than the broader market in 2013. Several factors are driving their current success. Certainly, cost cutting in advance of sequestration at the operational level has contributed to their profitability, and years of consolidation in the sector has narrowed the competition—and they have very diverse operations—but the chief factor driving the growth is their participation in the foreign military sales (FMS) program.

For those unfamiliar with this, the U.S. DoD FMS program facilitates sales of U.S. arms, defense equipment, defense services and military training to foreign governments. In this scenario, the purchaser does not deal directly with the defense contractor; instead, the Defense Security Cooperation Agency (DSCA) serves as an intermediary and handles procurement, logistics and delivery. Currently, America's allies in Asia are increasing their expenditures due to the China threat and in parallel with higher defense spending by China.

Tracking FMS trend spending is important to PCB and CEMs because all of the electronics contained in the aircraft, the radars, the ordnance, guidance systems and the communications systems being procured through the FMS program are largely legacy systems.

This, of course, means that many of us have already tooled up and previously produced either circuit boards or circuit card assemblies at the sub-component levels for our military prime customers.

There are many examples of FMS spending for us to examine, but if we look solely at the venerable F-16 Fighting Falcon multi-role fighter aircraft, we can begin to understand some tremendous opportunities. Produced by Lockheed Martin, the F-16 is the world's most prolific fighter with more than 2,000 aircraft in service with the USAF, and another 2,500 operational in 25 additional countries.

In addition to the outright aircraft sales, the market for upgrading the electronics suites in the existing fleets of participating FMS countries is in rapid growth mode. Last year, BAE Systems finalized a deal worth over $1 billion to upgrade over 130 South Korean F-16 fighters, and the company seeks additional orders in Europe and Asia. Just three weeks ago, the DoD notified Congress that it had approved the sale to Singapore of upgrade packages for 60 F-16s for an order valued at $2.43 billion. DSCA indicates the upgrades would provide Singapore's F-16 fleet advanced radar systems, new global positioning systems (GPS), newer friend-or-foe identification systems, and an array of newer weapons to include laser-guided bombs.

In an interesting sidebar to the deal, BAE Systems, who has been a key supplier at the subassembly level for Lockheed Martin on the F-16 program, seeks to compete against Lockheed Martin for the upgrade deal.

Depending upon the configuration and approved upgrades for each country's version of the F-16, electronic content could include the Lockheed LANTIRN infrared navigation and targeting system, a BAE Systems holographic display, HARM targeting system from Raytheon, or ordnance systems, radar and jamming systems by a plethora of the primes to include ITT, Northrop Grumman, Rockwell Collins and many others.

Do your due diligence research, be informed and check in with your customers in the mil/aero sector that participate on the F-16 program. The chances are very high that there are either current requirements, or requirements planned near-term for circuit boards and assemblies that you are already prepared to support.

I appreciate your feedback. With your input, we can explore areas based upon your interests to help grow our businesses, while strengthening the United States defense industrial base as it pertains to PCB manufacturing and electronics contract manufacturing. **PCB**

John Vaughan is president of Circuit Solutions LLC., based in the Washington, D.C. metro military market, and a provider of integrated supply chain and program management solutions to the military C4ISR, unmanned systems and IED detect and defeat communities. To contact Vaughan, click here.

IPC 2014 Events

Mark your calendars now for IPC events in 2014! While many of the programs are being finalized, you can sign up today to receive updates on select event news and special promotions as they become available.

SIGN UP FOR EVENT UPDATES

March 23–27 | MEETINGS & COURSES
March 25–27 | CONFERENCE & EXHIBITION
IPC APEX EXPO®
Mandalay Bay, Las Vegas, NV, USA

April 18 | Woking, England
April 21 | Riesa, Germany
April 23 | Stuttgart, Germany
IPC & EIPC Failure Analysis and Reliability Testing Roadshow

May 7–9
ECWC 2014
Nuremberg, Germany

May 19–22
IPC APEX India™
Bangalore, India

May 28 | Singapore
August 20 | Penang, Malaysia
Southeast Asia High Reliability Conferences

June 10–11
IMPACT 2014: IPC on Capitol Hill
Washington, D.C., USA

September 28–October 2
IPC Fall Standards Development Committee Meetings
co-located with SMTA International
Rosemont, IL, USA

October 14–15
IPC Europe High Reliability Forum
Düsseldorf, Germany

October 28–30
IPC TechSummit™
Raleigh, NC

November 18–20
Cleaning and Conformal Coating Conference
sponsored by IPC and SMTA
Schaumburg, IL, USA

December 3–5
International Printed Circuit and APEX South China Fair
(HKPCA and IPC Show)
Shenzhen, China

Questions? Contact IPC registration staff at +1 847-597-2861 or registration@ipc.org.

TOP TEN

PCB007 News Highlights This Month

1 American Standard Circuits Earns "Manufacturer of the Year"

U.S.-based circuit board manufacturer American Standard Circuits (ASC) has been awarded "2013 Manufacturer of the Year" by the Alliance for Illinois Manufacturing. The award is intended to showcase a company that serves as a testimonial to the Alliance's integrated business delivery model.

2 Viasystems Reports 10.9% On-year Sales Growth

"We finished the year with some positive momentum that sets us up to continue to make progress on our cost structure in 2014, but in many ways I am glad that 2013 is behind us," said David M. Sindelar, CEO. "During the past year, we have worked through a number of challenges, including factory relocations, recovery from a fire in one of our largest factories, and new project launches, not to mention the economic pressures from reduced government spending."

3 Invotec Wins Formal ESA Approval

The company is delighted to announce it has been formally awarded ESA approval--the first PCB supplier to achieve such approval in many years. Invotec already has a rich space heritage, manufacturing HDI and HDI flex-rigid boards for a variety of ESA and non-ESA space programmes to OEM specifications which, in many cases, go beyond current ESA approvals.

4 IPC: North American PCB Sales Continue Slow Recovery

"North American PCB sales in December continued their slow recovery, while orders have been volatile," said Sharon Starr, IPC's director of market research. "In the current cycle, the book-to-bill ratio appears to have hit its low point in November and is now beginning to climb again."

5 Chinese PCB Firm DPMC Refutes Bankruptcy Rumors

China-based printed circuit board manufacturer Dalian Pacific Multilayer PCB Co. Ltd (DPMC) has denied rumors that the company is going bankrupt.

6 IPC APEX EXPO 2014 Proves Leadership; Space Sold Out

To visitors, the sold-out status means that the show floor will be busy and informative, with more than 425 exhibitors introducing new product technologies, innovations and demonstrations of the industry's newest advancements, many of which will also be highlighted in the dedicated New Product Corridor on the show floor.

7 MFLEX Doubles Sales to New Customers

Reza Meshgin, CEO, commented, "Net sales to our newer customers more than doubled sequentially, and are expected to represent approximately 23% of total net sales. Looking ahead to the fiscal second quarter, we expect a significant sequential decline in net sales that we anticipate could approach 40%."

8 Dragon Circuits Intros Pure Gold LPC for Medical Circuits

Texas-based circuit board manufacturer, Dragon Circuits (DCI) has announced immediate availability of their Pure Gold LCP, 100% pure gold traces plated on liquid crystal polymer (LCP) without the use of copper-base metals.

9 TTM Reports Strong Q4 and FY 2013 Results

"We delivered strong results for the fourth quarter as seasonal revenue growth combined with solid execution resulted in increases in gross margins and operating profit," said Tom Edman, CEO. "Strong demand for our advanced HDI and rigid-flex PCBs drove our product mix shift toward advanced technology PCBs and brought our Asia Pacific factory utilization rates above 90%."

10 Global Flexible PCB Market to Reach $12.686B in 2015

The FPCB market was valued at $11.321 billion in 2013, up by 9.4% year-on-year. In 2013, the most significant change in the industry was in the slumping profit margins of veterans and the soaring profit margins of new entrants. Market veterans lagged behind new entrants in equipment and technical R&D strength, according to market analyst Research in China.

EVENTS

For the IPC Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For the iNEMI Calendar of Events, click here.

For a complete listing, check out PCB007's full events calendar.

NORDIC HDI 2014
March 5–6, 2014
Copenhagen, Denmark

Houston Expo & Tech Forum
March 6, 2014
Stafford, Texas, USA

SMTA Webtorial: Tin Whiskers—All You Should Know
March 11 and 13, 2014
Online

Electronics New England
March 26–27, 2014
Boston, Massachusetts, USA

Printed Electronics Europe 2014
April 1–4, 2014
Berlin, Germany

Internet of Things and WSN Europe 2014
April 1–2, 2014
Berlin, Germany

South East Asia Technical Conference on Electronics Assembly
April 8–10, 2014
Penang, Malaysia

Intermountain (Boise) Expo & Tech Forum
April 17, 2014
Boise, Idaho, USA

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