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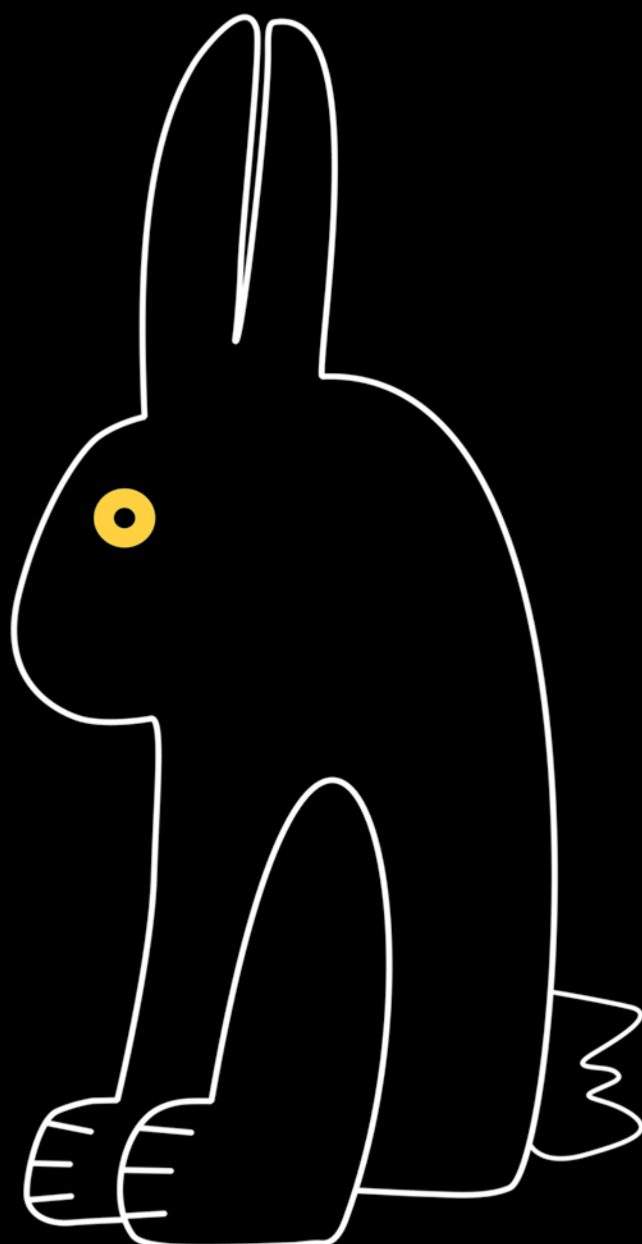
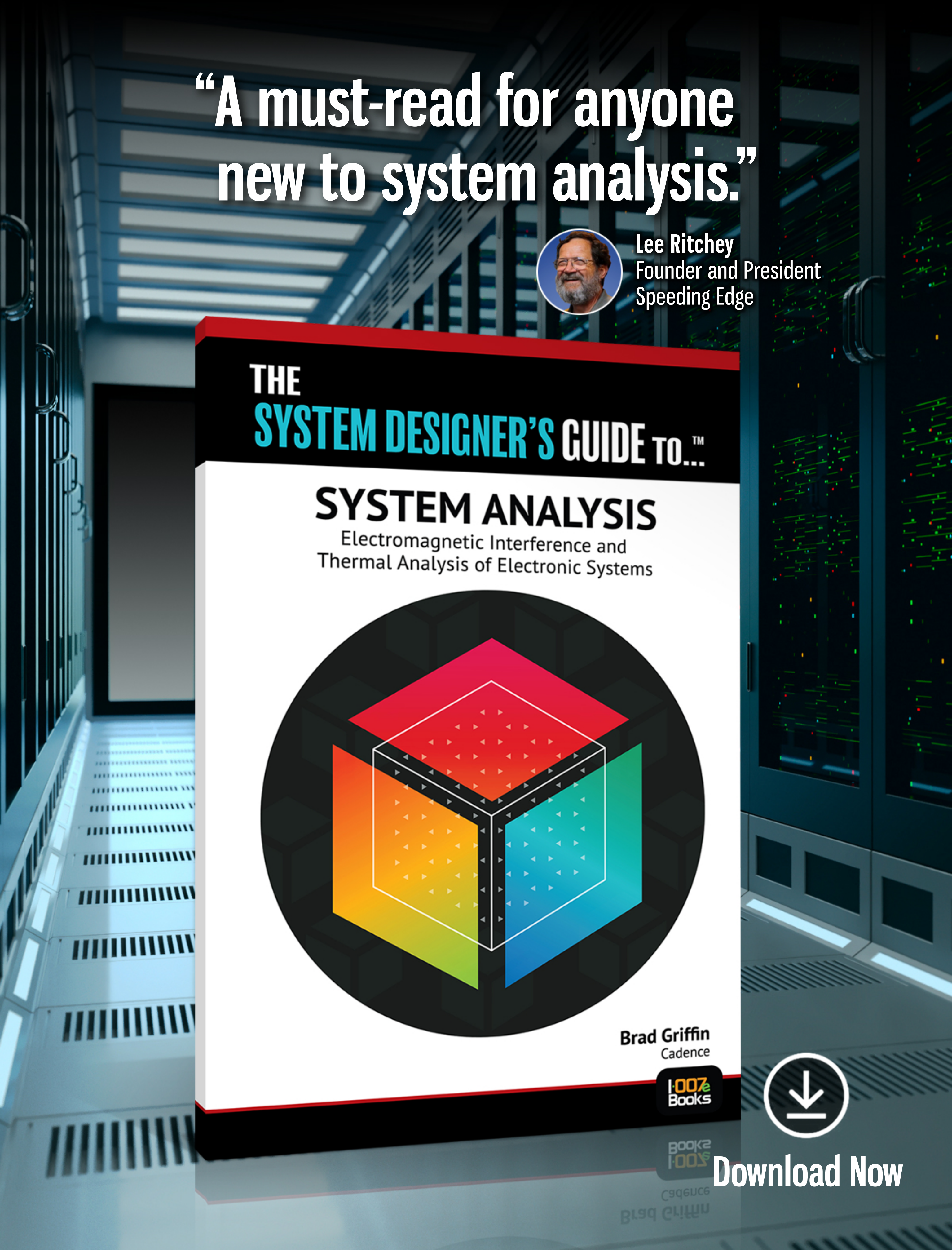


DFM: From a Fabricator POINT OF VIEW



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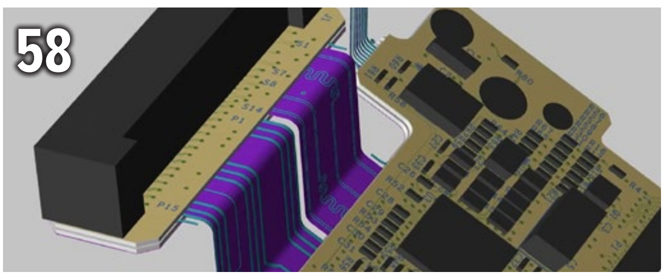


FEATURES

PCB007 MAGAZINE

DFM From the Fab Point of View

The Shaughnessy Report

by Andy Shaughnessy, I-CONNECT007

When we started planning this issue, we had no idea it would result in flipping DFM on its head. But consider this: When you think about DFM, what's the first thing that comes to mind?

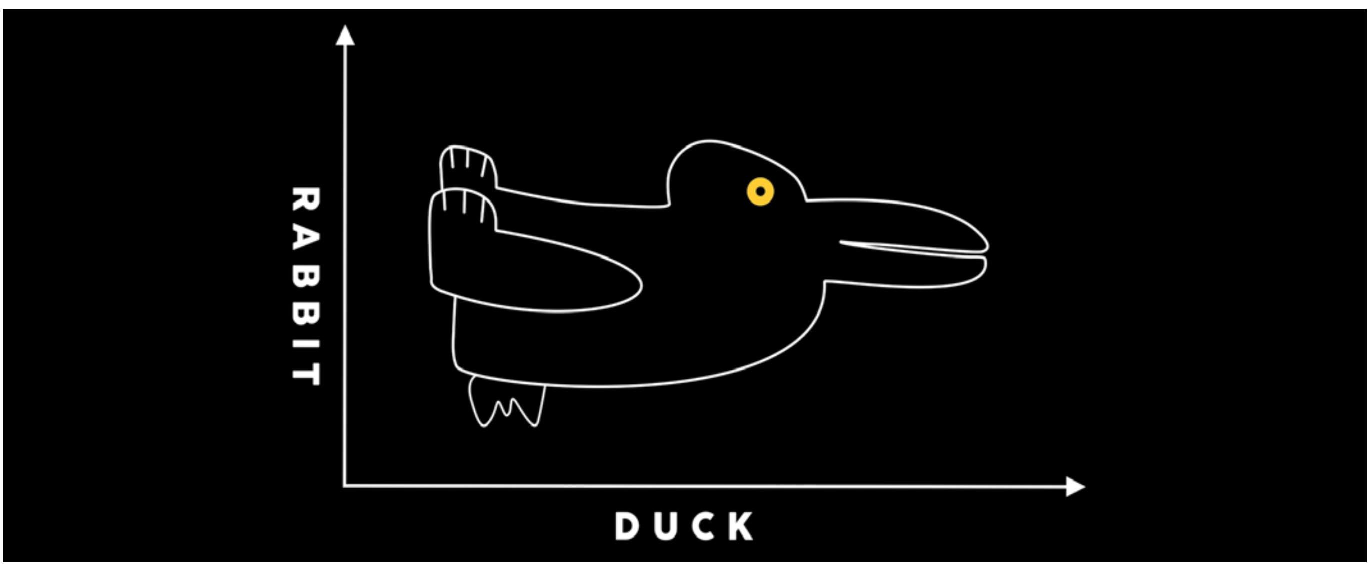
Most of us immediately think about steps that PCB designers and design engineers should take to ensure that their designs are easily manufacturable by their fabricators. And DFM errors are generally seen as the responsibility of the designer; when the CAM operator finds discrepancies in the BOM, acid traps, or impedance mismatches, he knows who to blame.

The whole push for DFM practices came about in the first place because designers were laying out boards that could not be manufactured. It only makes sense that DFM would be driven by the fabricators who must do the actual manufacturing.

In the past few decades, there have been numerous discussions about proper DFM practices, mostly focused on the PCB designers' need to understand more about the fabrication process. This is a fair point. Many designers haven't seen the inside of a board shop in 25 years, if they've ever visited one.

But despite years of talk about DFM, these problems remain, and they're getting worse. In our surveys, designers and fabricators frequently point to DFM issues as their biggest challenge. Designers will often defeat the most cutting-edge signal integrity challenges but make simple mistakes in the data handoff—usually a designer's least favorite part of the process.

And there are often zero consequences when designers don't follow DFM guidelines. Designers know that they can hand off data packages that are incomplete or full of errors, and



the CAM department will work its magic—because the fabricators want to keep getting jobs from that customer.

As we learn this month, because the fabricators want to get the job, they wind up allowing designers to keep making the same DFM errors. It's a lot like an enabling relationship. I can imagine Dr. Phil looking at both parties and saying, "What on earth were you thinking?"

There's room for improvement on the fab side. We hear one common cry from designers: Fabricators don't like to share their information. In recent Design007 surveys, PCB designers and design engineers complain that many fabricators will not share their technical capabilities with them. Some fabricators will direct designers to their website, but as one designer pointed out, "What does 'advanced' really mean?"

It turns out that DFM is actually a bi-directional concept, which leads us to our August topic. This month, we asked a variety of contributors to turn DFM around. What does DFM mean from the point of view of the fabricator? Should PCB fabricators share more information about their technology capabilities? What are the fabricators' responsibilities in this delicate dance?

We kick off with an interview with CAM veterans Dana Korf and Mark Thompson, who detail the current designer-fab relationship and what needs to happen for the industry to embrace true DFM practices. Vince Mazur discusses why today's designers must design boards with the end-product in mind, and how DFM itself is evolving. Joe Clark, Rick Almeida and Max Clark point out the need for reluctant designers and fabricators to be open to changing their DFM processes. Chris Clark explains why flex designers and fabricators must work together as one solid team. We look at some of the results and comments from recent I-Connect007 DFM surveys. And Karel Tavernier discusses Ucamco's recent move to add Mandarin notes to the Gerber job editor.

The struggle for true DFM is likely to continue, but early communication between designers and fabricators can lower the risk factor for both sides. As we've learned over the past crazy year and half, we're all in this together, and we can overcome most hurdles if we communicate with each other.

Speaking of communicating, try to get to a trade show or conference and talk to some of your designer customers. There's no substitute for having a conversation in person. We'll be covering PCB West, PCB Carolina, and IPC APEX EXPO. I hope to see you there! PCB007

Andy Shaughnessy is managing editor of *Design007 Magazine* and co-managing editor for *PCB007 Magazine*. He has been covering PCB design for 20 years. He can be reached by clicking here.

A Fabricator's View of DFM Processes

Feature Interview by the I-Connect007 Editorial Team

In this experts interview, Dana Korf, Mark Thompson, and Happy Holden discuss DFM, but not from the designer's point of view. Instead, we wanted to know what DFM means to the fabricator. They delve deeply into the complicated exchange of information between designers and fabricators, the role of software tools in this formula, and why the entire industry revolves around checking incoming data.

Andy Shaughnessy: Dana, what would you like to see as far as DFM from the fab side?

Dana Korf: Everyone knows my view. I'd like DFM to just go away. It's a non-value-add function from a Lean standpoint. I was with a customer last week and we talked about this. I said, "I wish we could go back to the '70s when we took a design from our OEM, we built it, and we sent the board back to him." Right now, we must assume that the data is bad coming in. And what does "bad" mean? I break it into three elements. One, the fabricators are not good at giving the designers the rules that they want, that the engineering group uses to design against. Second, the software tools actually can't even include all the rules that are used to review a design.

Third, we still use non-intelligent data, the Gerber exchange methodology, instead of more intelligent methods like ODB++ or IPC-2581. So, there's a lot of manual intervention interpreting data. And we send duplicate data out. They will send a Gerber and an ODB file and they're different. Which one is right? We'll send a fab print and the Gerber data. They conflict, so which one is right? So, fabricators must assume the data coming in is not good.

My experience talking to people in this area is 90-95% of the data packages need to be modified or at least should be questioned. I've never met a designer who intentionally designs bad. It's the design knowledge transfer system that's the problem.

Mark Thompson: I agree with Dana. The problem with IPC-2581 from a fabrication standpoint is that you are obligated as the fabricator to review all the sets of data that are included.

So, if they include 274D, 274X and ODB, and as you said, there's a flaw in one of those three, we need to catch it; therein lies the rub. The CAM operators don't like having to look at three sets of data. They'd much rather have one set of data like the '70s again. Send us Gerber data, ODB, or whatever you're going to send, but just send one of those.

Nolan said earlier, "Share your capabilities with the world." Now as an FAE, I was constantly getting questions, such as, "Can you provide us with your Valor ERF settings?" Well, we had a problem doing that. We'd much rather they look at the capabilities published on the website as opposed to providing them with a spreadsheet of numbers that have no rhyme or reason. I had a conversation with a guy from an aerospace company about a month ago. He said, "Mark, it would be a whole heck of a lot easier as a designer if all fabricators provided us with their ERF settings for Valor." I said, "Yes, it would, but that doesn't allow the fabricator to no-bid based on intangibles."

So, if you had a situation where you send them their ERF settings and it meets all your ERF settings, but the quantity is too large, or there are six or seven different caveats and it exceeds the amount of heartbreak, if you will, the fabricator would like to no-bid. But if you send him those ERF settings, then they're going to come back and they're going to say, "Well, it meets all your ERF settings." That is one problem.

The other side of that is, what if you don't provide them those ERF settings, and you just rely on them to look at your capabilities page on your website? They're not very straightforward, and a lot of them are convoluted. Honestly, look at them. What is "advanced" and what is "standard" exactly? Define them. That ends up being a bit of a problem as well.

Dana Korf

Happy Holden: The reason that I dislike the term DFM is that what Valor sells is design rule checking, not DFM.

Korf: Exactly.

Holden: I managed the software engineers for Mentor. They were in Poland, and these are brilliant guys who write the EDA software, but they had never been to a printed circuit shop. So I arranged one day to take them all over to Krakow to visit a fabricator.

You've never seen such upset, disturbed engineers in your life. Maybe they thought this was going to be an ultra-modern clean place with bunny suits. Instead, they find vats of acids and other things going on there.

Korf: I developed a course for IPC on DFM. One of the key elements I put in there is, what is DFM? When a fabricator opens that file, what is in their mind? And what are you trying to do? One of the most important requirements is that the board must work when it gets shipped to the customer. One key element is you're trying to get the lowest cost maybe, or maybe not. And then, what does that mean? Well, you're trying to use the cheapest materials that won't negatively affect the design performance.

The process steps are pretty much well-defined, you can't really add or delete process steps that often. And then you must make sure the data will yield whatever the intended yield is for that product, to Mark's point on technology. You open a file, and you look at the impedance. I'm going to modify the line widths and release it very quickly, but the modifications may not work within the SI noise budget.

And none of the software that you have—even the software tools you're mentioning—really have an automated check that checks everything. It doesn't exist out there. I worked with a large CAD software company and I said, "Here are the design rules for routed edge trace and scored edge trace to punched edge." They're going, "We only have trace to edge." Those three profiling methods may have different rules, but they can't even check it. Probably about half of the rules that I went through with them don't exist.

Mark Thompson

Holden: And that technology can change so rapidly in so many different directions. The only place where it comes together is at the fabricator.

Korf: Each fabricator can have a different set of rules based on how their factory process is and the rules that govern it. One OEM challenge is how to integrate the multiple sets of rules into a common set for the designer.

Holden: And each OEM is pushing for some direction other than what another OEM is. And fortunately, the assembly industry is diverse enough to have specialists, but the fabricators, through consolidation, come together in a much smaller group of people. Especially in prototype, we're down to 290 facilities in North America from what used to be 3,000, and those 290 have to do more variety to handle the increasing number of OEMs, and the permutations and combinations that come together. And no DFM software or sets of ERFs can cover all the different ones. It still comes back to that CAM engineer.

Thompson: CAM operators are very literal people. So don't induce rounding errors by mixing Imperial versus metric. If you're exporting your drill format as 2:4 trailing, and you output your Gerber 2:6 leading, it takes a little while for the CAM operator to fish through those things and figure out what is the actual format to be able to place that data. Additionally, there are those discrepancies, those rounding errors, that happen for drawings. For instance, if you call out an eight-mil line for 50 ohms, and you actually output it as 0.2 millimeters, and it's true, it's 0.0078." So what is that 0.0002" going to do to the impedance? Probably nothing. But as a very literal person, such as a CAM operator, they're going to look at it and say, "There aren't any eight-mil traces." Then they're going to make a phone call, and it's going to waste time.

Holden: The thing I used to love the most was in China reading all the manufacturing instructions that are in English, and the CAM engineer is constantly asking you what this means because people weren't using proper English. They're using slang or undefined terms that hadn't been defined by the IPC yet. I was trying to emphasize to everybody that, although you understand the English, to get it translated into Chinese, it may not be the same. But if you translated English into German or Russian, it will have exactly the same meaning.

Korf: I worked in China for many years, where front-end engineers are working in non-native languages. For example, you have an engineer in France whose native language is French. He translates the TQ question or note into whatever version of English he learned—whether the queen's English, American English, Southern English, a French version of English. A Chinese engineer then interprets the note in the version of English that they learned and then into Chinese. Sometimes a planner would bring me a note from a customer, and it was in English. I'd read it and say, "I have no clue what they're talking about." And to your point, there's no such thing as Chinese in China—there are two basic languages, and then there are 21+ dialects on top of that.

Thompson: Case in point: app notes. I'm sure you've seen some crazy app notes. Some things that have been translated three or four different times and you read them and you're like, "That doesn't make any sense at all. Even the instruction doesn't make any sense."

Holden: And IPC-2581 is standardized so that we wouldn't have all these extra spreadsheets or Word documents. We could just refer to something in IPC-2581 that defines it for us.

Korf: We actually have a sub-team part of the 2581 consortium looking at fabrication notes now. Which ones can we make intelligent? Or, what additional attributes do we need to add to get rid of these non-intelligent notes? Because if you look at a fabrication print, to Mark's point earlier, the board outline a lot of times doesn't match the board outline in the Gerber file. And so you send a TQ back to the customer asking which one they want us to use. The extracted dimension doesn't match the fabrication print dimension. They say, "You use the one you extracted from the Gerber file." It's not uncommon to have issues like this.

To Andy's question earlier, my goal is to get rid of the drawing as an intelligent method of transferring the data and treat it as a report. Instead, send the information using attributes wherever it is in the design file. The drawing could be extracted from the data. There's software out there that can create a drawing if they want to have a picture or hard copy. So, why can't we send specs electronically too? There's no reason they must be retyped again.

Thompson: One of my favorite things that customers would say, they'd have a Class 3 job, and they'd say, "Well, go ahead and generate a net-list. At what point would I ever have a mismatch?" I don't think we really want to do that.

Shaughnessy: But it's interesting to talk about having too much data because one of the things we heard when we were doing our fab notes issue was that a lot of times the CAM operator doesn't get enough data. So is it feast or famine?

Korf: And/or it's conflicting.

Thompson: That's where the fab engineer comes into play. That's the person that must call and say, "Hey, what did you mean by this? What did you really mean by that note?"

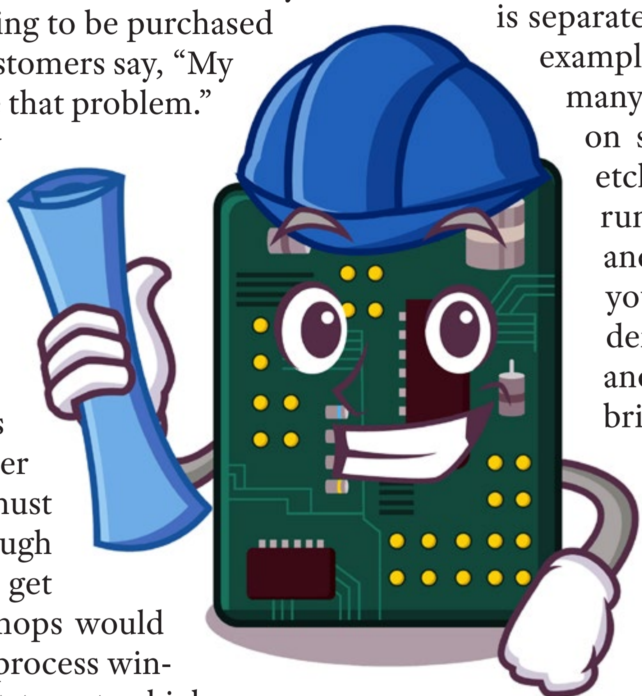
Shaughnessy: Right. One thing that came up in our survey is there's a disagreement among people as to whether DFM is a philosophy or a process. For some companies, DFM has become a philosophy.

Korf: I think it's a little bit of both. My opinion is, from a philosophical standpoint, everyone's assuming that the person receiving the data is going to run a DFM to check it. The whole industry is based on that premise. So, in that respect, it's a philosophy. If the philosophy was that they're going to build it the exact same way I send it to them, you don't need DFM. But the process of performing a DFM is definitely a process. To me, it's both.

Thompson: Good point.

Shaughnessy: That's interesting. If I give you data, I'm assuming that you're going to check it to make sure it's right.

Korf: They're assuming you're going to fix it. Why would I check it if it's right? Having worked in the volume side and proto side, it's often you get a job in Asia, like Happy said, from a prototype shop in North America. The prototype shop is being paid to get in and out quickly and make some money at it. They're not paid to necessarily make it low cost because they don't know where it's going to be purchased in volume anyway. So customers say, "My last fabricator didn't have that problem." I'll say, "You probably didn't need to check it. They didn't have to optimize the yields like we have to do when running volume, or their rules and capability were different." Prototype shops typically will have a wider process because they must run many designs through in very low volumes and get it out quickly. Volume shops would tend to have a narrower process window, so you can tailor it to get a high yield out of it. Kind of competing standards there.



Holden: I knew Steve Jobs, and I worked with Wozniak, and Apple actually had two different design organizations. One group worked with R&D to get the prototype in the first iteration out as quickly as possible. Then they had the second group whose job was to make it manufacturable and lower-cost. But two to four months later, competitors would reverse-engineer and start to copy them. Then, as they were looking at ramping up, Apple would introduce the second, more cost-effective design. Apple knew that getting to market first is not the same thing as cost in manufacturing.

Korf: Different goals. Then you overlay the fact that there are many companies purchasing from multiple vendors to get the best price. The design is done, so now you go pick your vendor. Well, it's kind of too late for that and do anything of real value to affect the cost or performance, and that's just real life. That will always be a problem.

Thompson: Good point. A good fabricator has both a test and validation department that is separate from manufacturing. An example of that would be that many manufacturers can cheat on stuff. Let's say you over-etch something, and you're running high in impedance at the TDR tester. Do you hand it back to the solder mask guy and he throws another coat on it, and you bring it down to 50 ohms? No. If you did something like that, then the board gets to the customer and they've got two boards in their hand, one that's built the right way the first time, and the second one that has that extra coat of solder mask. The other thing that happens all the time is customers call and ask, "What's the dielectric constant for P370?" It's as simple as that. I'd say, "Well, what speed? What dielectric?" It's an open-ended question.

Korf: Mark, I figured out the other day that teams I worked with have probably seen over a million different part numbers over my career. Impedance vs. operating and test frequency were always conflicting. Many years ago, a company I worked at said, "Timeout. We validate a board when we ship it out the back door. How do we validate it? We validate with a TDR, a fundamental frequency around two gigahertz, plus or minus."

We would tell customers, "You want the impedance at 64 gigahertz or 16 gigahertz? Go calculate it. I can only guarantee two gigahertz." And it's a broadband measurement, not a single frequency test. Every stackup report had a note at the very bottom of the picture, indicating what test frequency was used to calculate the reported impedance. Of course, some companies have VNA testing, but that's for very low volumes because it's a slow test. But we would just get ourselves out of discussions saying, "Sorry, I can't guarantee any other frequency than my TDR."

There are designers that get mad at you because some other fabricator asked more than you did. I had to fill out a corrective action for a customer because two fabricators asked three more questions than my team did. They wanted to know "Why didn't you ask these questions?" True story. In Asia, the customer's always right. It's the way they're trained, and so they don't want to get a customer mad by asking too many questions. They don't tend to challenge hierarchies and the people who pay your bills.

Holden: It takes many, many years to really understand PC board materials, and even then it's a moving target. My group oversaw the design manual that included material characterization, and we used to get constant complaints because it would take us six months to characterize the material because we would take samples from the lab every two weeks. It also included a second chart of temperature variations of the frequency of the signal and the effect of humidity on dielectric constant dissipation factors. Because too many times we had to troubleshoot some HP test gear that we couldn't operate in Louisiana in August, whereas the rest of the time, it seemed to work perfectly fine. Engineering never considered that higher humidity will affect the loss on their part for laminates.

Thompson: To Happy's point, as far as the temperature and humidity, at Prototron we had two facilities, one in Tucson, Arizona, and one in Seattle. Well, you can imagine the humidity in Seattle is such, but humidity in Tucson was vastly different, and trying to keep parity between those two shops was crazy. It was difficult for us, not to mention you not only have humidity, but you have individual press parameters from fabricator to fabricator. So, the press thickness of a particular ply of 1080 of P370 may be this at one for the fabricator, and then something else at a different fabricator, and yet something again at another fabricator.

Well, you can imagine the humidity in Seattle is such, but humidity in Tucson was vastly different, and trying to keep parity between those two shops was crazy.

Holden: That's not counting each particular innerlayer, or how much copper they etched off.

Thompson: Exactly. The nesting value based on the layers, the layer configuration. Is it a pure signal? Is it a split plane or is it a full plane? All those have different nesting values of that prepreg. Once it heats up and fills those voids in a signal layer, it's going to fill the maximum amount.

Korf: Just basics like impedance assumes a lossless line. If the TDR trace comes out flat, that's impedance. When you get down to 2.5 mil wide lines, the second that TDR hits the trace, it starts going up because it becomes lossy instantaneously. The customer will take a measurement and reply, "Your impedance is wrong because it measured 100 ohms." Yes, the trace becomes lossy at the source. You're adding impedance as you go along. You have to teach them that the only place you take the impedance is at what we call the launch point, exactly where it hits the board. That's the only place it's valid for this lossless test method. Many of engineers replied, "I didn't know that." Then they appreciate the feedback.

> You have to teach them that the only place you take the impedance is at what we call the launch point, exactly where it hits the board.

Holden: I just wonder; the electronics industry continues to grow and design tools are focused on helping people get designs faster. But we're not producing CAM engineers with the appropriate experience to solve all these problems. As I said, we've gone from 3,000 to 290 shops, and if you look in our magazines at the number of advertisements for CAM engineers, when does it come down to the fact that we have so few CAM engineers that the bottleneck is the front end?

Korf: Here's a part of the problem. CAM software is sold based on seats. If I'm a software supplier, I make money every time I sell a seat. So, re-designing the software to be more automated works against the current sales model because they'll sell fewer seats. We need a company to provide a fully automated tool generation process. This a fundamental problem in the industry that conflicts with the current business model.

Andy, going back to one of your original questions, my interest in digital twin is that it gets into automation. If they can really start to gather real-time process information, and compile it in a reasonable way, you can now update design rules on an intelligent basis in the company. Then real-time updates can be integrated into automated CAM processes to improve yield more quickly. Then if you extend this further, assuming relationships can be set up, those rules could be automatically passed back to the designer. Conceptually, it's on the right track.

Shaughnessy: Right. Do you think IPC-2581 is the best data standard going forward for DFM?

Korf: With 2581, there are two things. One is that it just transmits the data in an intelligent fashion. The second reason is that the new Rev C now has an embedded DFM function. You can embed the TQ questions in the data file along with the answers and store them in the data. Many times a fabricator receives a design, especially in volume. "Here's a design, and we've been buying it for seven years. We're transferring to Asia." Then a DFM is performed with a list of proposed modifications. It gets sent to the customer who says, "Oh, geez. The person who knows how to answer these died 10 years ago. We don't know what the right answers are." When the prior DFM reviews are embedded in the design, the knowledge will be transferred with the design and this problem is eliminated.

Holden: How many other companies are selling CAM software other than ADIVA?

Korf: I know five companies globally that sell CAM software around the world. There are probably 100 in China that I'm not aware of.

Holden: Well, Ucamco keeps modernizing Gerber for us. I wish they'd kill Gerber, but you've got a company that's focused on supporting

Gerber, so it's tough to shoot something. I keep asking, "Why should we use something that's 60 years old?"

Korf: I'm not worried about them still pushing it, but it's the user that's got to quit using it. I don't blame them at all. It's the users that have to move out of the 1960s and into the 2020s on data formats, right?

Holden: Dana, is there any chance that CFX will get modified so we can use it in fab automation?

Korf: I haven't heard of any movement by IPC along those lines yet. So, I don't know.

Shaughnessy: Is there anything that we haven't covered that you'd like to mention? Any big takeaways here?

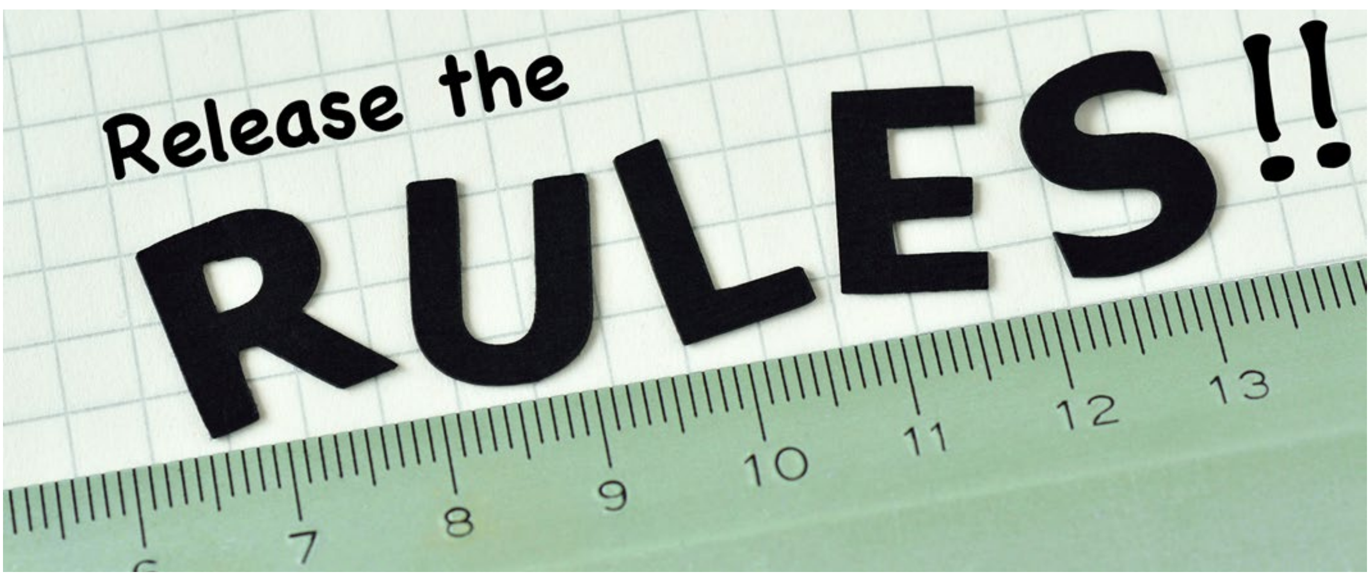
Korf: Andy, the summary from my standpoint is three-phased. What do we need to go forward? One, we need to get fabricators to release the design rules to the designers, so they could be designing against the rules that the designs are being checked against, and not consider it IP. They don't need to tell the designer how to build the board, just what the rules are. Then we've got to get people to quit using dumb data and use intelligent data, and that will grow over time. The third element is getting the CAD systems to build and accommodate all rules that would be given to them so the designer gets as much knowledge embedded in the system as they can. That's my answer to what needs to happen going forward.

Holden: Dana, one of the emails you sent me from China said, "You don't understand my problem. I've got 60,000 young engineers here that don't know anything about PCB design rules." And if they do, they find financing and create their own company because everybody wants to be an entrepreneur and be the boss.

Korf: The last Chinese city I worked in, Zhuhai, is next to Macau. They've built four brand-new large fab shops in that town since I left there almost two years ago. Where'd those front-end people come from? They're all brand new. It takes months to teach designers the fabrication rules and how to interpret customer data packages. That's a challenge. It's not something you can do in an hour-long PowerPoint presentation.

Shaughnessy: Thank you all for the great discussion. Lots of stuff to think about here.

Thompson: Thank you, Andy. PCB007



Designing With the End in Mind—How the Meaning of DFM Will Transform in the Future

Feature Article by Vince Mazur
ALTIUM

Introduction

The late American educator, author, businessman, and keynote speaker Stephen Covey coined the phrase, "Begin with the end in mind." He said, "To begin with the end in mind means to start with a clear understanding of your destination. It means to know where you're going so that you better understand where you are now and so that the steps you take are always in the right direction."

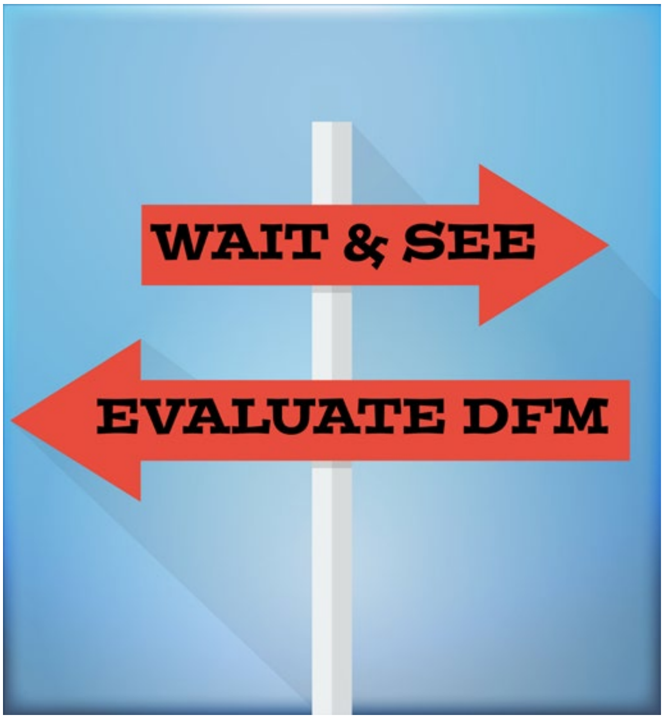
I recall a summer trip when a college buddy and I were on our return trek from the Havasupai campground area near the Grand Canyon. When we were almost to the top, we came across a solo hiker wearing jeans and carrying a camera, tripod, and a small bottle of water; he was about to make the eight-mile trek to Supai, Arizona. We suggested to the ill-prepared hiker to take more water, but the person chose to just continue. My friend and I looked at each other and said, "He's not going to make it." I am not sure how things worked out for that hiker, but I think you will agree that he was not prepared and that he certainly did not begin with the end in mind.

Designers of today's complex printed circuit boards occasionally encounter setbacks due to their lack of early planning. Such consequences for apathy in preparation and awareness will continue to escalate along the growth curve of complexity that the industry continues to experience.

In this article, I will offer a view of how designers can be served by a design for manufacturing (DFM) mindset to help assure first-pass success. I will also provide a glimpse of the potential future of board level design along with a discussion of how the adoption of new and uncharted concepts will assist the journey of electronic product realization that lies ahead.

DFM Fluency is no Longer Optional for PCB Designers

First pass, high yield, cost optimized, and reliable PCB fabrication and assembly is the target objective for PCB designers. Fall short of this outcome, and the consequences can be



quite substantial, including derailed new product introduction, sub-par profit margins, unreliable field performance, unnecessary rework, time-consuming redesign, and more. Compound this dynamic with the rapidly escalating complexity of today's PCBs, and designers find themselves at a crossroads: Either continue the prevailing "wait and see" feedback from manufacturing after committing a project or, with little overhead, proactively and authoritatively evaluate DFM as an inherent part of the designer's normal incremental PCB design process.

Some Design and Manufacturing Dependencies

As components are placed on a board, the design immediately inherits several design and manufacturing characteristics, such as component spacing and solderability, flying probe access, and more. All these characteristics can influence the fabrication and assembly of the PCB. In addition, the design also inherits characteristics of the parts that are largely outside of the designer's control. Some of these characteristics include availability, cost, life cycle, performance-to-datasheet, quality, and reliability. All these represent touchpoints of risk that, left unchecked, can derail product realization.

As PCB design progresses, manufacturing characteristics can be inadvertently created, such as acid traps and edge clearances that impact bare board fabrication but may have no impact on assembly. Likewise, without manufacturer-specific DFM checks at design time, boards can be fabricated to specification, yet cannot be assembled due to limitations of the target assembler. Any of these outcomes escalates costs and delays new product introduction. Care must also be taken even when changing existing designs. If not properly revalidated, simply replacing a component can have unintended consequences, and can prevent reliable volume manufacture. This single change can impact an entire assembly run. The resultant cost and time risks can be quite high.

In addition, while not typically associated with traditional DFM, component sourcing is becoming an increasingly significant area designers must pay attention to during the entire design process. If the components cannot be reliably procured, designs cannot be manufactured.

The Value of PCB Design with Full Spectrum DFM Awareness

The key to insulating designs from DFM issues is alignment of design rules and constraints with the capabilities of board fabrication and assembly providers. Once established, the rules and constraints constitute an over-the-shoulder auditor that is there to assure the manufacturability of the design. Issues created during design can be identified and corrected easiest at design time. The insurance that implementing DFM awareness within the design context provides can pay great dividends. Capturing manufacturing issues during the initial design also reduces the amount of time-consuming, development-plan deviating redesign. This frees designers to start new, exciting designs rather than trapping them in a quagmire of preventable redesign of projects that were previously considered complete.

Augmenting traditional DFM with "design for availability" of components is required to provide full spectrum DFM assessment. Designers can simply open their bill of materials (BOM) anytime throughout the design process and have immediate real-time insight into part availability. Components can be created with a number of ranked, alternative manufacturer part choices that can be automatically included in the BOM, if the primary part is unavailable. This process brings inherent resiliency to the component-sourcing aspect of design, allowing designers to remain focused on design, while providing early warning for part supply risks.

Bringing full spectrum DFM awareness forward into the design context, where it can be leveraged early and often, also has the secondary benefit of improving the designer's skill set. As issues are identified, the designer will gain exposure on how to avoid the actions that triggered DFM validation flags. When institutionalized across design teams, DFM awareness will improve the entire team of designers. This provides the best of both worlds, DFM resilience, with little overhead on the designer. In addition, as designers improve their DFM awareness, they increase their value in the industry.

'Understanding of Your Destination'

Referencing Covey's definition of beginning with the end in mind, it is paramount for designers to have a clear understanding of their destination. In the context of PCB fabrication and assembly, this implies having a comprehensive understanding of the capabilities of the chosen fabrication and assembly providers. Typically, this capability is detailed in a document available from the provider that must be migrated into a collection of rules and constraints applied within the PCB design environment.

Some manufacturers provide their capabilities in the form of a rules file that can be immediately used in the PCB design environment, but there is little consistency across the thousands of PCB manufacturers and assembly services across the globe. At the same time, PCB design, fabrication, and assembly complexity continue to escalate, and manufacturing capacity is getting tighter.

In assessing the future of board level design, one may want to consider the history of IC design. While the two areas differ dramatically in their targeted implementation of desired electronic system behavior, they share the same generalized, define–validate–implement design cycle. IC designers have had to be all but obsessed about their target fabrication process early in their design cycle. The library files they rely upon for the hardware description language (HDL) design compilation are deemed "signoff quality" by the IC fabricator and embody comprehensive details of their specific fabrication process. As HDL-based development generated design complexity quicker than it could be validated in the early '90s, improved design verification tools and methodologies were developed to fill the gap. The IC domain also shares some historical roots with board level design. Schematics were initially used for design, later to be replaced by HDLs and, yes, designs were submitted or "taped-

out" to fabrication and, when returned, implemented as an IC that did not function.

Today, it is well appreciated that with the very high non-recurring engineering (NRE) costs, IC design and fabrication is a "moon shot." The costs are so high that it simply must be right the first time. To achieve that objective, the industry adopted a collection of design methodologies and tools, enabled in part by multivendor support for library and design data exchange. This relatively open data exchange even included the portability of "rules-decks" used across competing physical verification systems. Out of necessity, the methodology considers fabrication aspects early in the design cycle.

While it is too simplistic to say that an IC is just a smaller version of a multilayer PCB, the comparison is not completely without merit. As PCB fabrication and assembly processes become more differentiated across manufacturing providers, PCB design will likely begin to embrace some of the same concepts that the IC design industry used to cope with complexity escalation.

While it is too simplistic to say that an IC is just a smaller version of a multilayer PCB, the comparison is not completely without merit.

Boldly Going Forward

The increase in PCB complexity, density, and edge speeds shows no sign of abating. Research is even underway on PCBs that use mixed copper and embedded polymer waveguides as interconnects. Combine this with more widespread use of package-on-package and other newer assembly techniques, and PCB manufacturing will become more of the art form than it already is. Just as semiconductor fabricators, such as Intel, Samsung, and TSMC are differentiated along the strength of their closely guarded fabrication IP, the same will continue to exert influence in the PCB manufacturing arena. Fabricators and assemblers will continue to be differentiated by their capabilities and proprietary IP know-how.

With a fully connected and data-enabled global ecosystem of fabricators and assemblers, as soon as the designer chooses a fabricator or electronics contract manufacturer (ECM), the designer gains immediate access into capabilities. Their design space would be immediately populated with the inherent rules and constraints that would need to be applied to their design, based on the capabilities of the target manufacturer. The concept is similar to how the preview in a print dialog changes when different printers are chosen. Choose a color-capable printer, and the preview changes along with available graphics resolutions, page size options and other printer-specific capabilities.

This data-enabled, global ecosystem approach moves manufacturing awareness much earlier in the design cycle where it can be leveraged through the product development process. This can lead to reduced or eliminated Zoom meetings and email threads, and much more awareness. Say an ECM adds a new pick-and-place line with greater capabilities; this awareness is immediately propagated to designers targeting that company, updating the rules and constraints for immediate leverage.

If a design is already completed, imagine a situation where you can take your PCB design and submit it, with a mouse click, to the global community of PCB fabricators and assemblers to find the best fit. The submission would return a list of companies that not only can manufacture the board, but can do so while satisfying criteria on factors such as lead-time, cost-target, current capacity, geography, etc.

While in a slightly different domain, there is a precedent for this type of paradigm. In the

early '90s, there were a variety of compelling programmable logic device (PLD) suppliers. All of them offered free tools that targeted only their specific devices. A start-up in Colorado Springs called Minc offered a product whereby the digital logic design could be described in either Verilog or VHDL—still the two most popular HDLs. The software had a comprehensive, vendor independent library of most of the programmable logic devices, detailing their capabilities and cost. The user could choose to optimize the implementation across a variety of tradeoffs such as speed, device count, vendors, and cost. With a mouse click, the design would be compiled and the software would find the best fit into the appropriate device(s). Many solutions used devices from multiple vendors. The designer then chose the best solution and moved forward in their process. Again, it was define–validate–implement, but the implementation was in a programmable device.

Conclusion

First pass, high yield, cost optimized, and reliable PCB fabrication and assembly are the goals; rapidly identifying and correcting DFM issues where they are created, in the design context, is key to avoiding the pains of releasing a design that cannot be manufactured. Augmenting conventional DFM checks with real-time component intelligence will help to eliminate surprise component shortages that are currently idling many assembly lines. This full spectrum DFM-aware PCB design sets the foundation for building a design process that is not only tuned for the challenges of design, but biased for the avoidance of downstream manufacturing problems that can impact profits, product development timelines, and industry reputation. As complexity continues to increase, full spectrum DFM-aware design will remain a high value, strategic capability that fosters an increased amount of certainty to the electronic product realization process.

An indication of where PCB design, fabrication, and assembly are moving can be gleaned from where IC design has already been. While the two domains differ in their target implementation, their respective design processes share many common elements. Moving forward, the opportunity exists to provide electronics OEMs with the ability to "connect" with a global, data-enabled ecosystem of fabrication and assembly service providers for immediate capabilities-awareness and rules-driven design guidance and validation. This paradigm also supports optimization across OEM-defined parameters for such factors as turnaround time, cost, and availability, which will enable OEMs to "shop" their project out across the ECM ecosystem with a click of the mouse for thoroughly informed, warp-speed decision-making fitted to the capabilities of ECMs. **PCB007**

Vince Mazur is product and persona marketing engineer at Altium.

DFM From the Fabricator's Point of View

Feature Interview by the I-Connect007 Editorial Team

What do you think of when you hear the term DFM? By its very definition, design for manufacturing tends to focus on what designers need to do to make sure that fabricators can manufacture their boards according to design intent.

But what about the flip side of this equation? What should the fabricator do to facilitate better DFM practices? The I-Connect007 Editorial Team posed this question to a trio of design and fabrication experts: DownStream Technologies co-founders Joe Clark and Rick Almeida, and Max Clark, business unit manager for Valor at Siemens EDA. We think you'll enjoy this wide-ranging conversation.

Andy Shaughnessy: We've run a lot of coverage of DFM, and it tends to be from the designer's point of view, so we wanted to get it from the other side. Because you deal with both sides of the equation, what would the fabricator like to see from the designers, as far as DFM?

We've heard some designers say that fabricators won't tell them their capabilities. They'll say, "Look on our website."

Joe Clark: Often the fabricators do keep their cards close to their chest.

Barry Matties: Why is that?

Joe Clark: Why do fabricators gladly accept Gerbers rather than intelligent data, which is going to make the handshake that much better? Max can certainly jump in here from his experience, but many times it's nothing more than a fear that if they push them to get the intelligent data, the customer will go somewhere else. But virtually every CAD tool today supports ODB or 2581, so obtaining these formats should not be a problem.

Max Clark: That's a good question. I suggest we divide this discussion into things like data exchange, and then maybe manufacturing capabilities exchange, because they're two separate topics. From a data exchange, you're


Max Clark

right. Part of the challenge there is acceptance. I work with a lot of the OEM sides wanting to use ODB++ and the challenges that we go through there is they must accept internally that it's what they want to do. It usually becomes a type of decision to say, "We're going to send this, and that's it." And the fabricator just learns to live with it. That's usually the way it seems to go.

But before they're willing to make that leap, they don't have confidence in themselves that the transfer will be successful, that the manufacturer can work with it. We end up going through what might be several weeks, or even several months, of back and forth, comparing designs. They want to try every type of design they have. If they have multiple EDA tools they want to test it on all the EDA tools because they want to commit to it all at once. Then we end up going back and forth with the fabricators to obtain their acceptance. While this is not DFM related it's still what hinders them from a DFM perspective.

Matties: My understanding is that there are some manufacturers offering price discounts if you're using IPC-2581.

Max Clark: Yes. That's been tried even with ODB++ in the past, using it as a carrot to get data faster. The transfer is smarter; I don't care whether you're using 2581 or ODB++ from that perspective. The exchange is smarter, faster, it gets in the system, and more comes in correctly the first time, so that's a huge advantage. I think the first hurdle people must get over when it comes to DFM acceleration is the acceptance of a new, better, or improved-upon way to transfer that data. The analysis that you perform, either on the design side or the fab side, is only as good as the data you're being presented with. From my experience, trying to reverse engineer that intelligence into the Gerber data is only so accurate, and it is time consuming.

Matties: Is this a generational issue? Will the young engineers gladly use IPC-2581 if we train them to that?

Max Clark: I don't think so. There's a mirror image of this in silicon manufacturing where the foundries at first were very inward looking and they didn't want to share a lot of information. I think it's just a matter of maturity within the industry. It needs to evolve. Possibly the fabricators must do more insistence. Fabricators say, "They don't want to lose any business." They're afraid the customers will go somewhere else. That fear has got to leave.

Rick Almeida: They've been using Gerber a long time, and with all its warts, it still works for the design side. These guys are getting older and older. It's just ingrained in them that when you're done you're going to produce Gerber and go. Unless there's some compelling reason to switch that process nobody really gets a couple months where there's no work to do and they can go in and try a different process for the sake of trying a different process.


Rick Almeida

Joe Clark: Right, and they're very risk-averse. They have a process that works. They've been taking thousands of databases in Gerber format for a long time, and they have perfected this process. The fabricators went reluctantly to ODB and while the benefits to both sides—the fabricator and the OEM—are now indisputable, ODB is "different," and the current process works, so why change? The Valor people should be in the EDA hall of fame with the whole idea of a neutral intelligent design format that we're now leveraging off and has resulted in the IPC-2581. It's a no-brainer. As a segue here, we can have the same conversation on the contract manufacturing side. Just think about getting Gerbers and a spreadsheet for the parts list and having to put that together to drive the assembly process.

Max Clark: Oh, it's actually worse, because there you have to plug it into equations and all the other challenges that go with it.

Joe Clark: Yes, and then there are ECOs. You've got to put these designs onto an assembly line which is very manual, and the design keeps changing. The CMs are very risk averse; they have a process that works, they're driven by maximizing capacity utilization, and it is generational in a way. It's going to take time, and what will rule the roost here is the market. It's going to take the big OEMs telling their fabricators and their contract manufacturers this is what we want to work with. It improves that handshake between the upstream processes, where the IP is created, and the downstream processes where we manufacture these things.

Max Clark: Right. You're trying to perfect the process to release these products as effectively and as efficiently, as well as error-free, as possible. Everything else is pointless. If I was a fabricator, and I'm going to oversimplify this, but if I could get a design—and I don't care what format it came in—and just get everything to handle my best process and then send it out to the factory floor, I'd be styling. We build all these complicated CAM applications with the intention to improve yield. That should be the tool. That should be the focus of the CAM applications. Instead, the fabricators and assembly people end up spending their time finding where their challenges are going to be.

Almeida: The average ages, the average experience, and the average number of years moves up. As you get to a certain point in life you don't want to make changes unnecessarily.

Joe Clark: When I go into a company to present one of our products, if I see a group of people who are my age, I get a little worried (laughs). If I see a younger group—like some of the young people in the IPC-2581 consortium—they're usually embracing new ideas, like this use of intelligent design formats in a way that is great to hear and see. It will happen, it will. We'd like to accelerate it for various reasons. Gerber will probably always be with us to some degree, but there is a transition happening. It'll just take time.


Joe Clark

Max Clark: There's also another challenge that I don't know how anyone can solve. We're all used to working with the large OEMs. If you take all those people and you add their number of EDA seats together, it's minuscule compared to the smaller guys. Recently, I saw that there are approximately five million copies of a smaller but popular EDA solution out there.

Joe Clark: All legal? (laughs).

Max Clark: Whether it's legal, as long as there's that volume out there, they're the customer base that everybody on this call doesn't usually have traction at.

Matties: In one of our recent interviews, somebody posited a question to Andy: Who actually owns the design? Because if you're moving the design downstream to let the fabricator do the heavy lifting, who owns it at the end?

Joe Clark: There's an analog to this that Rick and I discuss a lot. Back in the day when there were tools like Quad Design and Quantic Labs for signal integrity, such tools were so specialized and difficult to use that there was this "end-of-the-line verification" process where you sent your design when done, and someone would run this magic test using Quad and Quantic and provide the results. If there was a problem, you had to go back "upstream," address it and repeat; this resulted in lost time and all the risks that go along with this. But what you really want is to do the signal integrity analysis in line as you're doing the design, not as an afterthought. That's where a tool like HyperLynx came in and exploded in the market because of its ease of use and lower cost of ownership.

> What you really want is to do the signal integrity analysis in line as you're doing the design, not as an afterthought.

The same thing is happening here. You had these big, heavy tools that were best in class at that time. They were expensive, and the fabricators were the ones that ran them. But now, with the acceptance and the embrace of these intelligent data design formats, combined with the analysis tools being greatly improved, designers can run, for example, DFM analyses in line on their designs rather than wait until the end, or even wait until the fab runs the analysis and reports back. We no longer talk about just CAM in the design space, we now talk about PCB preparation or PCB post-processing—taking the design from the virtual space to the physical space more efficiently. The analyses required to accomplish this are being run earlier in the process and the successes companies are realizing that have adopted such tools and formats speak for themselves.

Dan Feinberg: You're saying that the fabricator and the designer communication could improve significantly?

Joe Clark: That's always the case, yes.

Feinberg: But there is some communication between the designers and the fabricators.

Max Clark: Not often. Frequently, the designers have no idea where their board is even going to be made.

Joe Clark: Max is right, but you've got to separate the market. A military OEM is limited in terms of where they can go to get their boards. They also have a very tight handshake with the few vendors that they've blessed. All those other companies that could go anywhere, that's the problem. I'll even throw out the economic argument that I believe fabricators (and CMs) grapple with and that we touched upon earlier. As a fabricator, I'll take anything you've got because I want my capacity to be utilized as close to 100% as possible. I think that's a part of it as well. It's not just the technology, it's also a fear. It's that fear that the customer can and will go somewhere else if one pushes back.

Feinberg: Here is a quick example. I was a supplier for what was, at that time, the largest circuit board fabricator in the world—Western Electric in Richmond, Virginia. They're no longer there now. They wanted something with their photoresist and we told them, "We can't do that. We can't give you that frequency response and we can't give you that color that you want." They were dying their own auto-

matic detection equipment. You can't do that because it's going to change the side wall. They said, "What do you mean it's going to change the side wall?" I told them, "It's when you get a little bit of a slant at the bottom of the side wall where it meets the copper." They said, "You mean you can actually do that?" "Yeah, we have to avoid it." "No, we've got a project where we have been wanting to do that for years. Why didn't you tell me you could do it?" The result was I ended up taking $50 million a year in business from DuPont after that. Communication.

Matties: I know we talk a lot about communication, but there are those two events that trigger a higher need for a higher level of communication. You keyed in on the big guys with their AVLs; it's that smaller group that just may be out price shopping. That's probably where they get into more troubles with the DFM and respins.

Joe Clark: I totally agree with that.

Max Clark: It's good you said that, because I just met with a fabricator, a friend of mine that has been with the industry a long time. That's one of the biggest arguments he has with his sales staff. Designers come to them with the design that they want to build, they take the contract, he looks at it and says, "You know how many of these we're going to have to build at our facility in order to get the quantity that you want?" They say, "It's good business. We couldn't leave it behind." "Yeah, but we could have maybe taken another job, or two, or three because I have a fixed capability. I have a fixed volume that I can make." I mean, the one board he took was so bad that he's going to have to make 100 to possibly get four or five that would work. That's ridiculous.

Almeida: Yes. Somebody's got to pay for it. The fabricator may be paying for it, but if he doesn't get that back from his customer, he's not going to be in business too long.

Matties: Well, they're paying for it in lost opportunity. It's not just the hard dollars, it's all this stress that you're putting on your team, and all the lost opportunity. How do you really measure that?

Not to turn this into a sales pitch for your tool, but what's the traction that you're getting with the encrypted capability data, making that available?

Max Clark: Actually, it's getting pretty good. A lot of our OEMs are insisting that their fabricators go about doing this. Obviously, that's because they want to see it upstream. They want to be able to see the result of that upstream. You're right, not to pitch my own product, but that's the approach that we decided we must take because the fabricators in general are still hesitant.

Matties: Now, in terms of capabilities, as you're putting this tool together, are you seeing that there's what you might call a standard set of capabilities that need to be published, or is it unique to every fabricator?

Max Clark: That's a good question. When the fabricator puts their stuff up there it's even kept from me. I don't even know. The stuff is encrypted. We didn't look at it to the degree to start doing that kind of comparison. Obviously, it's probably possible, but everybody's facility is a little bit different, and they all have their own way of doing things. So I can't tell you if I notice a similarity. Say you had three manufacturers that were your options. In theory, it's possible to run an analysis once and look across all three to see who has the most likely capabilities to build this with the least number of issues. We have customers that say, "Even with this kind of knowledge I might be able to tweak a few things in the design and move it from our high-end fabricator into our mid-range fabricator. I reroute three traces and bingo, I go from $1 a board to $0.80 a board, just like that."

Matties: Happy calls this the cost drivers that the designer needs to be aware of. Happy, would you talk a little bit about this?

Happy Holden: There's a set of design rules that are considered a commodity in that they're built into the process and the chemistry such that you can price boards based on the number of layers and the square inches. But when you get to the limit of those commodities, there starts to be a cost slope, like if the diameter of a drilled hole goes under 10 or 12 mils, then we've got to get a drill bit, we've got to not stack as high, etc. Now there's a slope that, depending on how many of these are in your design, we add a cost to the commodity price. If you go under 75 micron there's an extra cost because of a yield loss. The horizontal commodity hits a slope, then the slope ends with our next capability. Beyond this we can't accept this design at all. But designers are not specifically aware of the cost drivers, and the slope of the cost drivers. The poor designers just have to guess or do the best they can.

Max Clark: Too late now.

Holden: Designers need information rapidly at particular points in design. If it's not there they do the best they can and they move forward because they can't stop and run around waiting for a question to be answered. Schedules any more don't allow that. It's not just communication, but we don't have tools and visibility of assembly, fabrication, test, things like that, made available to designers in the right form at the right time.

Max Clark: That's an interesting concept. In a sense, you're saying what the fabricators want to do in terms of shifting their process capabilities is to not just shift the process capabilities, but also provide a relative cost. It doesn't have to be a finite cost, but a relative cost, if that particular item is violated. Let's say you have a particular via size, and if you go below this via size you would like to have the designer knocked on his head, saying, "You can do this, but you need to know when everything is said and done this is going to add an additional cost."

Holden: At HP, we created a relative cost index (RCI). We created a hypothetical currency because we found that nobody wanted to give

X things in cost in dollars. By having an artificial currency as the relative cost index, it was most useful in comparing choice A with choice B with choice C. It wasn't useful for pricing a board, but it was useful in design decisions like, "What route on this important milestone here should I travel down?"

Max Clark: Right. If I use a via that's too small and I've spent three days routing this board, then you come back and tell me, "It's going to cost you more because you did." I'm going to say, "That's too bad, because I'm not going to go back and reroute this whole board."

Holden: Like you mentioned, you have some goals to begin with. The goal of this board is to be fabricated by a tier two, not a tier one. We have some excellent tier twos that are always good on quality, but their prices are great. So I want to stay away from the tier ones that are prima donnas; they can build anything, but I want this. You don't have to put a particular name when you encode the data into the cloud database that drives advice and recommendations.

Joe Clark: We're always pushing the envelope, especially in the mil-aero space. But I can't tell you how many customers we deal with across the spectrum worldwide that don't even do blind and buried vias. And, in the PCB world, what's really changed? What's the biggest change in the last 20 or 30 years?

Almeida: The last big change in PCB was probably surface mount.

Max Clark: Now you have the embedded components.

Almeida: But those are the outliers. I mean, if you look at the main market, it's two-layer, four-layer, six-layer designs. It's exactly what you said earlier, Happy, the commodity PCB. That's what's being built most of the time.

Matties: I think we're going to start seeing some rapid change, though, with M-SAP and these others, especially with inflation. If we start seeing the inflation hit hard, the designers are going to have to get smarter to reduce cost. I think we're going to see some innovation, right?

Max Clark: It's going to force it. I do see some changes occurring even though we're still in our infancy with the progress that we're wanting to make. One of our competitors started this idea of shifting the manufacturing. They had something in place as well. Everybody is going in this direction. I think it will continue to shift in that direction where more and more of the analysis is done less based upon what the designer put in for the design tool to design to, but more about what the manufacturer is capable of and looking for that intersection. The designer will never design a board just because a fabricator can make it. They're originally designing the board because the technology needs it. They build it because the technology needs it. Now they look to see if their manufacturers can manufacture it. Today, they're doing it mainly after the fact, when it's too late. What they need to do is shift that over so that somebody comes and says, "We need these criteria." And they start working on it, but if you want to make it at this board shop they can't do it; I can tell you that right now, so start looking for somebody else. Who else should we look for?

Joe Clark: Yes, but I really like that idea. It never occurred to me. I really like the idea of the encrypted fabricated data. I can bring that upstream and it's neutral, meaning anybody can read it; it's just encrypted. If the fabricators are nervous about releasing their family jewels, if it can be encrypted in a way that we can read it upstream regardless of whether it's your tool, my tool, anybody's tool, that's the information exchange that supports exactly what Happy said. You could do your analysis up front as you're designing the board. You might

be changing the fabricator that you're going to target this design to because those guys can't do it and he can. It's an intriguing idea.

Holden: That's why I think that AI and some of these chips and things like that will provide the software environment so that once the fabricator puts in his encryption key he can edit, update the proprietary information, but everybody can use it not knowing what it is, but how the software interacts and gets answers to its questions. You're facilitating the communication. Especially if it's part of the EDA tool and you're laying out, routing, and placing parts and things like that, that's when you need answers to questions. You may not be able to pick up the telephone to call. Now, I go back to a vertically integrated company where if you had a question like that you just picked it up, you could call down...

Joe Clark: You could just walk down the hall.

Holden: ... to the next building or walk it down the hall. Now it's on the other side of the world and you don't have that luxury. But you need some way to replace that, because of the schedule, you're not going to stop and wait to get the answer. You're going to punt. You're going to pick the best guess that's possible, the way you did it the last time and ask your boss, "What should I do here, boss?" And keep on trekking whether it's right or wrong. Most of the time it's probably not the best guess, but it's the only process in town. We need a better way to facilitate what's going to become more and more complicated, unfortunately, not less complicated. Yeah, because the guys designing single-sided boards don't have those. The bad thing about our industry is we're still making single-sided boards because they're the lowest cost and the technology may be in the semiconductor that's placed on a single-sided board. So, it may replace this 14-layer multilayer and now it's a single-sided board with this SOC. In fact, I've traced the generations of our RISC computers, our big ones from a 14" x 16" 14-layer board to a 4" x 4" MCM, to a 2" x 2" 2+2+2 HDI SLP.

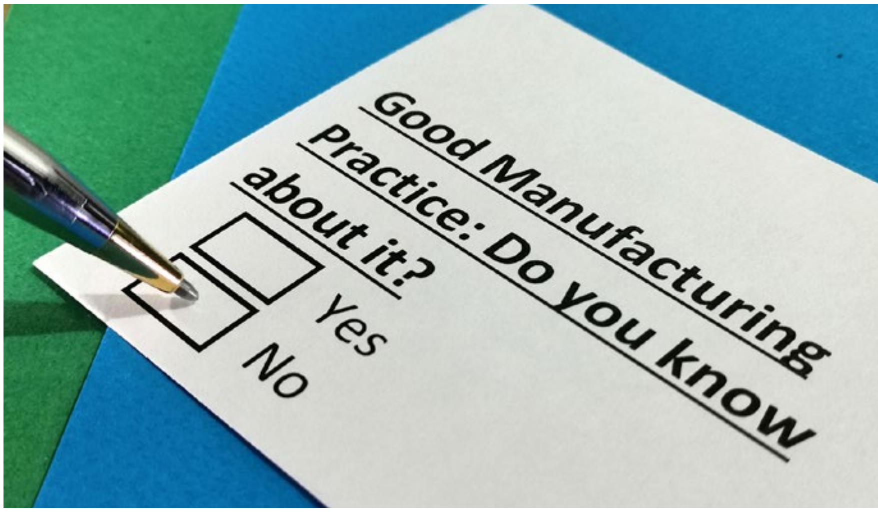
Joe Clark: But isn't that what we're going to be dealing with? I mean, the differentiation, the technology is part of the component. The PCBs are just becoming a carrying case.

Max Clark: They always were.

Joe Clark: Why would they get more complicated?

Max Clark: Because you put more on them.

Almeida: Yes, but that's always been the case. We've always put more on the PCBs.



Nolan Johnson: Now, making sure that your substrate and how it performs is a part of the analysis and the selection process was a point earlier on in this conversation. I think I would put out there that, as an industry, we're at a point in circuit board design where it's time to start using integrated circuit methodologies that were developed 25 or 30 years ago.

Shaughnessy: To wrap up, what do you think designers and fabricators seem to misunderstand about each other most consistently? They seem to talk past each other; they can't even agree on a standard set of terms.

Joe Clark: Let me start that conversation. Here's what I have learned in my years, and I go back to vertical companies as well. I started my career at GenRAD and we fabricated our own boards, assembled them, and so on. We dumbed ourselves down in the '80s when we outsourced manufacturing. What I find today is that most young engineers have no idea what happens to their designs when they go out for fabrication. They just know that this green thing comes back. I think that's changing, but the problem is more on the design side than it is on the fabrication and contract manufacturing side. Often, those upstream don't know what the best practices are and what the challenges are that people deal with downstream. If they knew, and knew that alternatives existed, they would not just send "unintelligent" Gerbers. I'll stop there.

Shaughnessy: When they were captives, designers all knew more about manufacturing because it was down the hall.

Joe Clark: I think we need to re-learn manufacturing upstream. That's my umbrella view on the world, and I see that changing.

Max Clark: Yes, I think the evolution is starting. It's going to take a while. This industry doesn't move fast, but it is going to get there. Anything we can do to push it along we should do. But I think it's starting. That's my last bit.

Joe Clark: One thing I would say here is that in many ways the fabricators are—not to sound a little harsh—their own worst enemy because they just take that data and they fat-finger it and cleanse it and spend a lot more time than they need to manufacture the boards.

Max Clark: You're correct.

Shaughnessy: This has been really great.

Matties: Great conversation. Thank you all so much for doing this.

Almeida: Thank you. It's always a pleasure to speak with you. **PCB007**

Check out Downstream Technologies' book, *The Printed Circuit Designer's Guide to... Documentation.*

Leadership 101: The Laws of E.F. Hutton and Connection

The Right Approach

by **Steve Williams,** THE RIGHT APPROACH CONSULTING

Introduction

Good leadership always makes a difference; unfortunately, so does bad leadership. This leadership truth continues as we will be talking about the 10th of the 21 Irrefutable Laws of Leadership.

When E.F. Hutton Speaks, People Listen

Anyone within a couple of decades of my age remember this tagline from the ubiquitous commercials of the '70s and '80s for the E.F. Hutton stock brokerage. Fifty years later it still sticks with me, and John Maxwell has leveraged it into one of the 21 Irrefutable Laws of Leadership.

"When the real leader speaks, people listen."
— John C. Maxwell

I was with a client recently where this law was on full display. When I am speaking or teaching, I have the unique perspective of being able to watch the audience and observe behaviors and reactions to what I am saying. I was recently facilitating an ISO certification kick-off meeting with a group of a shop supervisors and department leads at a new client's facility.

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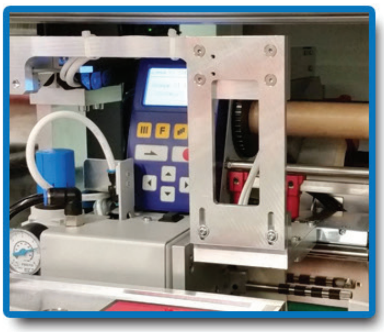

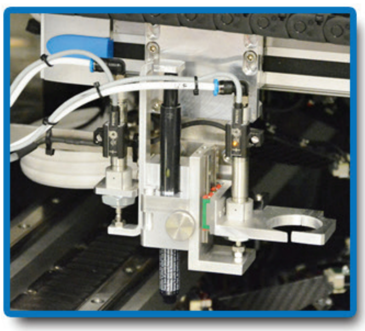

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We had about 15 people in the room, including the operations manager. I was feeling pretty good about my communication skills as I saw a sea of nodding heads while I spoke. One woman, "Sally," nodded enthusiastically after something brilliant I had obviously just said, but then I noticed a very slight delay before others began to also nod. I began to feel a bit deflated as I realized that many in the room were taking their cues from Sally and not necessarily from my charismatic dialog. When I asked the team if they were ready for the level of commitment, support, and work the project required, most of them looked first to Sally, and not the operations manager, before verbally agreeing.

It was clear that Sally was the "real leader" on the shop floor, the one everyone looked to for help and guidance. While this is not the norm, nor should it be, there are informal leaders in every company. *Positional leaders* have a title but not always a following while *real leaders* have a following but not always a title. *Positional leaders* influence positionally while *real leaders* influence everyone. How do you become a real leader? Real leaders become real leaders because of:

- Character
- Relationships
- Knowledge
- Intuition
- Experience
- Past successes
- Ability

Remember the saying, "The title does not make the leader; the leader makes the title."

Everyone Communicates, Few Connect

This is such an important concept that John Maxwell wrote an entire book on it. The ability to connect with people is an essential component of leadership and a "must have" for great leaders.

"You can't move people to action unless you first move them with emotion. The heart comes before the head."
—John C. Maxwell

Connecting with people is not easy. We need to touch a heart before we ask for a hand, and the first heart we must touch is our own. In other words, we cannot lead others to places we've never been to ourselves. What does it mean to connect with ourselves? It means understanding the answers to the following questions:

- Do I ask, "How can I help you?"
- What is my greatest asset?
- Am I applying my strengths?
- How can I use my strengths to coach others?
- How well do I relate and communicate with others?
- Do I like me? Am I likeable?
- What can I do to project my sincerity and add value to others?

Authenticity is a trait people look for in a leader. Do you ask questions about others' lives? Do you understand what motivates them? What is important to them? A leader fails if he or she does not know their followers. If you answered "no" to any of these questions, you might want to actively work on improving your connection skills in the following ways:

- Connect with yourself
- Be open and sincere
- Live your message
- Know your people
- Communicate on their level
- Commit to helping others
- Believe in others
- Offer direction and hope

Developing relationships with the real leaders in an organization and honing your ability to form meaningful connections with others will become vital tools in your leadership toolbox. Develop and use these tools early in your relationships with others and you will quickly see the benefits. PCB007

Steve Williams is president of The Right Approach Consulting. He is also an independent certified coach, trainer, and speaker with the John Maxwell team. To read past columns or contact Williams, click here.

Wearable Brain-Machine Interface Turns Intentions Into Actions

A new wearable brain-machine interface (BMI) system could improve the quality of life for people with motor dysfunction or paralysis, even those struggling with locked-in syndrome—when a person is fully conscious but unable to move or communicate.

A multi-institutional, international team of researchers led by the lab of Woon-Hong Yeo at the Georgia Institute of Technology combined wireless soft scalp electronics and virtual reality in a BMI system that allows the user to imagine an action and wirelessly control a wheelchair or robotic arm.

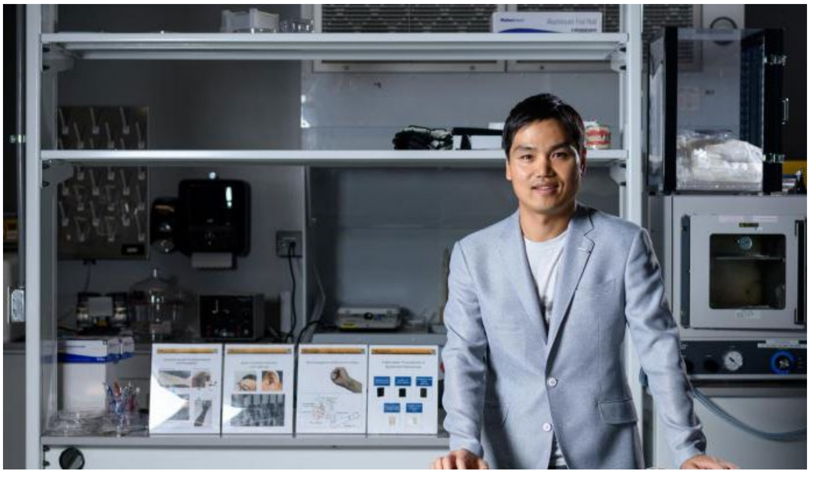
BMI systems are a rehabilitation technology that analyzes a person's brain signals and translates that neural activity into commands, turning intentions into actions. The most common non-invasive method for acquiring those signals is ElectroEncephaloGraphy, EEG, which typically requires a cumbersome electrode skull cap and a tangled web of wires.

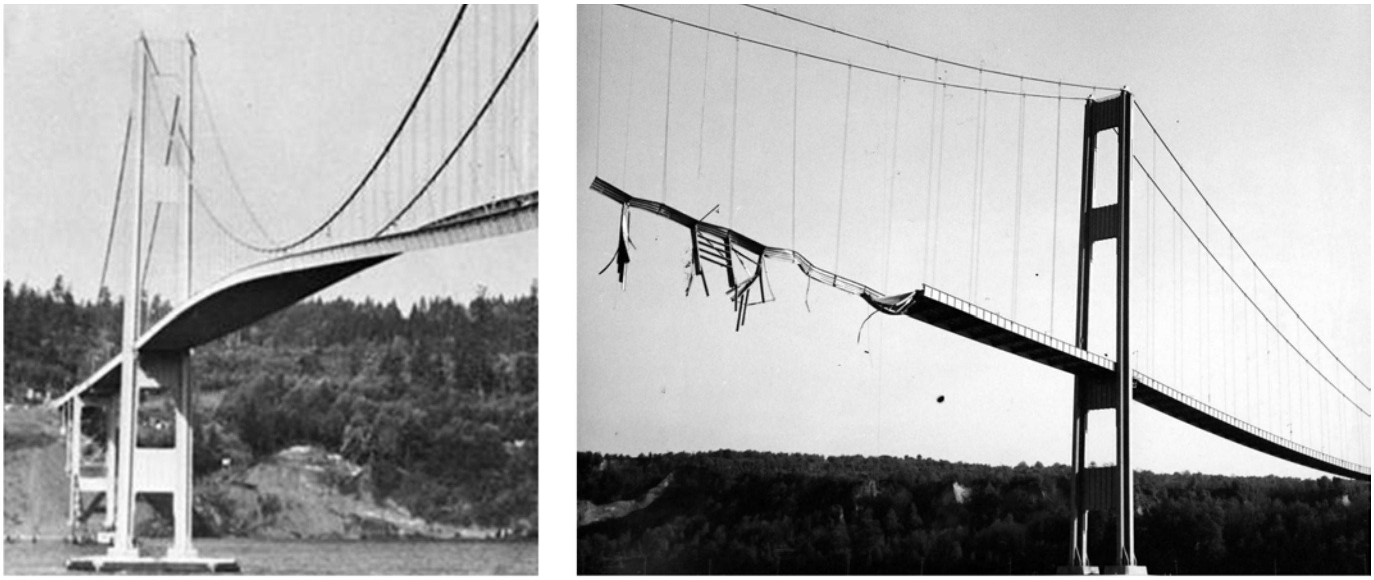
These devices generally rely heavily on gels and pastes to help maintain skin contact, require extensive set-up times, are generally inconvenient and uncomfortable to use. The devices also often suffer from poor signal acquisition due to material degradation or motion artifacts—the ancillary "noise" which may be caused by something like teeth grinding or eye blinking. This noise shows up in brain-data and must be filtered out.

The portable EEG system Yeo designed, integrating imperceptible microneedle electrodes with soft wireless circuits, offers improved signal acquisition. Accurately measuring those brain signals is critical to determining what actions a user wants to perform, so the team integrated a powerful machine learning algorithm and virtual reality component to address that challenge.

The new system was tested with four human subjects, but hasn't been studied with disabled individuals yet.

(Source: Georgia Tech)





Tacoma Narrows Bridge during wind storm, known locally as "Galloping Gertie." Photo: Washington State Department of Transportation Special Collections Nov. 1940

Flex DFM: When All Things Must Be Considered

Feature Article by Chris Clark
FLEXIBLE CIRCUIT TECHNOLOGIES

Engineers can't possibly think of everything, every time.

One of the worst examples of an engineering failure is the Tacoma Narrows Bridge in Washington state that collapsed in 1940. The bridge was not engineered to withstand the environmental factors placed upon it by wind and weather.

I realize comparing a flex circuit to the Tacoma Narrows Bridge is a stretch (no pun intended), but the point is that no one wants to see a project fail after they've poured their heart and soul into it.

One of the best ways to avoid flex failures is by communicating with your flex fabricator early and often. Here are a couple key reasons why involving your flex and rigid-flex supplier early in the design of your product will help you save time and money—and produce a more reliable flex circuit.

Product Cost

Many things can impact the final cost of the product. Choosing suppliers with significant experience and knowledge that they are willing to share will, without a doubt, help control your costs in the long run. These industry experts will pose the dreaded "Yeah, but" questions that can keep your project on track. For example, "We certainly can build your circuit exactly as you have designed it. However, the small tail you have extending from the main body of your circuit is costing you lots of money."

There are some instances in which shrinking something by only a quarter of an inch can greatly impact panel density, thereby lowering your production costs. Without knowledge of your supplier's processing needs, you have no way of knowing if the dimensions of your part are an efficient use of the material. Many things factor into this including panel size, tooling holes, fiducials, and coupon requirements. In some instances, having your designs reviewed

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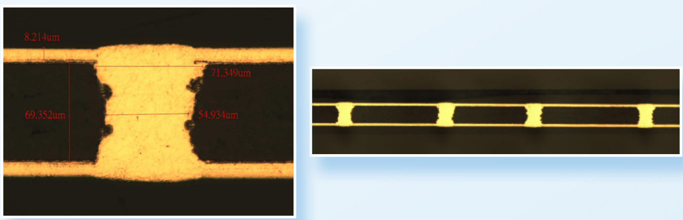

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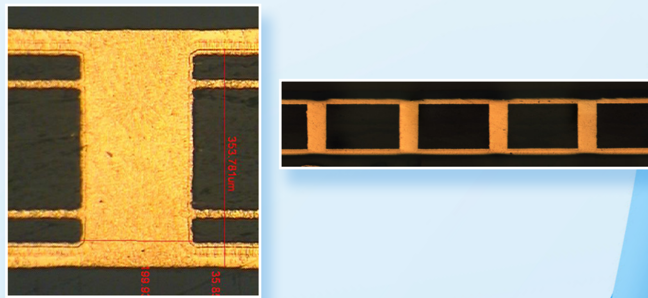
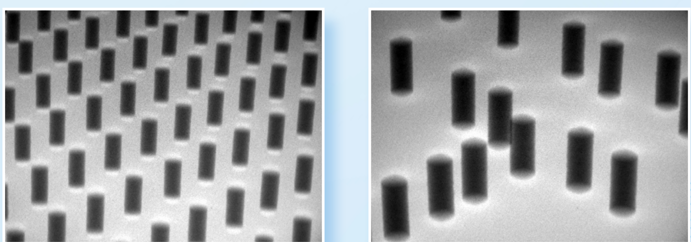


VOID-FREE COPPER BY X-RAY



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by an engineer with both circuit design and manufacturing experience may save you more than 25% in long term costs.

Another example is in yields. While it may be possible to build the circuit as you have it designed, a supplier with strong design for manufacturing (DFM) experience should be able to point out minor design changes that will increase yields measurably. For example, while a circuit may be able to be etched out of one-ounce foil, it may come at a reduced yield when compared to half-ounce foil. An experienced engineer should be able and willing to suggest materials based on the electrical and mechanical needs of your application. They should balance these requirements against manufacturability, allowing them to recommend materials that will be the most cost effective.

An experienced engineer should be able and willing to suggest materials based on the electrical and mechanical needs of your application.

Time to Market

Let's face it, time is money. Say you are working for a medical device company on a new project. You are well-versed in circuit design, so you decide not to engage with a circuit supplier offering DFM analysis. Instead, you think it will save time to work directly with a quick-turn house. After several weeks you receive the product and install it in your device. The product meets your needs both mechanically and electrically. You think, "Great, this is working exactly as planned." Now it's time for another round of parts so you go back to the same quick-turn shop and order a couple dozen more. The product is delivered, and it performs wonderfully. Teams are working in parallel on the qualification process. What the supplier didn't tell you is that your circuit design and your drawing are in conflict. To achieve the impedance you are requiring, they use different materials than what you had specified. The issue wasn't uncovered until a first article was performed on the low-rate production parts. Now the drawing and design must go through an ECO process that will take weeks. On top of that, the qualification process must start over, and you need to order more parts to perform FAI. Now the program has your team under the magnifying glass. All of this could have been prevented by taking a little bit of upfront time and working with a supplier that is willing to perform due diligence at the design review stage.

Drawing Review

Imagine you are a consumer electronics start-up. You work on a design and specify materials that you are familiar with. This is based on a small volume application you worked on in a previous life. After months of development, you get to a point where you are ready for the big time. You send out for volume quantity quotes only to find out that two of the three companies you have solicited bids from come back with a no-bid. The no-bid is due to limited material availability. The base material you have specified on your drawing is in short supply and only available through a certain distributor. The distributor has a sole-source agreement with the company you prototyped with.

You are now left with the decision of sticking with that existing supplier at a higher production cost or redesigning your product so you can save money in the long run. You might think that you must be very specific when choosing materials that you call out on your drawing. This simply isn't the case. Material can be specified to meet the stringent requirements of IPC, allowing your supplier to choose the materials that are the most cost effective and available. The flow down of a change notification process will prevent them from changing things on you midstream. A reputable flex and rigid-flex supplier should point out these types of things to you up front.

Latent Failures

This is the biggest one of them all. Think about the Tacoma Narrows Bridge. What if you were an automotive EMS company working on circuitry used in the next generation of airbags. To save costs, you partner with a supplier that doesn't take the time to ask about end use, including the circuit forming and environmental conditions. The installation of the circuit into the housing is a manual process and there is an aggressive form that needs to take place. Depending on the day of the week and which individual is doing the forming, there is a significant stress placed on a couple of conductors as they join up with a row of connector pads. Over time, the introduction of thermal stresses, as well as vibration, contribute to cause some of these conductors to crack. The end-result is a failure to deploy or inadvertent deployment. Even though there is a very low percentage of field failures, this can prompt a massive recall. All this could have been prevented if the supplier had stopped to ask for 3D modeling so the bend radius could be reviewed. An evaluation based on the types and thicknesses of materials could have been performed. With this information in hand, the supplier could have notified the engineering team on the procurement side and design changes could have been made up front.

These are only a few examples of things that can go wrong. My overarching message is to find a trusted supplier that will help "Tacoma-proof" your designs. Flex and rigid-flex fabricators know their processes and capabilities. It's in their best interest to help you engineer a product that is reliable and cost effective. **PCB007**

Chris Clark is a senior applications engineer for Flexible Circuit Technologies (FCT) with over 30 years of expertise in design and fabrication of flex and rigid-flex circuits.

Researchers Uncover Unique Properties of a Promising New Superconductor

Material could be used in future quantum computing applications

An international team of physicists led by the University of Minnesota has discovered that a unique superconducting metal is more resilient when used as a very thin layer. The research is the first step toward a larger goal of understanding unconventional superconducting states in materials, which could possibly be used in quantum computing in the future.

Niobium diselenide (NbSe2) is a superconducting metal, meaning that it can conduct electricity, or transport electrons from one atom to another, with no resistance. It is not uncommon for materials to behave differently when they are at a very small size, but NbSe2 has potentially beneficial properties. The researchers found that the material in 2D form (a very thin substrate only a few atomic layers thick) is a more resilient superconductor because it has a two-fold symmetry, which is very different from thicker samples of the same material.

The researchers attributed the newly-discovered two-fold rotational symmetry of the superconducting state in NbSe2 to the mixing between two closely competing types of superconductivity, namely the conventional s-wave type—typical of bulk NbSe2—and an unconventional d- or p-type mechanism that emerges in few-layer NbSe2. The two types of superconductivity have very similar energies in this system. Because of this, they interact and compete with each other.

(Source: University of Minnesota)

Reasons and Solutions to PCB Lead Times and Price Increases

Article by Stanley L. Bentley, P.E.
ICAPE GROUP

If there is anyone left in the electronics community that has not been impacted by the chaos in PCB pricing and lead times, they must live in an alternate universe. I have been in the industry for 50 years. In that time, there have been many periods of shortages and price variations. None of those periods compares to the situation today. Seldom does a day pass without someone requesting a conference call to discuss the price increase. Everyone asks the same question: "What is the root cause?"

I have spent quite a bit of time the past few months researching PCB costing, and I have concluded there is no single root cause. I wish to add a disclaimer: During my investigation, I did not solicit the opinion of anyone with a title of politician, economist, or professor. Sorry, folks. I went directly to the street, soliciting the opinions of people who actually live in this universe.

The first thing I wish to do is dispel the conspiracy theory that has been making the rounds. That theory is that the root cause of cost increases was that a certain Asian government believed that a new U.S. administration would remove the tariffs on electronics. Asia saw no reason for all the prices to fall since the United States had (seemingly) absorbed the tariff increases. Therefore, Asia wanted to create a general price increase that benefited all parts of the local supply chain by starting with the raw material. Whew! It is easy to see why this narrative has persevered. The reality is that the costing surge is a complex mix of economic events and not a single Machiavellian scheme. This conspiracy theory is the stuff of Tom Clancy novels, but not applicable to the present situation. (Sorry Tom.)

A small digression is needed to examine the costing structure of a PCB. There are many different models circulating around and every PCB fabricator has their own version from which they derive their pricing. I would pro-

pose to distill all these down to a simple chart that is a composite of the most accurate of the models.

I summarize the PCB costing into these three categories:

- Raw materials, 47%
- Technology processing, 43%
- Yield, 10%

Of these three categories, the laminate (FR-4 for those who insist on a generic label) is approximately 36%. Therefore, laminate is the number one cost driver in a PCB.

The category of raw materials (47%) consists of many different elements, including laminate, copper, films, coatings, etc. Each of these elements are part of a different commodity chain. The laminate is the most unusual because it crosses two commodities: metal and oil. Therefore, it has a complex cost model. An increase in copper demand impacts laminate. A change in global costing for oil impacts laminate. The chart in Figure 1 shows the relative breakdown of the major costs.

A useful problem-resolution tool when dealing with a complex problem is to answer the "Five Whys." For those not familiar with the process, it is identical to what your mother employed when you were "bad" but you refused to admit to the crime. You simply take each answer to the last question, and ask, "why?" If you do this enough times (usually five), you arrive at a simple root cause. I used this process with multiple fabricators and the internal ICAPE team in Asia. The answers are different, but intriguing.

From the Five Whys analysis, I received six different top-level answers to the following question: "Why did the PCB increase in cost?"

- Increase in copper pricing
- Increase in other materials such as resin and tin
- Increase in laminate cost
- Increase in factory loading
- Top-level increase in pricing due to margin loss by the fabrication shops
- U.S. inflation rate

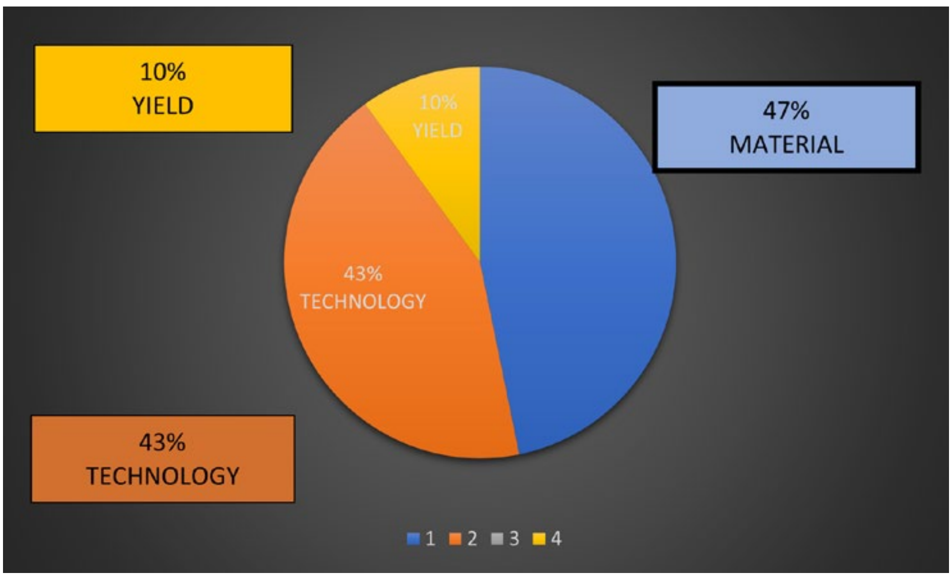


Figure 1: Simplified PCB cost model.

I would suggest that an illustrative exercise would be to take each of these major answers and perform a Five Whys analysis. Just as an example, I show one of the Five Whys responses I received (copied exactly as received) in Figure 2.

I found this Five Whys response fascinating as I heard a version of this same information from every source I researched. There is a perception in

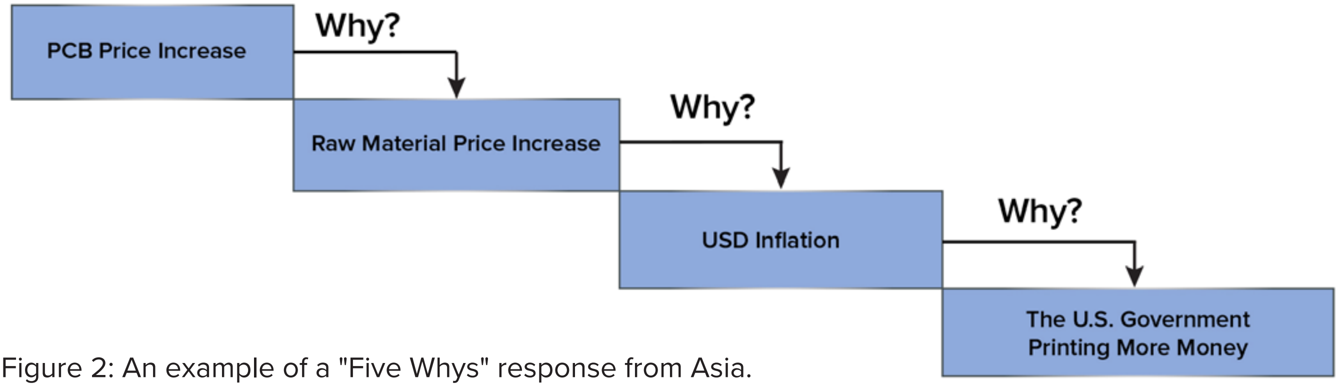


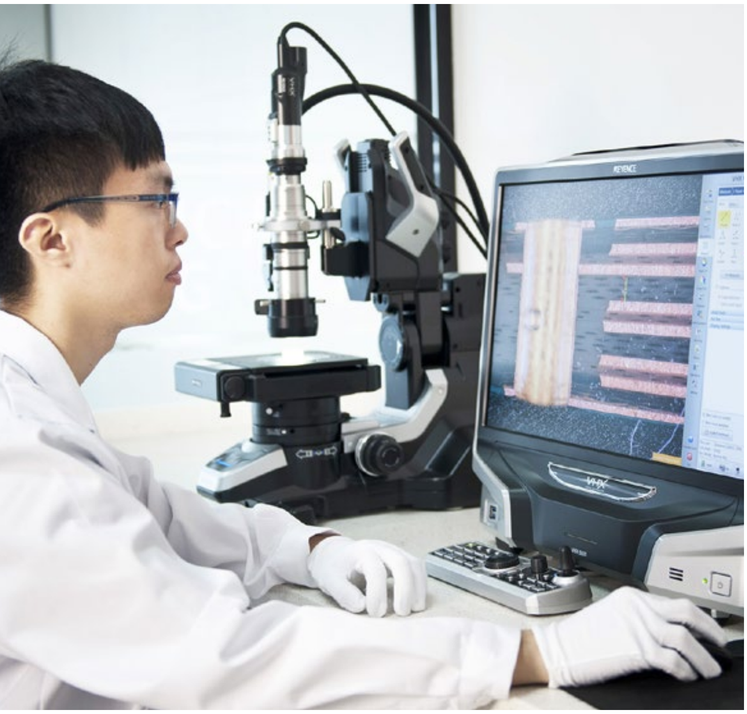
Figure 2: An example of a "Five Whys" response from Asia.

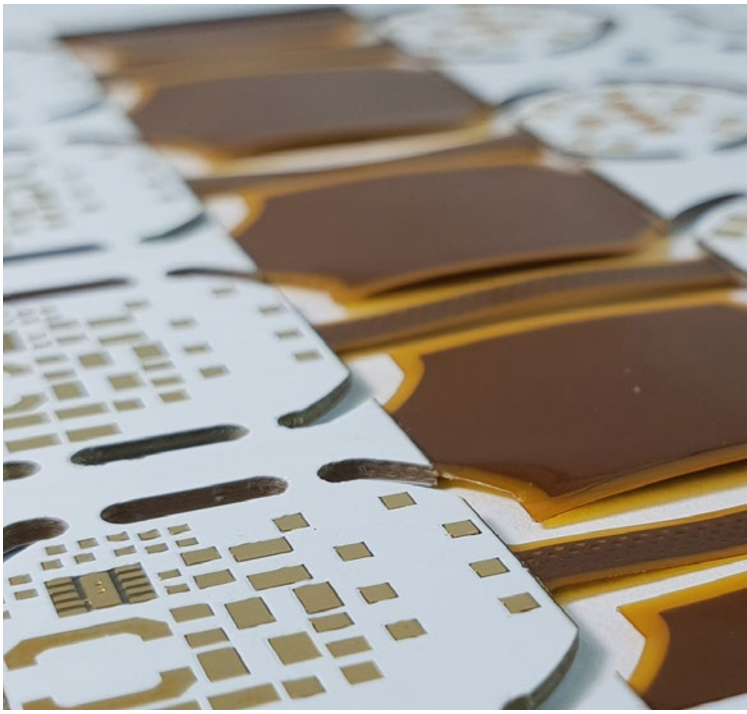
other countries that the rising U.S. debt is a major factor in raw material pricing. I will leave this one to the professors and economists to analyze.

Using statistics from the first six months of 2021, we have several intriguing facts:

- Overall demand for PCBs is up approximately 30% over 2020
- The average loading of the major fabricators exceeds 90%
- Average cost of the raw material to the fabricators is up 38%
- The U.S. dollar has decreased against the Yuan by approximately 8% (Note, this is after a de-valuation by China to offset the U.S. inflation rate)
- The public companies in Asia are under pressure to offset their margin losses and protect the share price. Margin loss resulted in a net drop in share price in 2021 from 10% to 38% for nine of the 10 public PCB shops in China polled
- The average cost to the fabricator of a multi-layer PCB has increased by approximately 40% over 2020

The critical fact to note is that the average retail price of a PCB (without any tariff) has not increased at the same rate as the cost to the fabricator shops. The average increase at the retail level (OEM) is closer to 25–30%. It is expected that the pressure on the public shops to improve their margin and share price





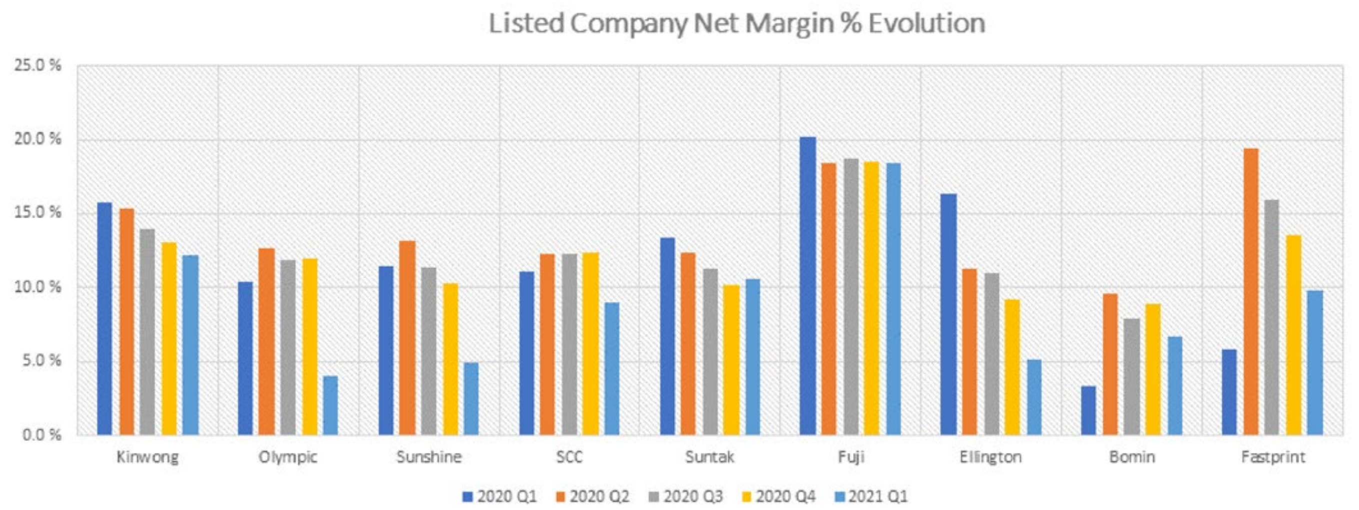


Figure 3: The net margin percentage evolution gathered from nine public Chinese PCB factories.

will continue to increase prices at the retail (OEM) level.

Figure 3 indicates a major concern because it means that even though it appears the shop efficiencies (capacity) are increasing and the raw material prices seem to be stabilizing (and in some instances dropping), there will be continued pressure on retail prices to offset the margin loss.

What Can the End User Do About This Situation?

Start with the assumption that none of us can impact the following:

- Raw material prices
- Factory efficiency
- U.S. inflation
- Margin pressure on public companies

My suggestion is to look at the factors that are in the control of the OEM:

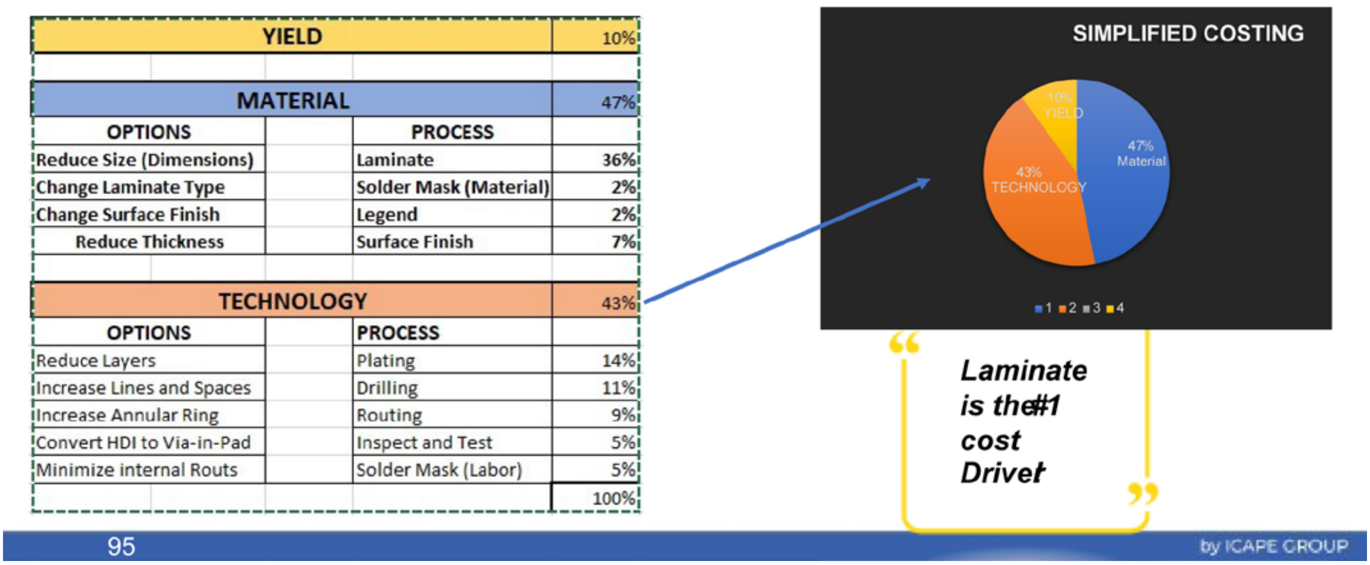
- Technology of the PCB (layer count, lines and spaces, via structure)
- Size of the PCB
- Choice of laminate (for example, what is the necessary T_g?)
- Surface finish (is ENIG always the best choice)

In many cases, none of these cost factors can be utilized (see Figure 4). The reasons vary, but if design factors cannot be considered what is left?

The remaining options that the OEM can consider are as follows:

- Increase the minimum order size
  - PCB costing decreases with volume
- Consider a VMI (vendor managed inventory) program
  - Six months is a reasonable stocking period
- Consolidate freight
  - This may be difficult without the assistance of a logistics supplier or supply chain manager
- The last item in the toolbox is often the first choice in the U.S.
  - Beat the supplier up by threatening to move the business

I would caution that while this option is very popular in business schools, the PCB is not a commodity, and it does not move between suppliers without collateral costs. If changing vendors is under consideration, I have a series



YIELD			10%
MATERIAL			47%
OPTIONS		PROCESS	
Reduce Size (Dimensions)		Laminate	36%
Change Laminate Type		Solder Mask (Material)	2%
Change Surface Finish		Legend	2%
Reduce Thickness		Surface Finish	7%
TECHNOLOGY			43%
OPTIONS		PROCESS	
Reduce Layers		Plating	14%
Increase Lines and Spaces		Drilling	11%
Increase Annular Ring		Routing	9%
Convert HDI to Via-in-Pad		Inspect and Test	5%
Minimize internal Routs		Solder Mask (Labor)	5%
			100%

Figure 4: A summary of the overall situation.

of articles about how to minimize the risk (and costs) by properly selecting a new PCB supplier. This process is too lengthy for this brief article, but suffice it to say it has three major steps:

1. Choose a supply chain partner that could recommend qualified fabricators for the volume and technology levels you require. In this process, they would ensure that the supplier had the requisite quality certifications.
2. Have the recommended supplier (or suppliers) supply samples of "running" PCB part numbers.
3. Have the sample PCBs analyzed by a qualified laboratory to the relevant IPC specifications and to your internal requirements. **PCB007**

Stanley Bentley is the technical director for ICAPE Group in the Americas. He is a 50-year veteran of the electronics industry. He is a registered professional engineer and the former owner and chief technical officer for Diversified Systems, an electronics design firm, PCB fabricator, and assembler.

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Electronics Industry News and Market Highlights

Russian Government Announces Competitive Selection of AI Research Centers ▶

The Russian government will allocate 5.4 billion rubles for establishing and supporting AI research centers in Russia. The competitive selection of candidate centers announced by Deputy Prime Minister Dmitry Chernyshenko started on July 15.

European Semiconductor Sales Up 31.2% YoY ▶

European semiconductor sales in May 2021 reached US$3.777 billion, an increase of 31.2% compared to the May 2020 sales, the European Semiconductor Industry Association (ESIA) reported based on World Semiconductor Trade Statistics (WSTS) data.

Qi 1.3 Wireless Charging Reference Design to Accelerate Automotive, Consumer Qi Transmitter ▶

The Wireless Power Consortium (WPC) has recently released the Qi 1.3 specification that requires authentication for improved safety when transmitting up to 15W of power between a transmitter and a receiver.

Semiconductor Equipment Forecast to Post Industry High of $100 Billion in 2022 ▶

Global sales of semiconductor manufacturing equipment by original equipment manufacturers are forecast to surpass $100 billion next year, a new high, after jumping 34% to $95.3 billion in 2021 compared to $71.1 billion in 2020, SEMI announced.

Survey: Companies Lagging the Industry in Digital Transformation ▶

46.6% of survey respondents believed that their own companies fell behind the industry average when it comes to utilizing digital tools as part of business processes, according to a survey conducted by AIBP and Oracle from March to April.

Researchers Develop Fabric-friendly Sensors ▶

Sensors are part of modern-day technology. From contactless payment to key fobs, credit card chips to smart devices, near-field communication (NFC) allows for humans to communicate with objects.

The World's Thinnest Technology—Only Two Atoms Thick ▶

The innovative technology may significantly improve electronic devices in terms of speed, density, and energy consumption.

Purdue to Lead Indiana Coalition to Develop Quantum Technologies ▶

Purdue University is leading efforts to establish a National Science Foundation-backed quantum research center that would bring dozens of scientists from four research partners and industry together to tackle applied research in the field.

Samsung, KT Launch First Commercial 5G SA Network in Korea ▶

Samsung Electronics and KT Corporation (KT) announced they have successfully launched Korea's first commercial 5G SA network, turning on next-generation service in the country.

DFM SURVEYS:
The Readers Speak

Feature Survey by Andy Shaughnessy
I-CONNECT007

As many of you know, we survey our I-Connect007 readers frequently so that we can keep on top of the issues and challenges that are affecting you every day. According to our surveys, DFM issues continue to be problematic for PCB designers, design engineers, and fabricators alike.

This issue of *PCB007 Magazine* focuses on DFM from the fab point of view, but it's instructive to understand what designers are dealing with as well. In a recent Design007 survey of PCB designers and design engineers, fully one-third of respondents pointed to DFM issues as their greatest current challenge (Figure 1).

Each time we survey our readers, the comments always tell the real story. Here are the top 15 comments we received as replies to the question, "What is the biggest PCB design challenge that you or your company deal with regularly?" Comments are edited lightly for clarity.

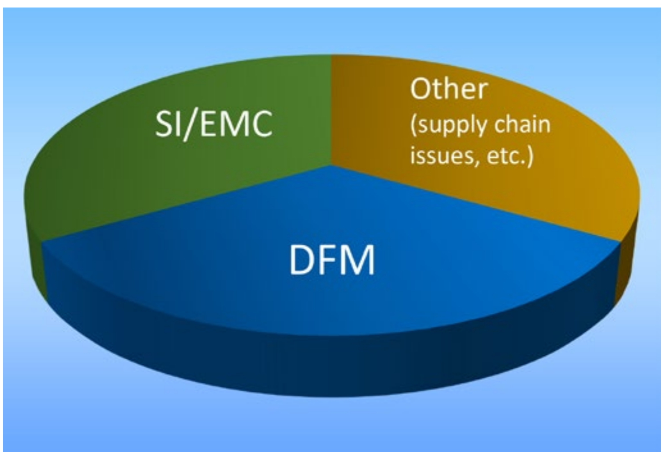


Figure 1: One-third of respondents named DFM issues as their biggest problem, tied with signal integrity/EMI and "other," which includes primarily supply chain issues, form factor updates, cost, and EDA tool issues.

- How to handle different offshore vendors who can't get the same material specified on the layer stack-up
- Rushing to production
- DFM for HDI
- Manufacturing optimization is often rare
- DFM rules are hard to comply with due to ever-decreasing board size and most of the time the violations are concentrated at component spacing
- DFM combined with strict HDI designs
- DFM, DFA, DFT and footprint libraries
- Fabs overpromising in terms of schedule and capabilities
- Not taking time to perform design analysis up front
- Getting complete and correct part data into our systems
- Lack of communication between designer and EMS provider during initial design and layout
- Manufacturing issues with solder mask
- Dumb mistakes, e.g., mirrored connectors
- Demystifying fab notes
- Time to market limits DFM, DRC

The I-Connect007 Research Team regularly solicits your feedback, which is vital in helping us create content that is both relevant and timely to our industry. We appreciate your time in responding to surveys and providing comments as needed. **PCB007**

Rigid-Flex Design Without Respins:

A Webinar Review

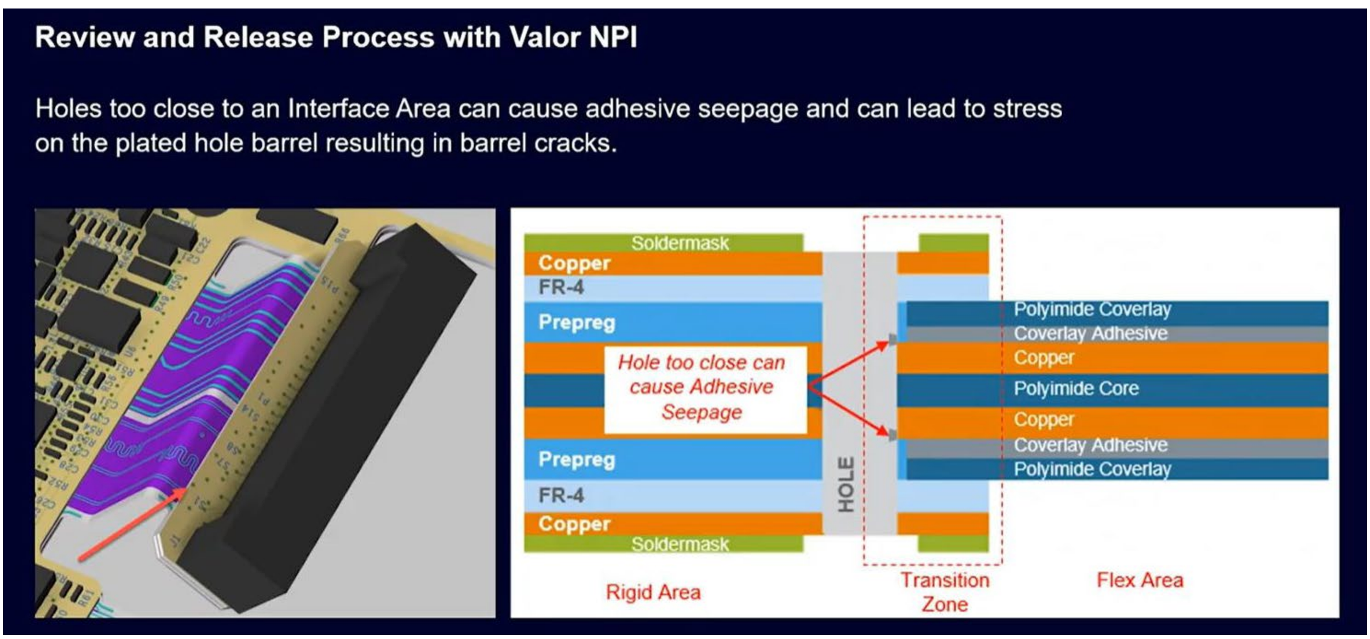
Feature Article by Andy Shaughnessy
I-CONNECT007

Editor's Note: This article was originally published in the July 2021 issue of Design007 Magazine.

Rigid-flex circuits have become almost ubiquitous over the past decade; most personal electronic devices contain at least one rigid-flex circuit. But there's a downside to rigid-flex: Respins are almost a given with rigid-flex designs. And rigid-flex respins can be quite expensive, since this technology costs quite a bit more, on average, than flex or rigid boards.

In this free 22-minute on-demand webinar, *Flex & Rigid-flex DFM Analysis,* Kevin Webb, an NPI technical marketing engineer with Siemens EDA, explains how using Valor NPI early in your rigid-flex design flow can help you reduce your rigid-flex respins, or possibly even eliminate them completely.

Webb discusses how Siemens' drive to "left-shift" manufacturing information into the designer's hands allows rigid-flex designers to make more informed decisions early in the design cycle, where mistakes are less costly. Webb walks the user through a typical rigid-flex design, explaining how Valor NPI is optimized to work with rigid-flex circuits. The



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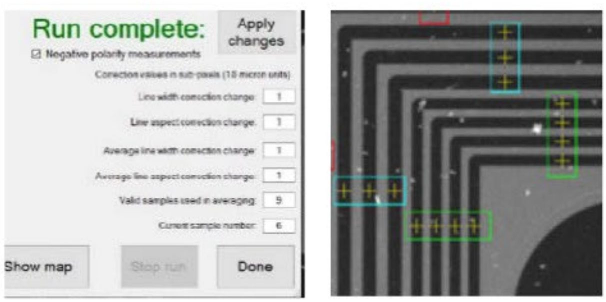

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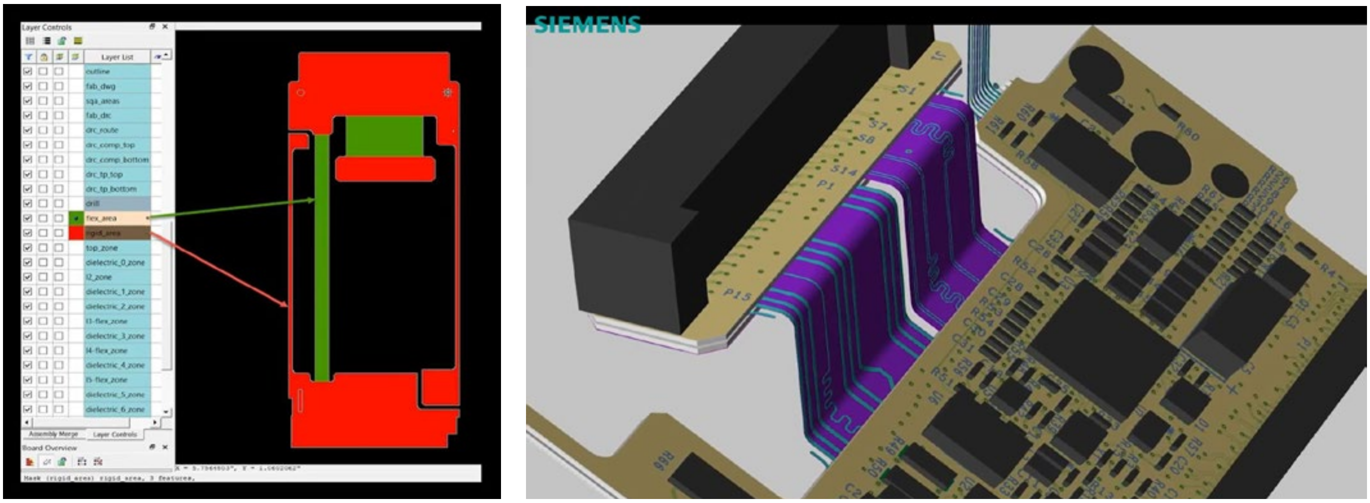

Figure 1: The webinar explains how Valor NPI detects errors in rigid-flex designs. The software includes 3D view, a handy feature for rigid-flex.

system helps the designer perform manufacturing checks that are unique to rigid-flex, such as overlapping traces that cause an undesirable "I-Beam effect," or plated through-holes and vias in bend areas (keep-out areas), which could lead to barrel fracturing and open circuits. Webb also demonstrates how to use Valor's Manufacturing Risk Analysis to identify potential problem areas in the circuit; designers can set the tool to report all errors, or only errors in critical areas.

Webb manages to pack a lot of information into a webinar that rigid-flex designers can watch during their lunch break and still have time left over. If you design rigid-flex circuits, no matter what your skill level is, this is a must-watch webinar. **PCB007**

Access webinar here.

Putting a Strain on Semiconductors for Next-gen Chips

Skoltech researchers and their colleagues from the U.S. and Singapore have created a neural network that can help tweak semiconductor crystals in a controlled fashion to achieve superior properties for electronics. This enables a new direction of development of next-generation chips and solar cells by exploiting a controllable deformation that may change the properties of a material on the fly. The paper was published in the journal npj Computational Materials.

Materials at the nanoscale can withstand major deformation. In what's called the strained state, they can exhibit remarkable optical, thermal, electronic, and other properties due to a change in interatomic distances. The intrinsic properties of a strained material may change, with the semiconducting silicon, for instance, transforming into a material that conducts the electric current freely.

Moreover, by varying the strain level, one can change these properties on demand. That notion has given rise to an entire field of inquiry: elastic strain engineering, or ESE. The approach can be used, for example, to modify the performance of semiconductors, providing a potential workaround for the impending Moore's law limit, when we exhaust our other options for increasing chip performance. Another possible application lies within the field of solar cell development. As study co-author Alexander Shapeev from Skoltech explains, one can design a solar cell with tunable properties that can be changed on demand in order to maximize performance and adapt to external circumstances.

(Source: Skoltech)

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Jumping the Technology Curve Collaboration With Your Competition

Trouble in Your Tank

by Michael Carano, RBP CHEMICAL TECHNOLOGY

Jumping the Technology Curve

Regardless of the industry in which one competes, there is constant pressure to develop new products and penetrate new markets. This difficulty is heightened when your company is situated in a high-technology industry such as electronics, which requires continuous investment in equipment, infrastructure, processes and, of course, skilled workers.

With increased competition coming from many of the so-called "low-cost countries" in Asia, small- and medium-sized printed circuit board and circuit assembly companies in North America and Europe are finding it difficult to compete. Certainly, they are not able to compete on cost alone. This would simply result in a race to the bottom.

At the end of the day, successful technology firms must up their game with respect to innovation, quality and yields, on-time delivery (meaning really fast), and managing increasingly complex interconnect devices. Recognizing that higher margins and profits lie in the state-of-the-art and leading-edge categories, how can a small firm that is unable to fund such innovation get into the game? The answer lies in either joining or forming an industry consortium or loose group of companies to share resources for the good of each firm.

Interestingly, most executives today are looking for significant government funds to maintain and enhance their companies' competitiveness on the global stage. While this may be viable for some of the largest companies, the smaller enabling firms that are critical to the supply chain are often left out of the discussion. Certainly, the behemoth firms in the semiconductor and medical industries feel they can go it alone if only there were enough cash and tax breaks forthcoming. The argu-

ments put forth are in the vein of national security, job creation, and technological leadership—and they have their merits.

However, from another perspective, this thinking is somewhat flawed.

One can recall the Foxconn project that was highly touted to bring 13,000-plus jobs to the state of Wisconsin. The original project called for the construction of a very large LCD factory with an initial investment of $10 billion. Now, the official word is that the factory will be drastically scaled down. Foxconn will now employ 1,454 people and invest $672 million. With the amended agreement, Foxconn will only be eligible for tax breaks of $80 million, down from the original $2.85 billion[1]. Even if the project met its original employment projections, what would be the end results for the state of Wisconsin? One will never know.

Could taxpayer funds be deployed in other ways to spur innovation and employment growth? Perhaps additional investments in workforce training and skills development will help close the gap and provide the necessary impetus for technology firms to innovate and compete successfully with the low-cost locales. With all this said, how can smaller firms leverage their respective techniques and know-how through collaboration?

Collaboration and Consortium

The word consortium is derived from the Latin word "con" (together) and "sors" (fate). Indeed, a consortium is a business collaboration framework for companies to work together and share both the risks and the future rewards of the collaboration.

For some, collaborating with potential competitors is met with deep-rooted suspicion. This is just human nature. However, consider the lack of action or collaboration. One loses the opportunity to learn from a diverse group of companies and individuals. Potential collaborators are like a team of medical providers. Some may be general surgeons, others may be heart surgeons, and others may be nurses. Each brings a unique set of skills and know-how to saving someone's life. Together, the team stays focused on the task at hand.

The same can be said about collaboration for industrial innovations. Each individual partner brings valuable, unique skills that you may never acquire yourself. This is extremely useful when attempting to solve a specific problem or issue.

Each individual partner brings valuable, unique skills that you may never acquire yourself.

Collaboration is a golden opportunity to innovate. In his book, The Innovator's Dilemma, Clayton Christensen wrote about "disruptive technologies," describing how they gain market acceptance through small wins without necessarily drawing attention from larger firms who remain steeped in their tried-and-true technologies and products[2]. This is the opportunity to fly under the radar and allow the innovation to evolve over time. Essentially, this is an offering of a less than perfect product, however, one that is functional, reliable, and cost effective. Subsequent improvements can occur over time and can be done so relatively quickly. So, how do we get there? One can start by looking at clusters.

In The Competitive Advantage of Nations, author Michael E. Porter details his view of clusters, which are geographic concentrations of firms in similar industries and market segments. Some of these companies are suppliers to other firms, while others may help with logistics, warehousing, and ancillary services. One can even go a step further and look to universities in the region, along with testing laboratories and consultants who can support these firms[3].

Indeed, if one surveys the North American electronics industry supply chain, there are several of these clusters spread out across the United States. This includes:

- Chicago-Milwaukee-Minneapolis area
- Santa Clara/San Jose, California
- Orange County/San Diego, California
- Dallas-Fort Worth, Texas
- Phoenix/Chandler, Arizona

In each of these clusters, there are multiple printed circuit board fabricators and circuit board assembly companies. Suppliers of necessary materials and chemicals are also in these locations. While many of these firms are in competition with one another, there are opportunities to forge mutually beneficial relationships. These firms have several things in common. And, if these firms cooperate or collaborate in some way, significant benefits can accrue, including financial, technology, and efficiency gains.

Call to Action

The prevailing school of thought is that certain countries, the United States in particular, are not competitive in critical industries. One can cite the printed circuit board manufacturing and assembly industries. These two interrelated industries form the building blocks (substrates) and the conduit that join the semiconductor chips and packages to the final electronic product. Electronics are crucial in thousands of products from heart-lung machines to engine control systems for your automobile, or myriad other consumer items including smartphones and computers. Without highly reliable printed circuit boards and circuit assemblies, those complex chips and components cannot function. This somewhat dire assessment places the safety and security of the United States at risk. The supply chain is already fragile due to numerous factors that have been presented elsewhere.

One idea is to form, under the umbrella of IPC, an HDI institute to work on innovations in high density and ultra-high-density interconnects. The consortia would focus on jumping the curve with respect to the state-of-the-art and leading-edge printed circuit board technology. The specific focus would be on the development of enabling technologies to manufacture interconnect devices to support chip packaging, semiconductor fabrication, interposers, and high-end internet infrastructure and telephony. In addition, the HDI institute would support mission-critical defense/aerospace applications.

Without highly reliable printed circuit boards and circuit assemblies, those complex chips and components cannot function.

The consortia could be located in various clusters within the United States. Consider three separate "consortia." Each separate group would focus on developing and delivering leading-edge and state-of-the-art printed wiring board interconnection substrates. The membership in each location could consist of three to five printed wiring board fabricators. These fabricators must be willing to share resources and essentially act as one company in each region. The business model for each consortium would be designed to compete on differentiation, not on price. The model would revolve around higher technology, e.g., higher layer counts, fine pitch HDI and ultra HDI, manufacturing efficiencies, and marketing expertise. The latter will provide connections to the end users in support of the higher technology offerings of the consortia.

Now, is this only about collaboration to solve a particular technical issue? No, this goes deeper than that. This is about leverage, whereby the members of the consortia form a for-profit company outside of their individual entities. Each member of the consortia would provide expertise and the processes that will enable the entity to bring these complex interconnection substrates to the market. As an example, one member would provide ultra-fine line imaging services; another would provide the required array of solderable finishes; another would provide the via-filling capability, and so on. Since the members of each consortium would be in close proximity to each other, the logistics of moving boards from one member's facility to the other would be simplified. Essentially the members of the consortia select the best practices and capabilities of each member. This ensures that the entity can deliver high technology, high reliability product to the end user. **PCB007**

References

1. Josh Dzieza, "Wisconsin amends Foxconn's contract to reflect radically smaller project," The Verge, April 20, 2021.
2. Clayton M. Christianson, et al. The Innovator's Dilemma, The Harvard Business Review Press, 1st edition, May 1, 1997, pages 93-97.
3. Michael E. Porter, The Competitive Advantage of Nations, Harvard Business Review, Vol. 68, No. 2, 1990, pp.73-93.

Mike Carano is IPC TLP chair, and vice president of technology and business development for RBP Chemical Technology, Inc. To read past columns or contact Carano, click here.

MilAero007 Highlights

Defense Speak Interpreted: POM—Explaining the Process for Defense Budgeting ▶

Anyone hanging around Defense programs will have surely heard of the term "POM." Most of the connotations I have heard say that if you have a POM or will get "POM'd," your program is "skating on solid ice." That led me to infer that if you were in the POM, your program was established. But why and how?

Coalition Calls on Congress to Invest in Domestic Semiconductor Manufacturing, Research, Design ▶

The Semiconductor Industry Association—along with a broad coalition of 19 other tech, auto, medical, defense, and other business and labor groups—in a letter urged Congress to enact funding for the semiconductor manufacturing, research, and design initiatives authorized in the "Creating Helpful Incentives for the Production of Semiconductors" (CHIPS) for America Act.

Mars Rover Mission Only Just Beginning One Year After its Launch ▶

Of all the exciting aspects a space mission entails for a planetary scientist who makes a living studying the outer limits, it's still the launch from ground zero that gets Briony Horgan's heart-pounding the most.

Adventures in Engineering: Test Points—The Other Side ▶

In many instances test points are a critical part of the process for launching, producing, and maintaining a successful product. Sadly, many times test points are left as an afterthought and squeezed/pushed into a design after PCB layout is "complete," signal integrity analysis is "done," and all but the final design review remains. Now, let's see what we can do to effectively place test points in our CCAs.

Key Tronic Reports Results for Q3 Fiscal Year 2021, New Program Win ▶

Key Tronic Corporation, a provider of electronic manufacturing services, announced its results for the quarter ended April 3, 2021. Reporting the results for the third quarter of fiscal 2021 was delayed until the Audit Committee of the company's board of directors completed its previously announced internal investigation.

Ducommun, an Airbus Detail Parts Partner, Awarded Multi-Year Contract ▶

Ducommun Incorporated, a global supplier of innovative electronic and structural solutions for the aerospace and defense industry, announced that it has been recognized as an Airbus Detail Parts Partner (D2P) and awarded a long-term, five-year contract to provide a titanium work package for key products on the A320 and A330 programs.

NASA's Self-Driving Perseverance Mars Rover 'Takes the Wheel' ▶

NASA's newest six-wheeled robot on Mars, the Perseverance rover, is beginning an epic journey across a crater floor seeking signs of ancient life. That means the rover team is deeply engaged with planning navigation routes, drafting instructions to be beamed up, even donning special 3D glasses to help map their course.

Holy Cow, What a Lead Time!

The PCB Norsemen

by Jan Pedersen, ELMATICA

It's summer and we are adapting to our second COVID summer. However, things are most definitely a bit different these days. Recently I got an order, just like every day. The designer had spent the last three weeks completing the design and got it approved for order placement. The next step in the flow is when the purchaser spends a few days to get prices right, and then the order can be placed.

Anything Wrong With This?

No, it's business as usual to make sure the design is correct, and prices are negotiated to save money. This is an everyday operation in this industry. However, in a normal year, with normal material lead times, and without escalating material prices, that is how it works.

Today, Things Are a Bit Different

Let me elaborate on an example from the last few weeks. I was contacted by a designer requesting a stackup for an eight-layer PCB. This was a quite standard stackup that could work for most eight-layer designs, meaning that he would need impedance per design, but not controlled, no microvias, and no critical thickness requirements.

But this designer always requests a stackup including the exact materials used, to match his lines to the stackup. Basically, this stackup works for most eight-layer designs, even for those with impedance lines. As long as we don't change the track, gap, and stackup, it will work. After this, the designer spends two to three weeks on the design. After one week he

was more or less done, but had the design sent for verification before he closed it and submitted it to procurement.

What About the Stackup and Changes?

The purchaser received the Gerber files and submitted his request for quotation to two or three of his most trusted PCB suppliers. He got the first quotation within eight hours but decided to wait another two days to make sure he had the best price. Order placed as usual, but now things started to happen.

The PCB factory replied that the material supplier for this brand and type suddenly had eight-week lead time. He sent back an engineering query for alternative materials that would keep the stackup and those designed impedance lines. Designer rejected; the stackup had been approved by the end customer with no chance to change it now. So, what happens next? The EQ is sent back to the PCB supplier, with the result of a five- to six-week increased lead time compared to the original offer.

What Can We Learn?

First, in a normal situation this is not necessarily an issue, but today with increased and less predictable material lead times, and on top of unpredictable material prices, we need to adapt to the situation and be smart.

But How?

First, make sure the stackup and material selection is as open as possible.

1. Don't lock your stackup to one material brand or type of material. Allow for factory standard materials to be used.
2. Try to use IPC 4101 slash sheet numbers, unless you have special needs.
3. If you have impedance lines designed in, make sure to describe what you need. The factory will in 99% of the cases be able to tune track and gap to meet their standard materials.
4. If you ask for a factory stackup, make sure you allow standard materials to be used.
5. Also consider releasing the stackup for material to be allocated, or even placing a material preorder.

By these actions, you can simplify the process of approving the design, and, as we currently face an unpredictable material situation, avoid sudden increased material lead times from when the stackup is approved, and up to order placement. Remember that the PCB factory doesn't order material before all EQs have been closed, adding on another two to seven days.

Is Price the Key to Success?

We all know price matters when procuring printed circuits. Some buyers only target on price, benchmarking, and swapping suppliers more often than the Kardashians shoot selfies. Long term relationships might sound boring, but also offer predictability, priority, and dual source if needed. Just to specify, I am only talking about relationships with your PCB supplier.

In a market like today, a few pennies saved can be at a high cost. My advice after decades in the industry and facing the current challenges daily:

1. Place the material allocation order as early as possible—as soon as the stackup is fixed.
2. Don't start negotiation prices and lead times the day you expect to place the order; it is too late. Not even the same week.
3. Select a trusted supplier that accepts material allocation on orders and stay with them.
4. Work on long time trust and be predictable within the nature of your business.

Be Realistic

The last thing I want to mention is the need for a PCB supplier that has skills and knowledge to guide you in the right direction. As in all matters of life, procuring printed circuits is also about finding solutions. We aim to guide our customers in a material selection, available within reasonable time. Finding solutions that combine function and availability is vital.

Today, the best direction is not necessarily to meet all the customers' needs, finding special materials, or processes, but maybe all of this in combination with a realistic view of what can be done, within a reasonable time.

Until last autumn, we did not have this understanding. Today, it is vital to reach the market in time. My senior technical advisor colleagues and I aim to maintain the attitude, "Nothing is impossible, we will find a solution."

That is still true, and in 90% of the cases it's possible. However, "the material availability ghost" is haunting the industry every day, which means we also need to use all our skills and knowledge about material lead times to find good solutions for the customers, and maybe most importantly, realistic, and reliable solutions. PCB007

Jan Pedersen is a senior technical advisor at Elmatica. To read past columns or contact The PCB Norsemen, click here.

Spin-sonics: Acoustic Wave Gets the Electrons Spinning

Researchers have detected the rolling movement of a nano-acoustic wave predicted by the famous physicist and Nobel prize winner Lord Rayleigh in 1885. This phenomenon can find applications in acoustic quantum technologies or in so-called "phononic" components, which are used to control the propagation of acoustic waves.

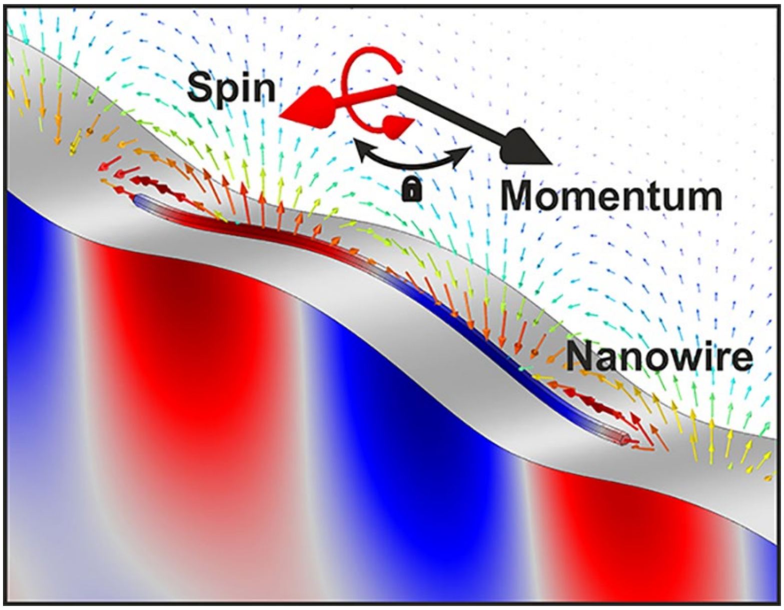
A research team used a nanowire inside which electrons are forced onto circular paths by the spin of the acoustic wave. Acoustic waves are incredibly versatile in modern nanophysics, as they can influence both electronic and photonic systems. For example, minute micro-acoustic chips in computers, smartphones or tablets ensure that the wireless signals received are electronically processed. However, despite wide-ranging uses of nano-acoustic waves, the fundamental property of spin of the nano-acoustic wave had not been detected until this study.

In their study, the researchers used an extremely fine nanowire that was positioned on a so-called piezoelectric material, lithium niobate. This material becomes deformed when subjected to an electrical current, and, with the aid of small metal electrodes, an acoustic wave can be generated on the material.

On the surface of the material, the acoustic wave generates an elliptically rotating (gyrating) electrical field. This, in turn, forces the electrons in the nanowire onto circular paths.

"So far we knew about this phenomenon for light," said Zubin Jacob, Purdue's Elmore Associate Professor of Electrical and Computer Engineering. "Now we have succeeded in demonstrating that this is a universal effect, which also occurs in other types of waves such as sound waves on a technologically important platform, lithium niobate."

(Source: Purdue University)



Representation of the spin of a nanoscale acoustic wave. Credit: Maximilian Sonner, Institute of Physics at the University of Augsburg.

Better by Design—Bringing PCB Design Professionals Together

One World, One Industry

by Dr. John Mitchell, IPC PRESIDENT AND CEO

As a member-driven organization, IPC works diligently to help our member OEMs, EMS companies, PCB manufacturers, and suppliers build electronics better. And we all know that you cannot build a great product without a great design.

To focus on the critical role design plays in the development of electronics, we created IPC Design to bring together printed board design professionals to connect with other designers, enjoy education and training opportunities, mentor and encourage the next generation of designer engineers, and above all, help advance the art and science of printed board design.

We welcome all designers to participate in IPC Design by becoming an affiliate—a free, zero-obligation way to expand your professional network. At no cost to you, you will have the opportunity to interact with academia and the next generation of printed board professionals, while also being the first in line for IPC events, including webinars, competitions, and other opportunities for you to connect with fellow designers. As IPC joins the industry in getting back to "business as usual," affiliates will be given the chance to voice their needs and help create the next generation of IPC Design activities.

Affiliation in IPC Design is completely free. You can register online.

IPC Design affiliates have already contributed their time to the development of a PCB Design Desk Reference, a table-top guide to

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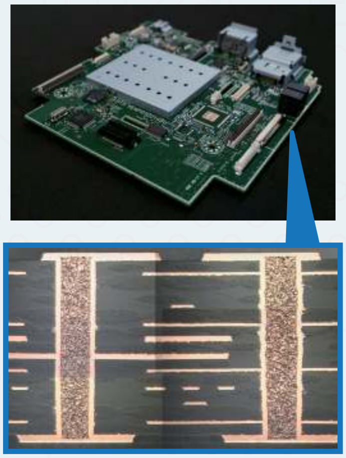
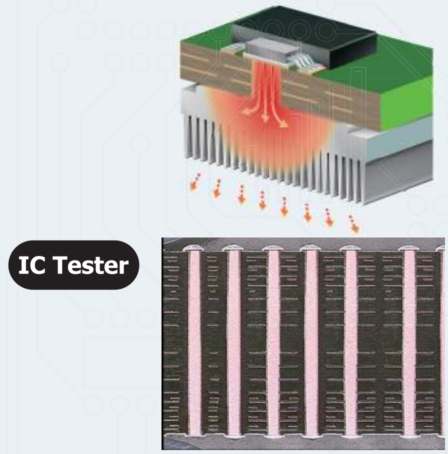


Device Solution for Thermal Management of PCB



Metalizing Paste - TLPS Type
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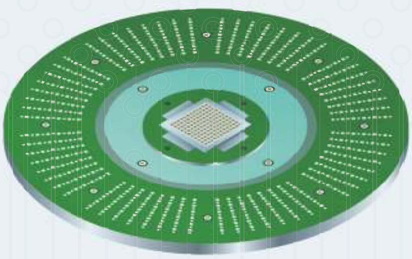
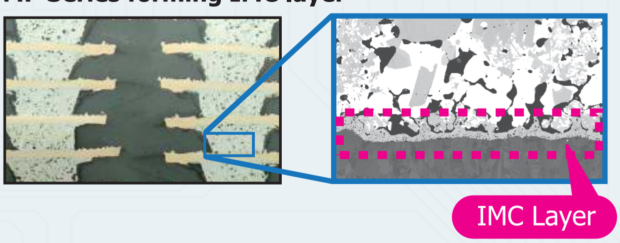


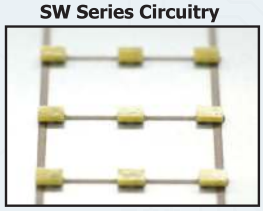
MP Series forming IMC layer



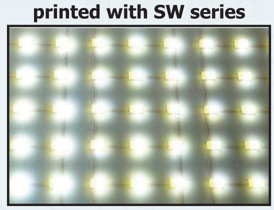
Circuitry Paste
SW Series

For Circuitry of LED Backlight Display

LED lights connected by SW Series Circuitry



LED powered by circuits printed with SW series



Manufacturer
TATSUTA
Kyoto, Japan

Agent
all4-PCB WORLDWIDE

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345 Mira Loma Avenue Glendale, CA 91204 USA

designing boards in accordance with IPC design standards, which will be available later this year.

The IPC Design Competition, scheduled for IPC APEX EXPO 2022, will test the design aptitude of professional designers from around the world. The preliminary heat will consist of a full board build-up: starting with a schematic, some mechanical/packaging constraints, and a pre-defined component library, competitors will be required to complete a design task in accordance with relevant IPC standards, culminating in a standard-compliant documentation package and IPC-2581 file. Finalists are chosen from this round and invited to APEX EXPO 2022. The in-person event will consist of a very low-complexity board (blinky-board or similar) with predefined stackup and component library; the best layout wins!

Also, at IPC APEX EXPO 2022, IPC Design will host a "Day of DFX" with panels covering topics such as designing for manufacturing, testability, assembly, and much more.

IPC provides educational opportunities in design, whether you or your team need an introductory course or advanced design knowledge. Designing for smaller, more complex, and more robust electronics devices requires creative thinking and extensive theoretical and applied knowledge. To meet these challenges, IPC Design courses were developed to help designers across different sectors of the industry acquire and sharpen skills required to design and manufacture innovative products that ensure organizational profitability. Currently, IPC offers two introductory, two intermediate, and five advanced design courses.

In addition to design courses, we offer the IPC Designer Certification program at IPC-licensed training centers worldwide. Both certifications, one basic and one advanced, provide objective evaluation of core competencies in PCB design, providing instruction in how to transform an electrical circuit description into a PCB design that can be manufactured, assembled, and tested.

IPC courses are taught by industry veterans who provide intensive training for learners to deliver effective and reliable design to customers. Information on IPC Design courses and certification can be found by visiting ipc.org.

We hope you'll participate in all the opportunities offered through IPC Design. As always, please reach out to me with any questions or comments. I look forward to hearing from you. PCB007

Dr. John Mitchell is president and CEO of IPC. To read past columns or contact him, click here.

Supplier Highlights

MKS Expands in Asia with Newest HDI PCB Laser Manufacturing Solution

MKS Instruments, Inc., a global provider of technologies that enable advanced processes and improve productivity, announced confirmation of an order for the ESI® Geode™ HDI via drilling system from TTM Technologies, Inc., a technology leader in the HDI PCB manufacturing market, for their facility in Guangzhou, China.

Rogers Reports Second Quarter 2021 Results

Net sales of $234.9 million increased 2.5% vs. the prior quarter from higher sales in the AES business unit. AES net sales increased primarily due to strong demand for EV/HEV applications and higher clean energy, defense, and wireless infrastructure market sales, partially offset by a decline in sales for ADAS applications.

Altix Receives New Order for AcuReel XL Imaging System

Altix is thrilled to receive its first order of its AcuReel XL from a major European FPC manufacturer. Dedicated to all FPC processes with an exposure area up to 500 x 1500mm, the AcuReel XL is the ideal contact exposure solution for automotive-related FPC production and other markets requesting extra-large imaging formats.

Candor Invests in On-demand Inkjet Printing System from MicroCraft

Toronto PCB fabricator Candor Circuit Boards has recently purchased and installed a MicroCraft CPQ7861 on-demand inkjet printing system, one of the fastest in the MicroCraft lineup.

Printed Circuits Completes Qualification of Notion Direct Soldermask, Nomenclature Printer

Rigid flex circuit board manufacturer Printed Circuits has completed the installation of the process line and qualification of their new Notion direct solder mask and nomenclature printer.

Ucamco's New Gerber Job Editor Now Accepts Notes in Chinese

Gerber Job Editor, Ucamco's software that allows designers to create and edit job files that provide all essential PCB production data, has been significantly improved. The tool now accepts notes in Chinese. This is a huge milestone in the evolution of the tool, which has clear advantages for the Chinese PCB market.

TTM Installs Orbotech Neos 800 Additive Printing Solution

Orbotech, a KLA company, announced that TTM Technologies, a global manufacturer of printed circuit boards and radio frequency components and assemblies, purchased and installed an Orbotech Neos™ 800, transforming the way solder mask is applied to PCBs.

EMC and Technica to Introduce New Extreme Low Loss High Speed Materials at DesignCon 2021

EMC and Technica invited OEMs, ODMs and PCB fabricators to stop by Booth #406 at DesignCon 2021 to learn more about these and other high-speed products they offer.

Design for Manufacturing? Don't Forget Test!

Testing Todd

by Todd Kolmodin, GARDIEN SERVICES USA

Over the last 35 years we have seen astonishing advances in printed circuits, flex circuits, and component technology. The introduction of surface mount technology back in the '80s and the continued progression of that technology has proven to be a challenge for PCB manufacturers and the electrical test arena as well.

From a development engineer standpoint, the task is to economically create the design using the best available technologies that provide the optimum result. This includes, but is not limited to, component packages, blind and buried via technology, and buried passives, while also considering the manufacturing abilities of the selected PCB fab vendor. Considerations are line width, spacing, component density, and deliverable characteristics such as TDR, HiPot, inductance, and of course, overall electrical compliance. In the early days this was never a problem as most PCBs were plated through-hole (PTH) and electrical test was straightforward. Not so much today.

Design for manufacturing (DFM) is a great discipline for creating designs that provide optimum performance while still maintaining affordability. However, what can be, and does get overlooked, is the design for test (DFT) variable. As greater manufacturing demands are put to the manufacturer, it also creates challenges to validate the electrical deliverables that may be required.

From an electrical test standpoint, the layer count of a given PCB is not an issue. The CAM systems of today can process many layers including blind/buried vias, buried passives and the like. The challenge becomes the actual test. Net intelligence is not the hurdle but how to effectively interrogate the PCB to provide vali-

dation of the electrical characteristics. Historically this has been easy.

Fixture technology and fixture testers were all the rave through the '80s, '90s, and into the new millennium. Using headed pin technology through featureless music wire allowed the successful test of most designs. Even with the higher density, the CAM systems were able to split fixtures to A and B tests to encapsulate the extremely dense PCBs. Unfortunately, this has some drawbacks. The extra fixtures and increased drilling and assembly time adds cost and time to the equation. Whether ET is captured in the quoting process by the manufacturer will be the decision of the individual manufacturer, but these costs are real in both time and materials/labor.

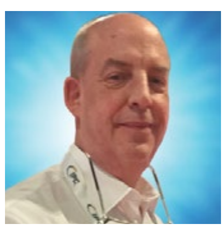
As today's designs get more complex, economics come in to play as to whether fixtures are the answer.

As today's designs get more complex, economics come in to play as to whether fixtures are the answer. Extremely dense designs are now requiring quad-density or greater to still utilize fixture technology, or they are being converted to dedicated spring probe fixtures that are very costly. These variables are usually not considered during the quoting process (remember DFT) and can cause loss of margin by the time the electrical deliverables are met.

Now, today's flying probe machines can test extremely dense designs without using fixtures. The cost is much less but there are tradeoffs from the fixture test. Flying probes cannot provide the full parametric test that fixture testers can provide. This can be an issue when testing some military, aerospace, and high reliability medical products. These require the "simultaneous" test of the PCB for opens and more importantly, shorts. So, in some of these cases a fixture or multiple fixtures will be required. This increases cost and can cause delays in the manufacturing window due to manufacture of the fixture(s).

Where is this going? Design for test. Speaking for the ET arena, PCB designers are encouraged to take into consideration how their electrical deliverables can be met. Sure, flying probes can tackle most designs and requirements of today, including test of buried passives, HiPot, inductance, and even capacitance. However, in high-reliability products that require full parametric tests, fixtures will be required. Here is where consideration will be most beneficial. Consult with your manufacturer on electrical test density capabilities to make sure your design can be tested effectively. If your design is beyond the capability, consider adding a pad or feature to allow the effective probing of the network. Sometimes adding a small 0.010-0.015" pad, spaced appropriately for ET capability, may turn your untestable design into a routine build. This can be increasingly effective for wire-bond technology where direct probing of the wire-bond pristine area is prohibited. Doing so may stress you out a bit finding real estate to add these features for test, but usually this would not increase the price of the actual PCB build. However, it does make a significant difference in the testability of the PCB design.

While DFM is an absolute necessity in the market of today, DFT needs the attention more today than ever. An overall great design implementing DFM and DFT will make the manufacturing cycle less expensive and keep the time frame for deliverables in check. Don't forget ET. PCB007



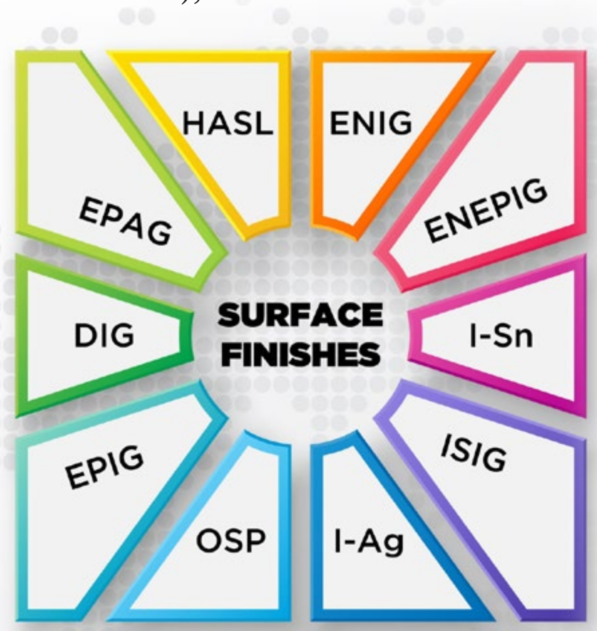
Todd Kolmodin is VP of quality for Gardien Services USA and an expert in electrical test and reliability issues. To read past columns or contact Kolmodin, click here.

An Overview of Surface Finishes

The Plating Forum

by George Milad, UYEMURA

Surface finish R&D departments on the supplier side have been very busy coming up with new finishes to meet the everchanging demands of the electronics industry. Today, designers have wide variety of finishes to choose from: HASL (hot air solder leveling), electrolytic nickel gold, OSP (organic solderabilty preservative), ENIG (electroless nickel/immersion gold), I-Ag (immersion silver), I-Sn (immersion tin), ENEPIG (electroless nickel/electroless palladium/immersion gold), EPIG (electroless palladium/immersion gold), EPAG (electroless palladium/auto-catalytic gold), DIG (direct immersion gold), and ISIG (immersion silver/immersion gold). In addition, most finishes offer variations within their process; specifying thickness of the layers and the type of electrolyte is used to meet specific performance criteria.



Historically, HASL was among the first finishes that saw wide use as a solderable finish. HASL was accompanied by tin-lead reflow where it was suitable, as long as tin-lead soldering remained the primary assembly method. Both HASL and tin-lead reflow required a thermal excursion. The technology (mostly double-sided) at that time could tolerate it.

OSP was introduced as a simpler, faster, and safer procedure. OSP gained market share as long as the primary assembly method required only a single excursion to tin-lead reflow temperature.

With the introduction of SMOBC (solder mask over bare copper), the dominant finishes were HASL and OSP for pads and electrolytic nickel/electrolytic hard gold for contacting fingers.

As MLB (multilayer boards) and surface mount were introduced, HASL topography (lack of planarity) became a problem at assembly as the pad size continued to shrink. ENIG and OSP became the better choices. ENIG had the advantage over OSP in that it withstands multiple thermal excursions required at assembly. ENIG was also aluminum wire bondable and a good metallic contacting surface. All these advantages justified the higher cost and complexity of processing associate with ENIG.

For a few years, ENIG, HASL, OSP, and electrolytic nickel gold were the staple for the industry, with HASL and OSP for simpler

products that require a single thermal excursion at assembly. ENIG was the choice for surface mount and BGA (ball grid array) used for surface mount, where co-planarity was paramount. Electrolytic nickel gold was used to plate hard gold over nickel for insertion fingers and with a thicker, soft gold layer it was the choice for gold wire bonding.

With the introduction of lead-free (LF) solder—an example is SAC 305—the reflow temperature was increased from 230°C to 260 °C.

ENIG had the advantage over OSP in that it withstands multiple thermal excursions required at assembly.

Standard OSPs could not withstand the reflow temperature of LF solder and a new generation of high temperature (HT) OSPs came to the market. This class of OSPs could withstand the increased reflow temp of LF solder and was capable of withstanding multiple thermal excursions.

In the same time frame, the industry saw the introduction of immersion silver and immersion tin. Immersion silver (a metallic surface finish) is a solderable, coplanar contacting surface. Although silver had some limitations like tarnishing and creep corrosion, it has its place with certain process modifications to contain tarnishing and creep corrosion. Immersion tin became a viable finish, particularly for press fit type connectors where its lubricity came in play. Of course, it was solderable for LF solder. For immersion tin, the IPC specified a thick layer (40 µin or one micron) to counter the natural tendency to form an IMC (copper-tin intermetallic) on storage or thermal excursion. If the IMC works its way to the surface it would render the surface non-solderable.

With continued miniaturization, electrolytic nickel gold for gold wire bonding became a problem as it required electrical continuity through bussing. There was a need for a gold wire-bondable surface that was non-electrolytic; this resulted in the development of the ENEPIG (electroless nickel, electroless palladium, immersion gold) surface finish. The palladium layer between the nickel and the surface gold is a diffusion barrier to the migration of nickel to the surface, which can create bond failures. ENEPIG offered all the advantages of ENIG plus gold wire bonding.

As the use of wireless networks and handheld devices continued to grow, massive data is transmitted through printed circuit boards in the form of high frequency RF signals. It became clear that the electroless nickel layer in ENIG and ENEPIG will create signal loss. This brought about the development of nickel-free surface finishes. At present there is commercially available EPIG and EPAG, both nickel-free. Another finish that fits the bill is thicker DIG. I wrote about DIG in a previous column. A new addition to this group is ISIG, which is presently under development.

On the manufacturing end, board shops choose the surface finishes they offer to their customer base. The newer finishes that are in limited demand are relegated to contract plating shops. These shops offer a wider variety of surface finishes to the board shop, which will, in turn, subcontract their services. As the demand increases, the board shop will eventually set up the capability in house.

Designers have a lot of choices where they balance availability, cost, manufacturability, and performance. In some instances, specific finishes are the only option (for example, nickel-free finishes for RF signal propagation). Designers also must specify the thickness that would meet their design criteria.

The IPC Plating Committee has put out specifications for ENIG, I-Ag, I-Sn, and ENEPIG. In the specifications, a thickness range for the different layers is included, as well as performance criteria. Designers can call out the IPC specification in lieu of specifying thickness and performance. It is important to note here that designers have the option of taking exception with any parts of the specification. Such exceptions are noted in the design drawings.

All the finishes discussed here have big pluses as well as certain limitations. All the finishes are in use today. Hardly any have been obsoleted. Simpler board designs and performance expectations are readily met by simpler finishes like HASL, I-Ag, I-Sn, and OSP. The more sophisticated designs require more complex finishes like ENIG, ENEPIG, EPIG/EPAG, DIG, and ISIG to meet the designer's performance expectations. **PCB007**

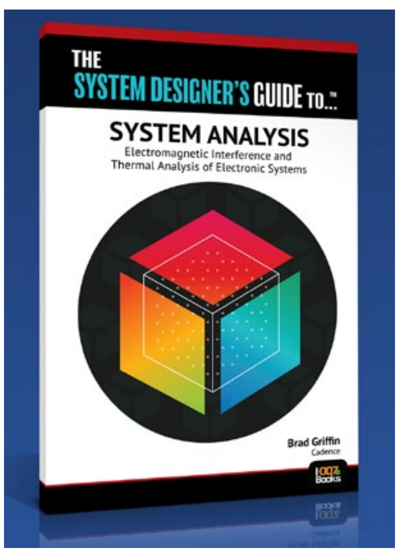
George Milad is the national accounts manager for technology at Uyemura. To read past columns or contact Milad, click here.

Excerpt: *The System Designer's Guide to… System Analysis,* Chapter 1

Chapter 1: Data Center Infrastructure and Requirements Related to Electronics Systems

System designers for 5G, automotive, high-performance computing (HPC), IoT, and other advanced applications have been facing growing challenges in EM interference and thermal issues. These are prevalent in all electronic devices. Data centers play a key role in this high-performance computing (HPC) era, and EMI/thermal issues have a huge impact on the performance of data centers. This book explains scenarios and issues based on the context of data center electronic systems.

The design, implementation, quality, and reliability guidelines as defined by the American National Standards Institute (ANSI) and the Telecommunications Industry Association (TIA) are critical considerations when developing leading-edge data centers. They directly translate into power, performance, area, integrity, and reliability requirements at every design and implementation stage of the electronic systems used to create the data center. Enterprises use data centers to house their business-critical applications and information from across the globe to aid better data management and security. The four main elements for the functioning of a computing environment are:



- Compute: Memory, local storage, and processing power
- Storage: Primary and backup storage devices Memory:
- Random access memory (RAM) and cache
- Networking: Equipment for connectivity ranging from routers and switches to controllers and firewalls

The high-density data flow and processing in data centers pose thermal and EMI issues at various levels in its computing environment. Hence it is extremely crucial to perform a thorough thermal/EMI analysis and optimization at the design level itself for every component at the individual as well as integrated level.

Data Center Categories

Data centers are classified into four main categories that serve different purposes depending on factors like destination, ownership, technology, and other characteristics.

To download this free eBook, published by I-Connect007, click here.

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Ucamco Improves Communication With Gerber Job Editor Notes in Mandarin

Feature Article by Andy Shaughnessy
I-CONNECT007

Ucamco recently announced that its Gerber Job Editor can now accept notes in Mandarin. This is a big step for Ucamco, the company that owns Gerber, which is the data transfer format used by most PCB designers. Other more "intelligent" data formats are making inroads in this area, but Gerber shows no signs of fading any time soon. I asked Karel Tavernier, managing director of Ucamco, to discuss the move to add Mandarin notes to the Gerber Job Editor, and what this means for CAM department users who may speak little or no English.

Andy Shaughnessy: Karel, Ucamco recently added Mandarin capability to the Gerber Jobs Editor. Would you walk us through this?

Karel Tavernier: Sure, but let's take a step back. The Gerber Job Editor edits Gerber Job Files. That's a file that was first introduced two or three years ago, and it contains data about the job in a formalized, standardized manner. The data includes copper weights, solder mask, whether the job is ITAR, etc. These are all kinds of things that relate to the job overall, and not necessarily specifically to a layer. That's something that Gerber will offer to the workflow, and there's no standard manner of transferring it. We put this in a separate sample JSON file. Why a separate file? Because plenty of CAD systems don't carry this data. Why should they? So, the ERP system contains this data. And asking the ERP programmer to understand PCB image data for simply defining a finish is not very realistic. A simple separate file is the way to go.

Shaughnessy: It's two different languages.

Tavernier: Yes. So why a JSON file? Because it's simple and human-readable. A few CAD systems have implemented it; Eagle is one of them; KiCad and a couple of others have implemented it too. We also know of ERP systems that generate the Gerber Job File. We created the Gerber Job Editor, a standalone application to view, create, and edit Job files.

Karel Tavernier

It serves as a debugging tool for the developers of Gerber Job data, but more importantly, it allows users to exchange this information in a standardized manner even if your CAD system does not carry this data.

The Gerber Job Editor is freely downloadable. You define your job parameters with a nice interface, and this can then help you fabricate your job. Or, if the fabricator does not want to use the Gerber Job Editor, he can just look at the JSON file and he can read what's there. Unless he was Chinese, until now. Because we had forgotten that China is the most important country in the world for PCBs. So it's all been in English until now. We received many requests from Chinese users, asking if we could provide a Mandarin interface. Of course, the data remains in English, because it's standardized work, but the interface is in Mandarin.

Shaughnessy: So a Mandarin-speaker will at least know what's in the file package.

Tavernier: Yes. The internal file data information remains in English. But the user interface can now be in Mandarin. Also, customer commands can be in Mandarin. People can add custom notes, as there are always things that are outside whatever standard we define. You can type it in any language. The Mandarin feature was released just a week or so ago.

Shaughnessy: The data itself stays in English, and I guess most of the manufacturers around the world have some facility with English if they're handling an international order. But this sort of facilitates it, right?

Tavernier: Yes. If it's a Gerber Job File, then they can open the Gerber Job Editor and it will be in Mandarin. That helps because the people handling this data are also not necessarily the CAM operator.

Shaughnessy: The files might be opened by an assistant, or an intern from a university.

Tavernier: Yes. That's right. Actually, the Job Editor will probably be used first on the low-end boards, because for the high-end boards, those OEMs have money to waste on inefficient data handoff from design to fabrication, but if you're selling a board for $5, how much money can you really spend on data input?

Shaughnessy: Does the Job Editor handle any other languages?

Tavernier: Yes—English, German, Japanese and Korean, and Mandarin. These are all the important languages for PCBs.

Shaughnessy: Do you have any idea how many or what percentage of manufacturers in China are using Gerber?

Tavernier: They all use Gerber. Most manufacturers only use Gerber. I know they sometimes

An example of Mandarin project notes as they appear in the Gerber Job Editor.

use old software. But I'm not sure how much is licensed, to put it politely. So if I had to say, going by the number of jobs, not in dollar volume, I think that over 95% of China's jobs are in Gerber.

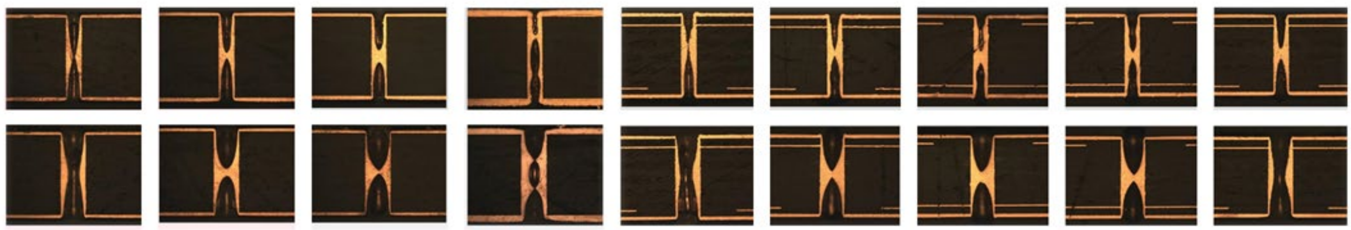
Shaughnessy: Right. We've seen a lot of updates in the newer formats, ODB++ and especially IPC-2581. But from what I've seen, Gerber reminds me of Mark Twain's quote, "Rumors of my demise have been greatly exaggerated."

Tavernier: Ah, yes. Indeed.

Shaughnessy: Well, Gerber certainly has some amazing staying power for being 50 years old and not even designed for this task.

Tavernier: Yes, that's why it's still here. And with Gerber X2 and the Gerber Job Editor, you can do anything—if you have the software, of course. If you work with 10-year-old software, then you cannot benefit from improvements in any format.

Shaughnessy: Thank you, Karel. Great talking to you. **PCB007**



One Step/One Bath Copper Through-Hole Fill Pulse Plating Process Across Wide Range of Panel Dimensions

Article by Nagarajan Jayaraju, Derek Thoresen, Jimmy John, Joanna Dziewiszek, David West, Zukhra Niazimbetova and Chi Yen
DUPONT

Introduction

Copper through-hole fill (THF) technology is a key breakthrough in sustaining the industry drive to increase wiring density and interconnect reliability while addressing the attendant challenges of thermal management and signal integrity at high frequencies. THF offers an elegant solution to the current process of plugging through-holes with conductive paste. The latter process involves multiple steps that are hard to control, making it expensive and making the plug itself unreliable and prone to thermal failures (such as degassing) under operation. THF, on the other hand, is a simple one-step electroplating process and, since copper is the filling material, it provides unmatched thermal performance.

Filled mechanically drilled through-holes are also an attractive replacement for stacked-via structures, especially for high-speed high-frequency applications. This is preferred since the single-piece cylindrical geometry of these through-holes results in less scattering of high frequency signal compared to the composite stacked-via structures with angled geometry and their susceptibility for misalignment during fabrication. Finally, THF can mitigate warpage of IC substrates during thermal processing by enabling fabrication of boards that are thicker but still have high interconnect density, as warpage rate and board thickness are inversely related.

Extensive screening of various organic additive formulations was conducted to achieve both bridging and filling in the same formulation. Candidate formulation was further optimized in conjunction with waveform and flow adjustments, resulting in a novel PPR waveforms process optimized for through-hole filling application. The composition of the inorganics used was 225 g/L copper sulfate pentahydrate, 40 g/L of sulfuric acid and 50 mg/L of Cl. The organic components in the bath are 10 ml/L THF Carrier, 0.4 ml/L THF Leveler and 0.5 ml/L THF Brightener.

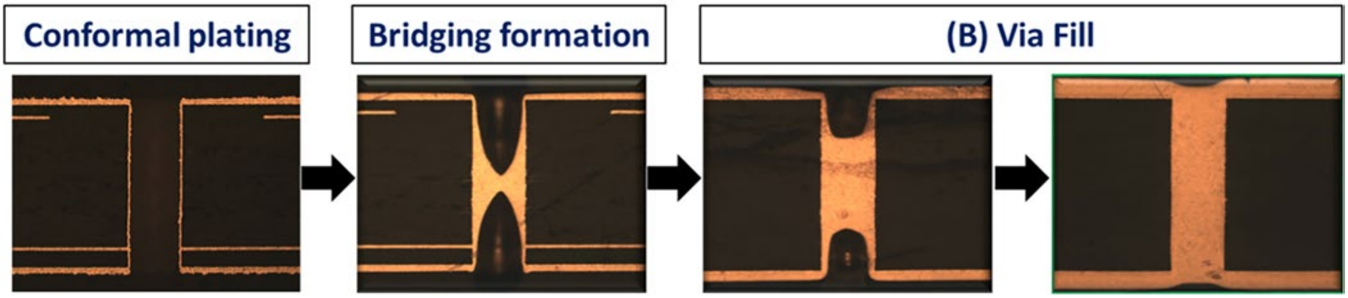


Figure 1: Various stages of through-hole fill plating: Conformal, bridge formation, and subsequent via fill to fill the entire through-hole in 250 µm diameter x 800 µm thick panel.

Figure 1 shows the various stages of the through-hole fill process in 250 µm diameter x 800 µm thick panel. The plating starts out conformal followed by bridging and filling the vias formed after bridging. The bridge formation is achieved by using a PPR waveform and the subsequent via fill is achieved using DC plating. Bridging and via fill time are optimized for the specific through-hole dimension and panel thickness.

One Bath, One Step Technology

Bridging and filling the through-holes is achieved by using PPR and DC plating all in one plating bath. Bridging in the through-holes is achieved by using phase shift PPR. Phase shift waveforms are generated by applying the same waveform on either side of the plating panel but are offset by a certain degree. The complex waveforms are generated by advanced rectifiers which are commercially available. The phase shift waveforms are also referred to as asynchronous waveforms. These waveforms enable selective plating at the center of the through-holes, thereby bridging the center. After bridging, the plating mode is switched to DC plating for filling the vias formed after bridging. The time for bridging and filling depends on the specific through-hole diameter and panel thickness.

The waveform for bridging included a long DC step followed by a pulse train. The entire sequence of this DC step is followed by a pulse train which is repeated for a specific period to achieve bridging in the specific through-hole as shown in Figure 2. The pulse parameters for

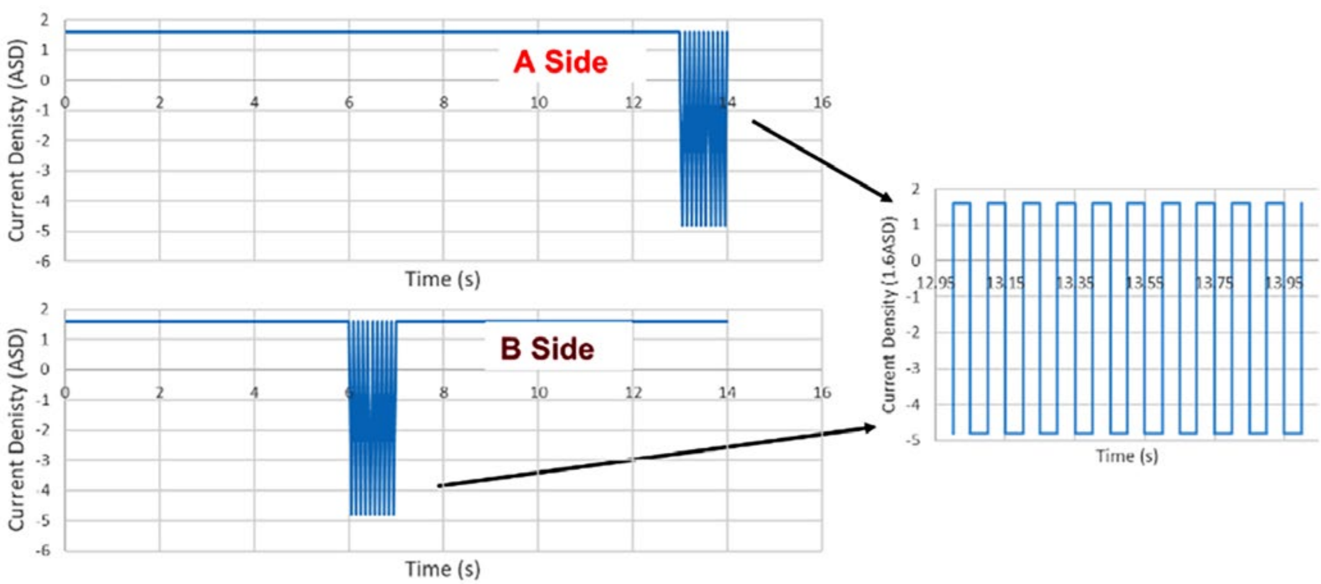


Figure 2: Phase shift waveform used for bridging the through-holes.

Waveform Parameters	Range	Preferred
Long DC Current	≤ 2.5 ASD	≤ 1.5 ASD
Long DC time	≤ 19 s	≤ 13 s
Pulse Forward Current :	≤ 2.5 ASD	≤ 1.5 ASD
Forward time:	≤ 150 ms	≤ 50 ms
Pulse Reverse Current :	≤ 13.5 ASD	≤ 4.5 ASD
Reverse time:	≤ 150 ms	≤ 50 ms
Phase Shift	180°	

Table 1: Phase shift pulse plating parameters for bridging the through-holes.

bridging are shown in Table 1. The long DC step includes plating at 15 ASF for 13 seconds. The pulse train consists of 50 ms for forward and reverse time with forward-to-reverse current ratio of 1:3 at 15 ASF. This pulse train is executed for a total time of 1 second.

Various factors can affect bridging, which is a critical step in the through-hole fill process and are listed below.

Effect of solution flow rate in bridging

Plating experiments were carried out using the waveform listed in Table 1 as a function of solution flow-rate. The plating tank is equipped with impingement flow across the panel surface. The solution flow-rate was varied from 8 L/minute to 24 L/minute during the bridging step and the cross-section results are shown in Figure 3. Good bridging is seen between 12–24 L/minute. Very low or high flow resulted in loss of bridging.

Function of phase shift degree in bridging

Plating was carried out using the waveform listed in Table 1 as a function of phase shift degree. The phase shift degree was varied from 25 to 180. As the phase shift was varied from 180 to 50 degrees, the bridging location shifted away from the center in the 150 and 250 µm diameter through-holes (Figure 4). No bridging is seen in the 250 µm diameter through-holes at lower phase shift degree.

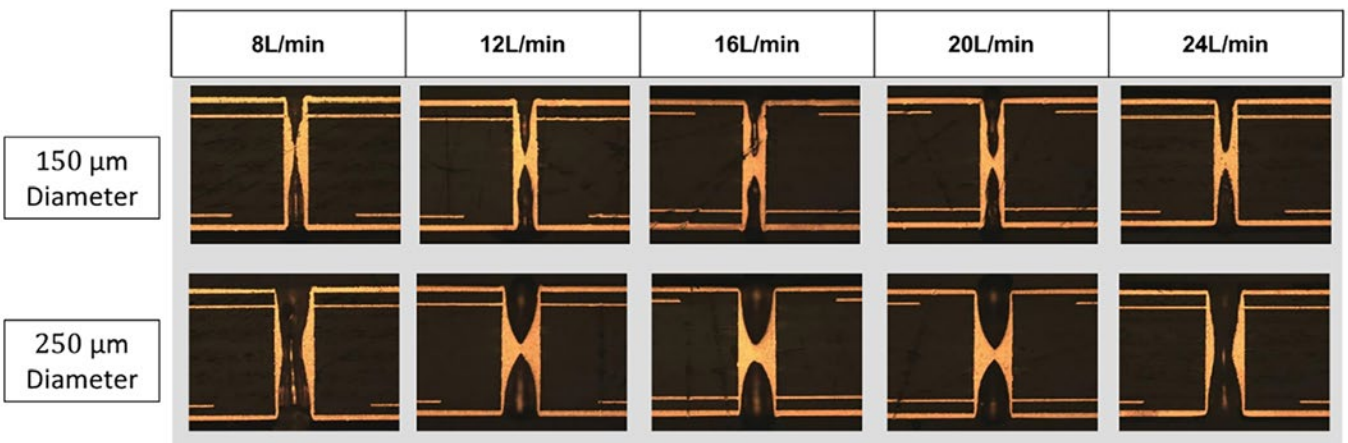


Figure 3: Bridging in 150 and 250 µm diameter through-holes as a function of solution flow rate.

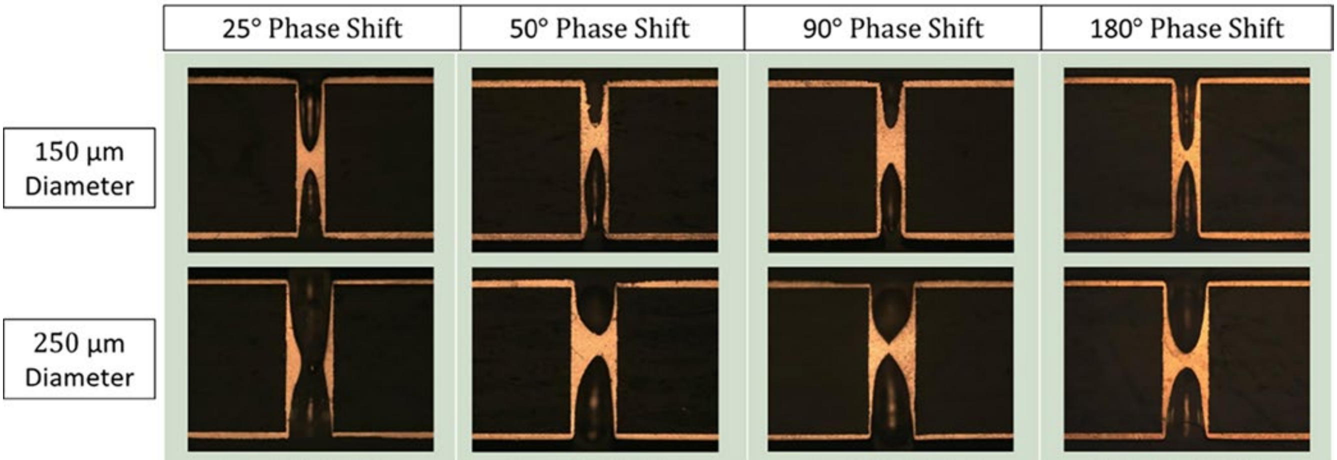


Figure 4: Bridging in 150 and 250 µm diameter through-holes as a function of phase shift degree.

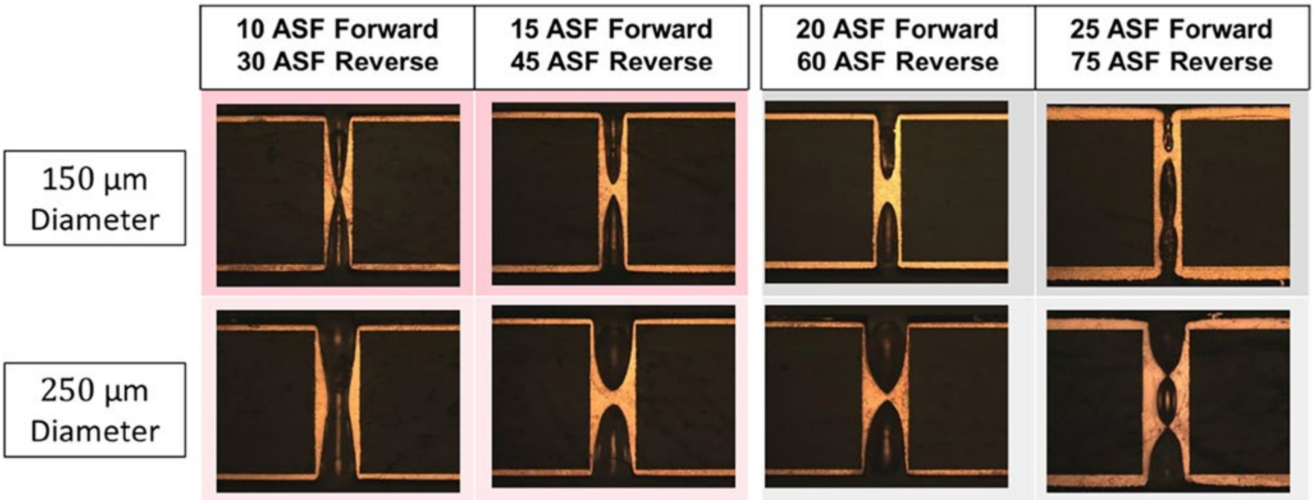


Figure 5: Bridging in 150 and 250 µm diameter through-holes as a function of current density.

Function of current density in bridging

Plating experiments were carried out at 10, 15, 20 and 25 ASF to see the impact on bridge formation (Figure 5). Plating at 15 and 20 ASF gave good bridging in the 150 and 200 µm diameter through-holes. Plating at the lower current density of 10 ASF showed no bridging in the through-holes while plating at the higher current density of 25 ASF showed pinching at different points leading to void formation.

Filling Copper in Mechanically Drilled Through-holes

The through-hole fill process of bridging and filling the through-holes was applied to a wide range of panel thicknesses and hole diameters. Mechanically drilled panels with electroless seed layer were used for evaluation.

250 µm thick core with 150 and 200 µm diameter through-holes

Mechanically drilled panels 250 µm thick by 150 and 200µm diameter were used for evaluation. For 150 µm diameter through-holes, the plating was carried out for a total time of 182 minutes, while the bridging was carried out for 38 minutes and fill was done for 144 minutes. The bridging was performed for 9 µm and fill was carried out for 34 µm for a total surface copper thickness of 43 µm. The 200 µm diameter through-holes were filled for a total surface

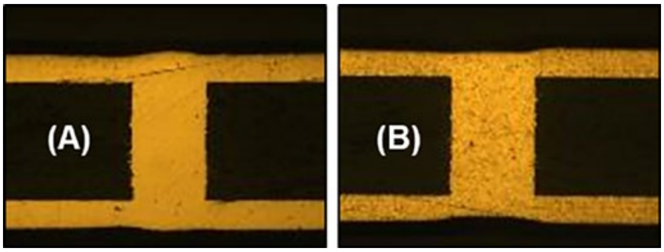


Figure 6: 250 µm thick panel: (A) 150 µm and (B) 200 µm diameter through-holes.

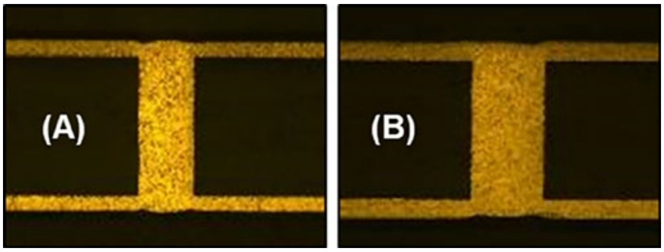


Figure 7: 400 µm thick panel: (A) 150 µm and (B) 200 µm diameter through-holes.

copper thickness of 43 µm. Void-free fill was achieved in the through-holes as shown in the cross-section picture (Figure 6) and confirmed by X-ray analysis.

400 µm thick core with 150 and 200 µm diameter through-holes

Mechanically drilled panels 400 µm thick by 150 and 200 µm diameter were used for evaluation. For 150 µm diameter through-holes, the plating was carried out for a total time of 174 minutes while the bridging was carried out for 38 minutes and fill was performed for 136 minutes. The bridging was carried out for 9 µm and fill for 23 µm with a resulting total surface copper thickness of 32 µm. 200 µm diameter through-holes were filled for a total surface copper thickness of 45 µm. Void-free fill was achieved in the through-holes as shown in the cross-section picture (Figure 7) and confirmed by X-ray analysis.

800 µm thick core with 150 and 200 µm diameter through-holes

Mechanically drilled panels 800 µm thick by 150 and 200 µm diameter were used for evaluation. For 150 µm diameter through-holes, the plating was carried out for a total time of 331 minutes while the bridging was carried out for 43 minutes and fill was performed for 288 minutes. The bridging was carried out for 10 µm and fill for 25 µm with a resulting total surface copper thickness of 35 µm. 200 µm diameter through-holes were filled for a total surface copper thickness of 67 µm. Void-free fill was achieved in the through-holes as shown in the cross-section picture (Figure 8) and confirmed by X-ray analysis.

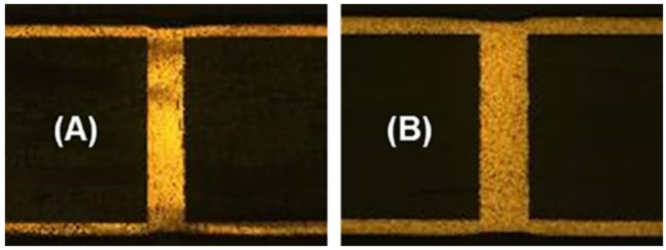


Figure 8: 800 µm thick panel: (A) 150 µm and (B) 200 µm diameter through-holes.

Process Capability

The process of bridging and filling the through-holes using phase shift pulse plating and DC plating can be applied to a wide range of panel thicknesses and through-hole diameters. The time for bridging and filling were optimized to achieve void-free fill for a given through-hole diameter and panel thickness. The cross-section images of through-holes of various dimensions and the surface thicknesses required to fill them are given in Figure 9.

X-Ray Void Evaluation

All the plated coupons were evaluated by X-ray analysis to confirm that void-free fill was achieved in the through-holes. The X-ray image for 400 µm thick and 200 µm diameter through-holes is shown in Figure 10. Void-free fill was seen in the through-holes. The coupons were then cross-sectioned and evaluated with a microscope to take other measurements such as surface thickness.

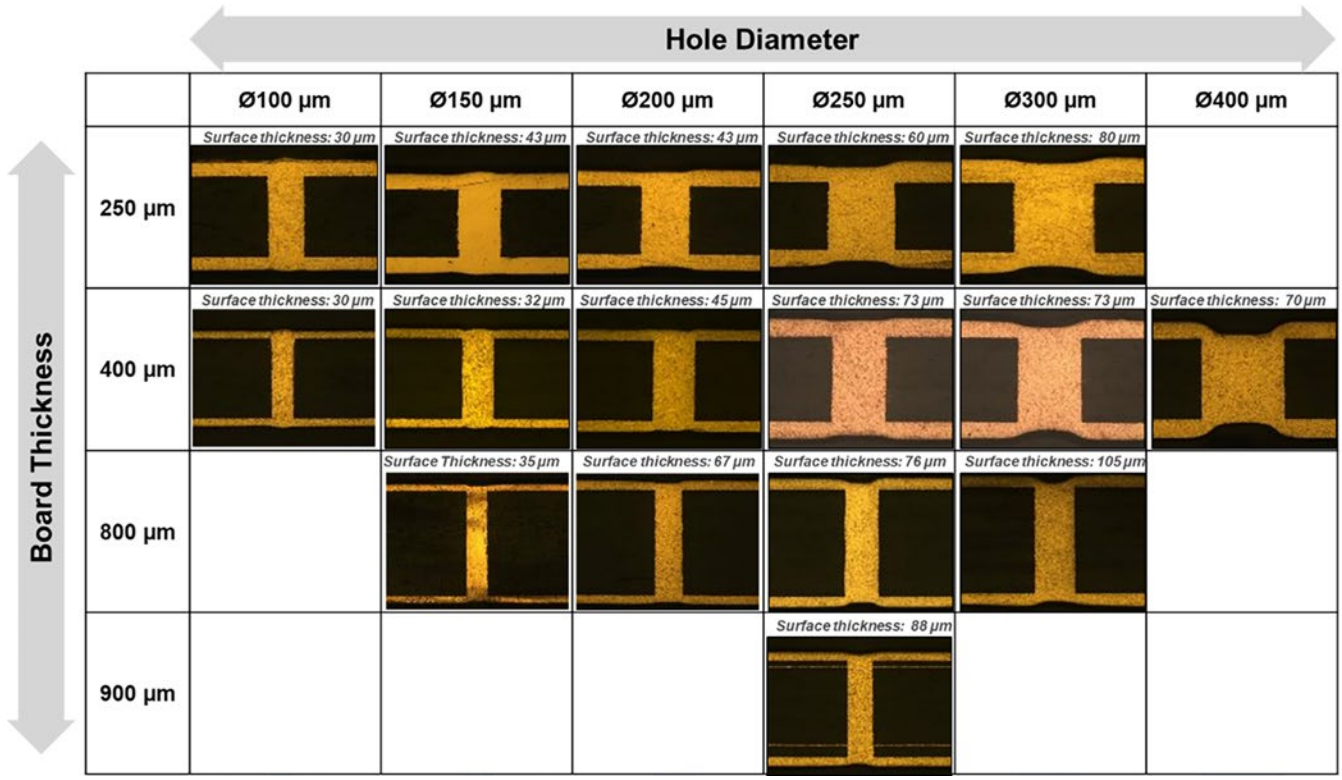


Figure 9: Process capability: Filling a wide range of through-hole diameters and panel thicknesses.

Filling Copper in Laser Drilled Through-holes

Complete void-free fill was not only achieved in the mechanically drilled through-holes but also in laser drilled through-holes. 200 µm thick laser drilled panels with electroless seed layer were used for evaluation.

200 µm thick core with 100 µm diameter through-holes

The laser drilled panels used for evaluation had 200 µm thick electroless seed layer. The diameter of the through-holes was 90–100 µm at the top and bottom while the center was 55–65 µm. The plating was carried out for a total time of 78 minutes with the time for bridging at 16 minutes and that for filling at 62 minutes. The bridging was performed for 5 µm and fill was carried out for 20 µm. Void-free fill was achieved in the through-holes as shown in the cross-section picture (Figure 11).

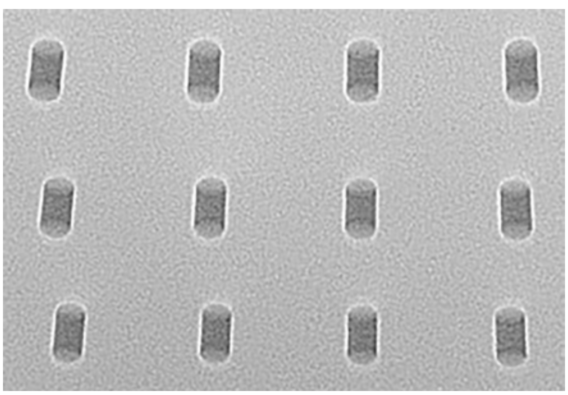


Figure 10: X-Ray image of 400 µm thick x 200 µm diameter through-holes.

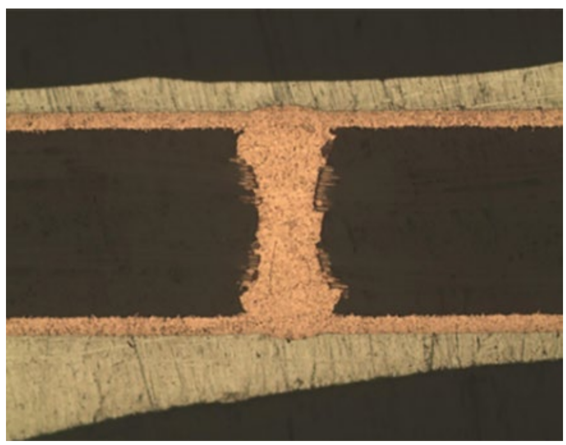


Figure 11. 200 µm thick panel: 90–100 µm diameter filled through-hole.

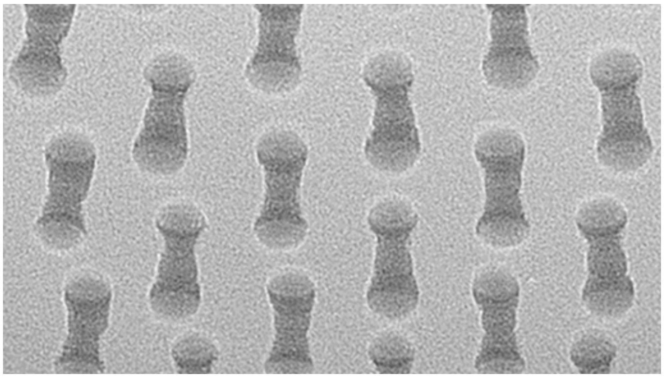


Figure 12: Void-free fill as seen in X-ray image of filled laser-drilled through-holes.

X-ray Void Evaluation

X-ray analysis was performed on the plated laser-drilled panels to confirm void-free fill performance in the through-holes. The X-ray image for 200 µm thick and 90–100 µm diameter through-holes is shown in Figure 12. Void-free fill was seen in the through-holes.

Conclusion

Through-hole fill process for filling mechanically-drilled and laser-drilled through-holes spanning a wide range of through-hole diameters and panel thicknesses was demonstrated. The plating was carried out by a one bath/one step process where bridging is achieved using a phase-shift pulse waveform followed by filling the via formed using DC. This process of filling the through-holes in one bath rather than two offers significant benefits to fabricators in the form of increased throughput and easier maintenance of the plating bath. Void-free fill was achieved in the through-holes as confirmed by X-ray analysis. **PCB007**

Acknowledgements

This work was performed in collaboration with our DuPont Interconnect Solutions colleagues in North America, Asia, and Europe. We sincerely thank them for their help and support.

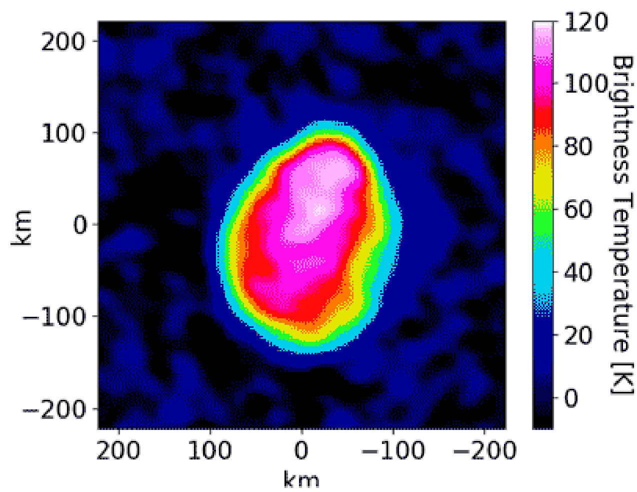
Observatory in Chile Takes Highest-Resolution Measurements of Asteroid Surface Temperatures Ever Obtained From Earth

Psyche orbits the sun in the asteroid belt, a donut-shaped region of space between Earth and Jupiter that contains more than a million rocky bodies that range in size from 10 meters to 946 kilometers in diameter.

With a diameter of more than 200 km, Psyche is the largest of the M-Type asteroids, an enigmatic class of asteroids that are thought to be metal rich and therefore potentially may be fragments of the cores of proto-planets that broke up as the solar system formed.

Studying such relatively tiny objects that are so far away from Earth (Psyche drifts at a distance that ranges between 179.5 and 329 million km from Earth) poses a significant challenge to planetary scientists, which is why NASA plans to send a probe to Psyche to examine it up close. Typically, thermal observations from Earth—which measure the light emitted by an object itself rather than light from the sun reflected off of that object—are in infrared wavelengths and can produce only 1-pixel images of asteroids. That one pixel does, however, reveal a lot of information; for example, it can be used to study the asteroid's thermal inertia, or how fast it heats up in sunlight and cools down in darkness.

(Source: Caltech)



Millimeter-wavelength emissions reveal the temperature of the asteroid Psyche as it rotates through space.

Editor Picks from PCB007

1 EIPC Technical Snapshot: Thinking Differently in a Post-Pandemic World ▶


Alun Morgan

President Alun Morgan introduced the 10th in the enormously popular series of EIPC's monthly Technical Snapshots. He said that although previous webinars had been directed at specific technical issues, the focus of the present session had been expanded to include a good measure of business content to provide better understanding of how it had developed during the pandemic.

2 Additive Reality: Drops of Technology ▶

The solder mask application revolves around solder mask material. The inkjet printed solder mask layer will be made of a collection of drops and next to the solder mask ink a few other materials play a role in the shaping of these drops.

3 Hire or Be Hired at jobConnect007 ▶

On July 2, 2021, I-Connect007 released the inaugural issue of jobConnect007, a monthly guide to job openings in the printed circuit board/electronics manufacturing industry. Sign up here to receive your copy, updated and sent monthly.

4 Catching Up With Archer Circuits' Echo Yang ▶


Echo Yang

I was thrilled when Echo Yang called to talk about her company, Archer Circuits. Echo is a 37-year-old woman who started her own trading company. She is well-educated, well-trained, and well-spoken; she is filled with ambition and passion for what she does. You are going to find her story and the story of her company as interesting as I have.

5 Feeling the Supply Chain Squeeze ▶

Nolan Johnson speaks with Joe D'Ambrisi of MacDermid Alpha to gain insight into what he's seeing in the market from his perspective as a specialty chemicals and materials provider.

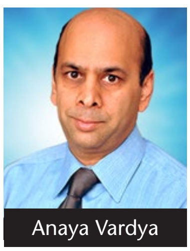

Joe D'Ambrisi

6 Schweizer Achieves Successful IATF Certification of the Jintan Plant ▶

More than a year ago, production was launched at Schweizer's new high-tech plant in Jintan, China. Another important milestone for the plant in China, but also for the global orientation of the company, has now been achieved with successful IATF 16949:2016 certification.

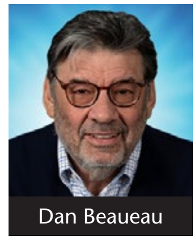
7 Standard of Excellence: The Beauty of a Partnership ▶

Partnerships are more important than ever. Not only with your vendors, as we regularly focus on in this column, but with your competitors as well. I believe that if we can all start working together in this new post-pandemic world, life will be much better for all of us individually but also better for our industry as a whole.


Anaya Vardya

8 Dan's Biz Bookshelf: Go Live! Turn Virtual Connections into Paying Customers ▶

If one thing has become clear during the pandemic, it's that more people are using social media to communicate. Use that to your advantage in your business. Dan reviews helpful tips from this book by Jeffrey Gitomer.

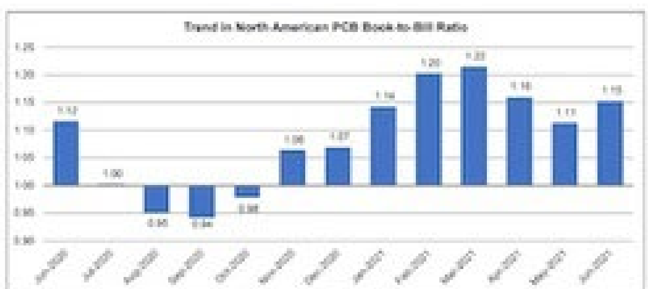

Dan Beaueau

9 AT&S Technology Enables the World's Smallest Digicam ▶

The image sensor is smaller than a grain of rice, lighter than a postage stamp but more powerful than any previous development of its kind.

10 North American PCB Industry Sales Up 6.3% in June ▶

IPC announced the June 2021 findings from its North American Printed Circuit Board Statistical Program. The book-to-bill ratio stands at 1.15.



Career Opportunities

Application Engineer (m/f/d)—Fulltime, Germany

Our company is expanding its product portfolio into custom made products. This creates the need for an Application Engineer to provide technical support to our existing sales team and customer base.

Responsibilities:

- Analysis of incoming technical data and handling of engineering questions
- Technical consultation of customers (incl. new customer specifications and discuss with relevant technical and quality teams worldwide)
- Support and consultation for new projects
- Lead and/or participate in local, cross-location/global cross-department projects of various scale
- Develop and provide function-related trainings to existing and new staff in order to transfer and optimize know-how
- Provide technical solutions

Skills:

- Technical expertise in battery power solutions and technologies for Rechargeable and Primary cells and Battery Packs
- Mechanical background or knowledge to be able to discuss and manage other products, like custom made connectors, cable assemblies and keypad touch panels.
- Written and spoken English and German, any other European language a plus.
- Highly technical with a commercial flare.
- Self-motivated, ambitious, and eager to grow in a dynamic organization.

Interested? We are looking forward to your application!

Please send your application to **hr@cmit.support**. For any inquiries, please contact Mrs. Amélie Filler. For more information visit www.cml-globalsolutions.com

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Sales Manager (m/f/d)—Worldwide Locations

CML Group is a leading provider of Printed Circuit Boards. We develop tailor-made sourcing concepts for our customers worldwide creating strong partnerships and reliable connections.

For the expansion of our target markets, we need you to generate new business, drive new projects from RFQ stage and manage the customer relationship.

Your Profile:

- Profound sales and technical expertise in printed circuit board industry
- Local market knowledge and ideally a customer base of contacts in one or more of the listed countries
- Have successful track records in developing new business opportunities
- Excellent command in spoken and written English and one additional local language
- Highly self-motivated, ambitious, eager to grow in a dynamic organization
- Able to work independently and have good communication skills and leadership skills
- Self-employed/contractor/commission-based agent also welcome

Your Target Markets:

- Europe: Spain, France, Germany, Netherlands, UK, Denmark, Sweden, Norway
- USA: New Jersey, Florida, Georgia, Michigan, San Jose, Bay area, Pacific Northwest and Canada
- Others: Singapore, Thailand, Malaysia, Australia, Brazil, Turkey, Russia, and South Africa

Interested? We are looking forward to your application!

Please send your application to **hr-china@cml-eurasia.hk**. For any inquiries, please contact Ms. Grace Feng. For more information visit www.cml-globalsolutions.com

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Career Opportunities

ICAPE GROUP

PCB Field Engineer–North America Operations

ICAPE Group is a European leader for printed circuits boards and custom-made electro-mechanical parts. Headquartered in Paris, France, we have over 500 employees located in more than 70 countries serving our +2500 customers.

To support our growth in the American market, we are looking for a PCB Field Engineer.

You will work in our North America technical center, including our U.S. technical laboratory, and will be responsible for providing technical and quality support to our American sales team.

You will have direct customer contact during all phases of the sales process and provide follow-on support as required.

RESPONSIBILITIES INCLUDE

- Feasibility recommendations
- Fabricator questions and liaison
- Quality resolutions
- Technical explanation (for the customer) of proposals, laboratory analysis or technology challenges

REQUIREMENTS

- Engineering degree or equivalent industry experience
- 5 years' experience with PCB manufacturing (including CAM)
- Excellent technical understanding of PCBs
- Experience with quality tools (FAI, PPAP and 8-D)
- Good communication skills (written and oral)

Communication skills are essential to assist the customer with navigation of the complex process of matching the PCB to the application.

SALARY

Competitive, based on profile and experience. Position is full time in Indianapolis, Ind.

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Prototron Circuits

Sales Representatives

Prototron Circuits, a market-leading, quick-turn PCB shop, is looking for sales representatives for all territories.

Reasons you should work with Prototron:

- Serving the PCB industry for over 30 years
- Solid reputation for on-time delivery (99% on-time)
- Excellent quality
- Production quality quick-turn services in as little as 24 hours
- AS9100
- MIL-PRF- 31032
- ITAR
- Global sourcing
- Engineering consultation
- Completely customer focused team

Interested? Let's have a talk.
Call Dan Beaulieu at
207-649-0879
or email to
danbbeaulieu@aol.com

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Career Opportunities

The Test Connection, Inc.

Rewarding Careers

Take advantage of the opportunities we are offering for careers with a growing test engineering firm. We currently have several openings at every stage of our operation.

The Test Connection, Inc. is a test engineering firm. We are family owned and operated with solid growth goals and strategies. We have an established workforce with seasoned professionals who are committed to meeting the demands of high-quality, low-cost and fast delivery.

TTCI is an Equal Opportunity Employer. We offer careers that include skills-based compensation. We are always looking for talented, experienced test engineers, test technicians, quote technicians, electronics interns, and front office staff to further our customer-oriented mission.

Associate Electronics Technician/ Engineer (ATE-MD)

TTCI is adding electronics technician/engineer to our team for production test support.

- Candidates would operate the test systems and inspect circuit card assemblies (CCA) and will work under the direction of engineering staff, following established procedures to accomplish assigned tasks.
- Test, troubleshoot, repair, and modify developmental and production electronics.
- Working knowledge of theories of electronics, electrical circuitry, engineering mathematics, electronic and electrical testing desired.
- Advancement opportunities available.
- Must be a US citizen or resident.

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Test Engineer (TE-MD)

In this role, you will specialize in the development of in-circuit test (ICT) sets for Keysight 3070 (formerly HP) and/or Teradyne (formerly GenRad) TestStation/228X test systems.

- Candidates must have at least three years of experience with in-circuit test equipment. A candidate would develop and debug our test systems and install in-circuit test sets remotely online or at customer’s manufacturing locations nationwide.
- Candidates would also help support production testing and implement Engineering Change Orders and program enhancements, library model generation, perform testing and failure analysis of assembled boards, and other related tasks.
- Some travel required and these positions are available in the Hunt Valley, Md., office.

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Sr. Test Engineer (STE-MD)

- Candidate would specialize in the development of in-circuit test (ICT) sets for Keysight 3070 (formerly Agilent & HP), Teradyne/ GenRad, and Flying Probe test systems.
- Strong candidates will have more than five years of experience with in-circuit test equipment. Some experience with flying probe test equipment is preferred. A candidate would develop, and debug on our test systems and install in-circuit test sets remotely online or at customer’s manufacturing locations nationwide.
- Proficient working knowledge of Flash/ISP programming, MAC Address and Boundary Scan required. The candidate would also help support production testing implementing Engineering Change Orders and program enhancements, library model generation, perform testing and failure analysis of assembled boards, and other related tasks. An understanding of stand-alone boundary scan and flying probe desired.
- Some travel required. Positions are available in the Hunt Valley, Md., office.

Contact us today to learn about the rewarding careers we are offering. Please email resumes with a short message describing your relevant experience and any questions to careers@ttci.com. Please, no phone calls.

We proudly serve customers nationwide and around the world.

TTCI is an ITAR registered and JCP DD2345 certified company that is NIST 800-171 compliant.

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Career Opportunities

ARLON ELECTRONIC MATERIALS

Arlon EMD, located in Rancho Cucamonga, California, is currently interviewing candidates for open positions in:

- **Engineering**
- **Quality**
- **Various Manufacturing**

All interested candidates should contact Arlon's HR department at 909-987-9533 or email resumes to careers.ranch@arlonemd.com.

Arlon is a major manufacturer of specialty high-performance laminate and prepreg materials for use in a wide variety of printed circuit board applications. Arlon specializes in thermoset resin technology, including polyimide, high Tg multifunctional epoxy, and low loss thermoset laminate and prepreg systems. These resin systems are available on a variety of substrates, including woven glass and non-woven aramid. Typical applications for these materials include advanced commercial and military electronics such as avionics, semiconductor testing, heat sink bonding, High Density Interconnect (HDI) and microvia PCBs (i.e. in mobile communication products).

Our facility employs state of the art production equipment engineered to provide cost-effective and flexible manufacturing capacity allowing us to respond quickly to customer requirements while meeting the most stringent quality and tolerance demands. Our manufacturing site is ISO 9001: 2015 registered, and through rigorous quality control practices and commitment to continual improvement, we are dedicated to meeting and exceeding our customers' requirements.

For additional information please visit our website at www.arlonemd.com

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KOH YOUNG TECHNOLOGY

Logistics Assistant

Koh Young America is looking for a Logistics Assistant to assist and oversee our supply chain operations. Working alongside a Logistics Specialist, you will coordinate processes to ensure smooth operations using a variety of channels to maximize efficiency. You must be an excellent communicator and negotiator well-versed in supply chain management principles and practices. Also, you should be meticulous with a focus on customer satisfaction. These attributes are ideally complemented by a Bachelor's in Supply Chain Management or equivalent professional experience in the manufacturing industry.

This position is in our Duluth, Georgia, headquarters, where we serve our customers within North and South America. We offer health, dental, vision, and life Insurance with no employee premiums, including dependent coverage. Additionally, we provide a 401K retirement plan with company matching, plus a generous PTO policy with paid holidays.

Koh Young Technology, founded in 2002 in Seoul, South Korea, is the world leader in 3D measurement and inspection technology used in the production of micro-electronics assemblies. Using patented 3D technology, Koh Young provides best-in-class products in Solder Paste Inspection (SPI) and Automated Optical Inspection (AOI) for electronics manufacturers worldwide.

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Maintenance Technician

Inspects work-related conditions to determine compliance with prescribed operating and safety standards. Operates power-driven machinery and uses equipment and tools commonly used to maintain facilities and equipment. Replace filters, belts, and additional parts for repairs and preventive maintenance. Moves objects weighing up to 150 lbs. using a hand truck or pulley. Cleans work area and equipment. Works with cleaning fluids, agents, chemicals, and paints using protective gear. Works at elevations greater than ten feet, climbing ladders, while repairing or maintaining building structures and equipment. Assists skilled maintenance technicians/workers in more complex tasks and possible after-hours emergency repairs. Must meet scheduling and attendance requirements.

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Plating Operator

Plating operator for printed circuit boards. No experience necessary, will train. Must be able to work with chemicals, lift up to 50 pounds, and have good math skills. Minimum high school/GED or equivalent. All shifts (1st, 2nd, 3rd), 8 hours per day minimum, Monday thru Friday. Saturday and Sunday work is common allowing for steady overtime pay.

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Water Treatment Operator

Responsible for operating waste treatment plant, our operation that converts wastewater in drains and sewers into a form that's metal free to release into the environment.

Control equipment and monitor processes that remove metals from wastewater. Run tests to make sure that the processes are working correctly. Keep records of water quality and pH. Operate and maintain the pumps and motors that move water and wastewater through filtration systems. Read meters and gauges to make sure plant equipment is working properly. Take samples and run tests to determine the quality of the water being produced. Adjust the amount of chemicals being added to the water and keep records that document compliance.

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Drilling Operator

Drilling operator for printed circuit boards. Minimum 2 years of experience. Minimum high school/GED or equivalent.

All Shifts (1st, 2nd, 3rd), 8 hours per day minimum, Monday thru Friday. Saturday and Sunday work is common allowing for overtime pay.

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I-Connect007
GOOD FOR THE INDUSTRY

SIEMENS

Marketing Coordinator/Writing Strategist: Embedded Software

Location: Portland, Oregon or USA (remote)
Job Number: 242982

Seeking a technology communications change maker! Siemens Digital Industries Software is looking for a content creator for its embedded software group. The ideal candidate for the Brand Marketing coordinator/writing strategist position will work closely with engineers and managers to write, edit and produce compelling technology marketing content (magazine articles, blogs, technology papers, multi-media, customer success stories and promotional materials). Do you possess creative energy and enjoy storytelling with an energetic team?

Requirements:

- Strong writing and editing skills
- Education and/or experience in technology, science, journalism and/or English
- A technical background or experience (such as a BS or an associate's degree in engineering or computer science) is preferred
- 1-3 years of experience in writing about technology solutions
- Basic knowledge of online publications, digital platforms and social media is useful to meet project specifications in a fast-paced environment
- Ability to research and collect data, repurpose existing materials, collaborate with subject matter experts, and translate technical information into compelling marketing communications content that engage audiences

Creative materials will be used globally, in a high-energy environment, supporting the world's leading industrial software company.

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JOHNS HOPKINS

CAM / Process Engineer

The JHU/APL PCB Fabrication team is seeking a Computer Aided Manufacturing Engineer to support front-end data processing of APL manufactured hardware. You will directly contribute to hardware fabrication in support of National Security, Military Readiness, Space Exploration, National Health, and Research related to fundamental scientific advancement. This position includes a variable mix of core CAM work scope with additional opportunities for hands-on support such as bare board electrical testing, laser drilling, and mechanical CNC drilling and routing.

Responsibilities:

1. Computer Aided Manufacturing for rigid PCB, rigid-flex, and flexible circuits
   a) Perform design checks, panel layout, coupon generation, file generation, stackups
   b) Support manufacturability reviews with internal APL engineers (customers)
   c) Generate work travelers
   d) Communicate status to supervisors and internal customers
2. Support transition of software tools (Genesis 2000 to InCAM Pro)
   a) Edit design rules checks and generate automation scripts
   b) Develop new ideas to further the technical progress of our product
   c) Develop CAM area through continuous improvement initiatives
3. Interface and inform APL Engineers on PCB design for manufacturing guidelines
4. Operate bare board electrical tester
5. Backup operator for CNC drilling, routing, laser drilling (on-site training)

For more details and to apply:
http://www.jhuapl.edu/careers and search for CAM.

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U.S. CIRCUIT

Sales Representatives (Specific Territories)

Escondido-based printed circuit fabricator U.S. Circuit is looking to hire sales representatives in the following territories:

- Florida
- Denver
- Washington
- Los Angeles

Experience:

- Candidates must have previous PCB sales experience.

Compensation:

- 7% commission

Contact Mike Fariba for more information.

mfariba@uscircuit.com

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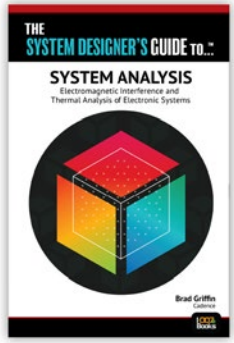
EDUCATIONAL RESOURCE CENTER

Introducing:

The System Designer's Guide to... System Analysis

By Brad Griffin, Cadence

In this latest title from I-007eBooks, readers will learn how system-level analysis of complex and high-speed electronic designs is critical to solve electromagnetic, electrothermal, and electromechanical simulation challenges and to ensure that the system works under wide-ranging operating conditions. **Get your copy now!**

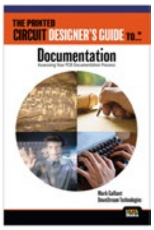


I-007eBooks The Printed Circuit Designer's Guide to...

Thermal Management: A Fabricator's Perspective

by Anaya Vardya, American Standard Circuits

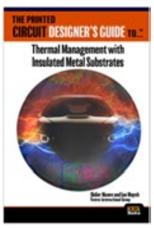
Beat the heat in your designs through thermal management design processes. This book serves as a desk reference on the most current techniques and methods from a PCB fabricator's perspective.



Documentation

by Mark Gallant, Downstream Technologies

When the PCB layout is finished, the designer is still not quite done. The designer's intent must still be communicated to the fabricator through accurate PCB documentation.



Thermal Management with Insulated Metal Substrates

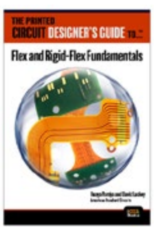
by Didier Mauve and Ian Mayoh, Ventec International Group

Considering thermal issues in the earliest stages of the design process is critical. This book highlights the need to dissipate heat from electronic devices.

Fundamentals of RF/Microwave PCBs

by John Bushie and Anaya Vardya, American Standard Circuits

Today's designers are challenged more than ever with the task of finding the optimal balance between cost and performance when designing radio frequency/microwave PCBs. This micro eBook provides information needed to understand the unique challenges of RF PCBs.



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