I-Connect007
MAY 2021
DESIGN007 MAGAZINE

Design Challenges

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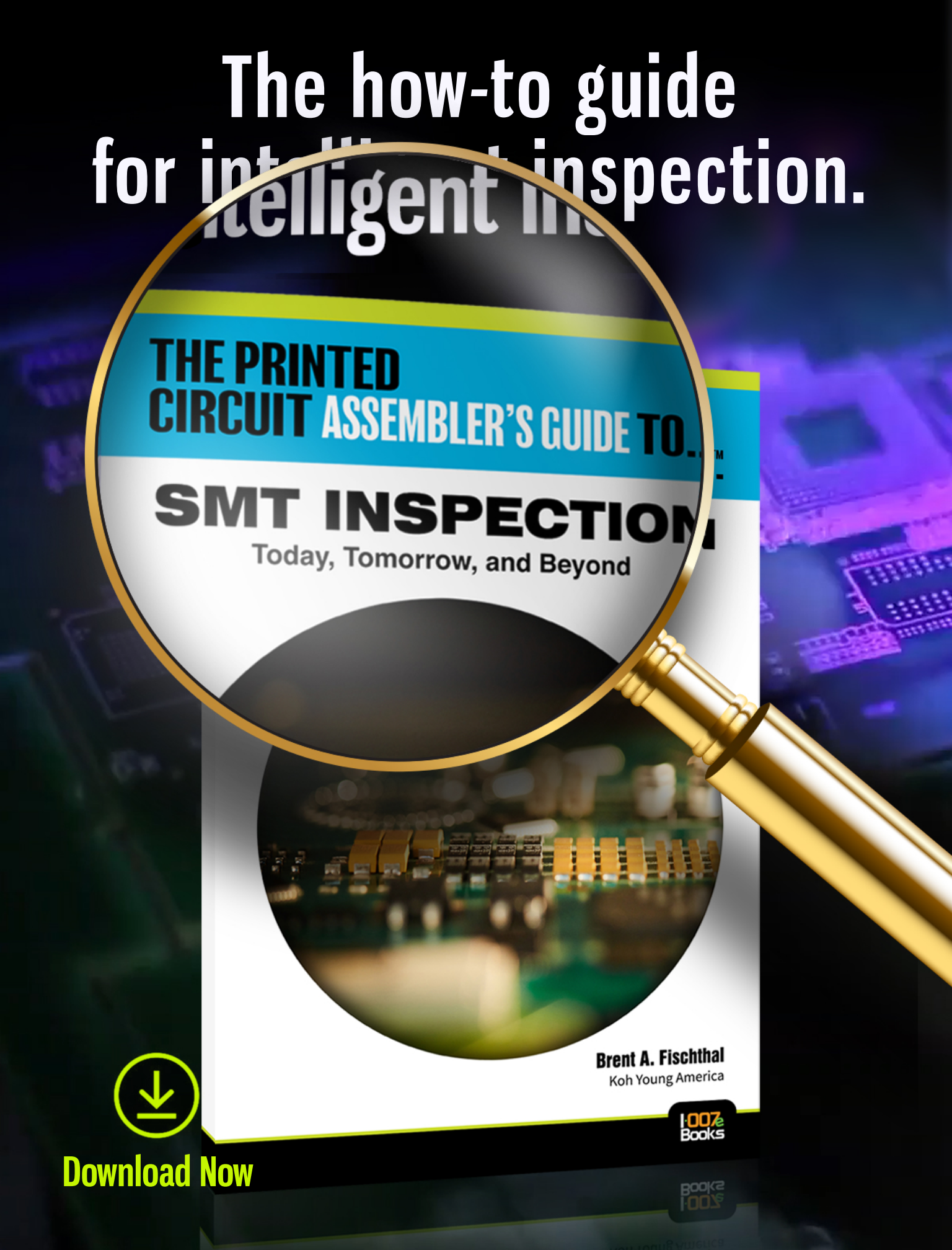
SOLUTION TO PUZZLE ON PAGE 10 ➡

The how-to guide for int[illegible]elligent ins[illegible]pection.



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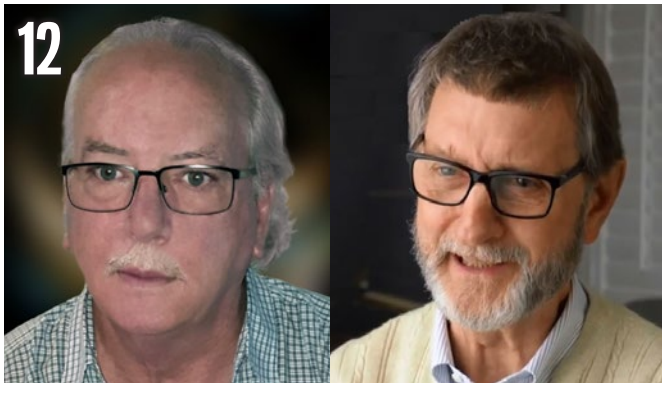
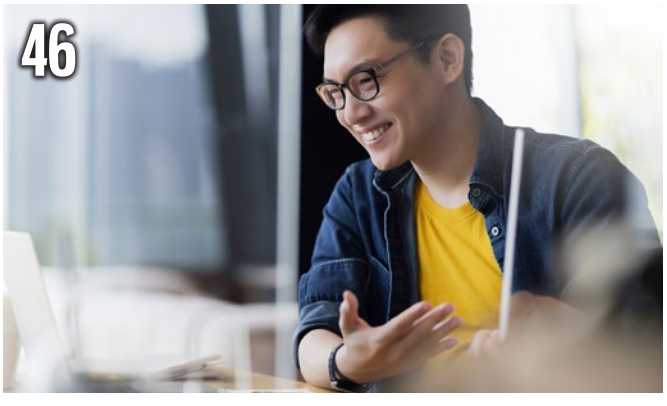
DESIGN007 MAGAZINE

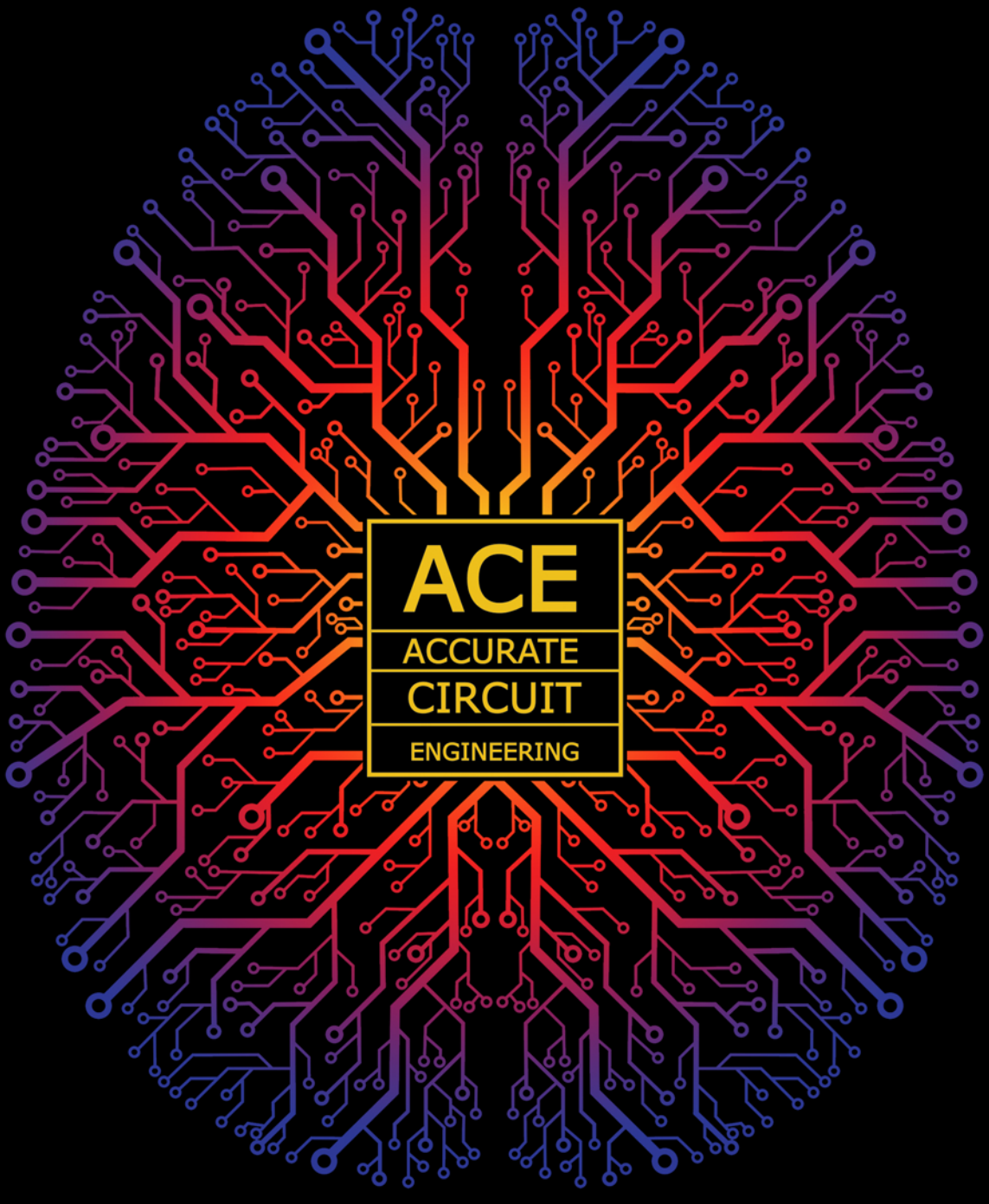
Top Design Challenges

It's safe to say that there is no Number 1 PCB design challenge; it's more like a multiverse of problems, to borrow a term from Marvel's movie franchise. So, this month, we asked a select group of expert designers and design engineers to discuss some of the many ongoing problems that they face with each design.





Don't Overthink Your Prototype Builds



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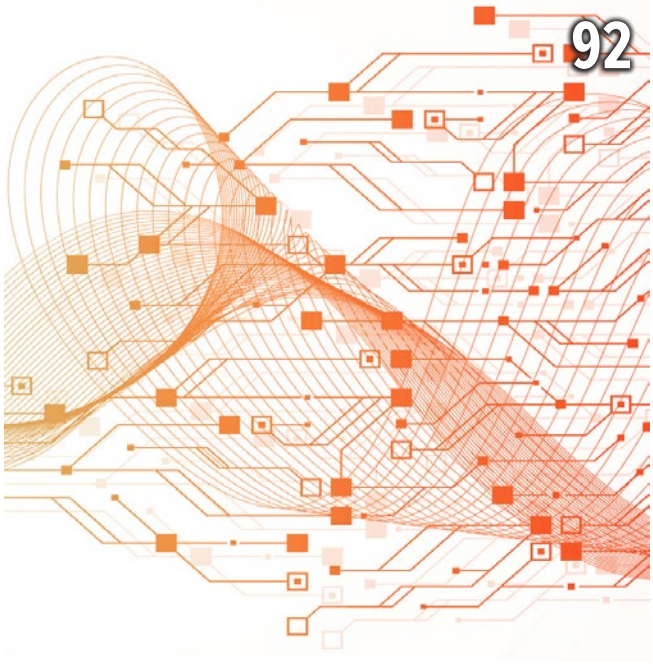
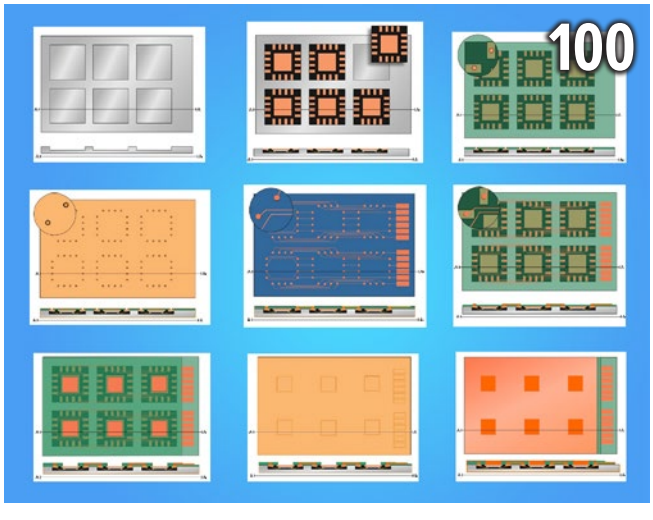
FLEX007

This Month in Flex

The challenges facing rigid board designers pale in comparison to those that their flexible brethren must contend with. Flex designers work their black magic in a dynamic, 3D environment, and almost every design could be considered a custom build. This month, we look into a new process for using copper-filled vias for HDI flex designs.





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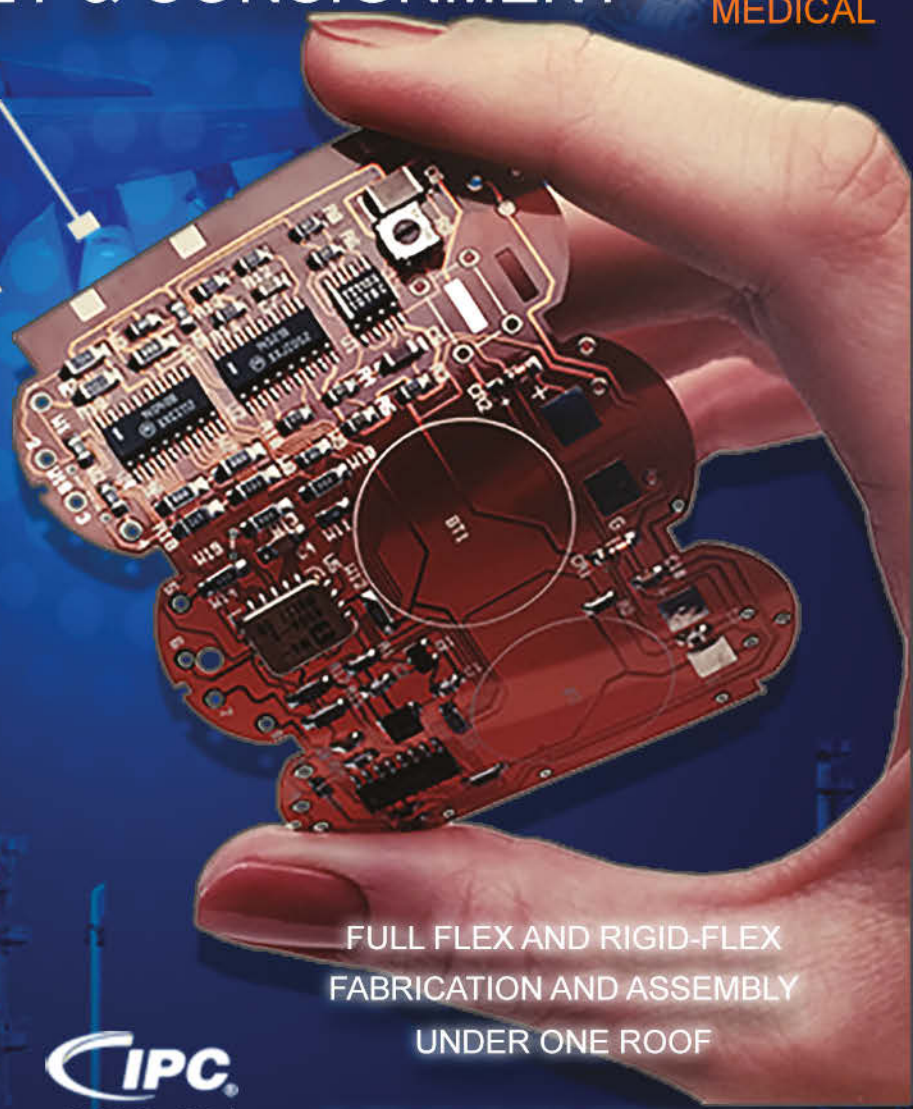

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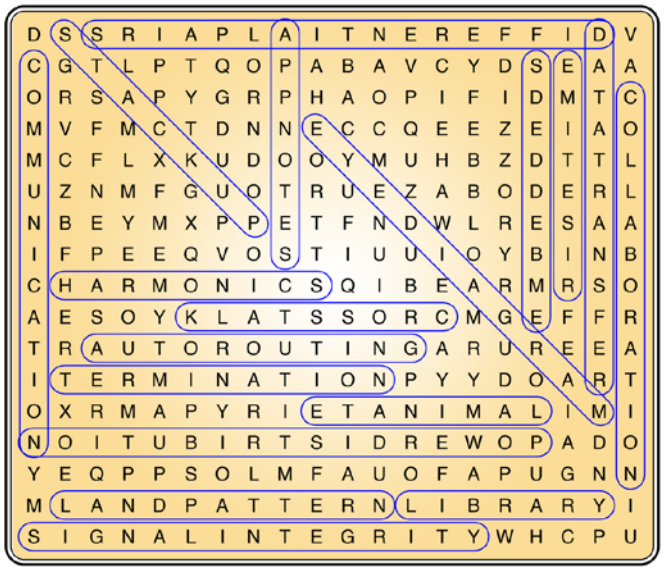
What Are Your Top Design Challenges?

The Shaughnessy Report

by Andy Shaughnessy, I-CONNECT007

When we started planning this month's issue, we decided to survey our readers regarding their most common design challenges. I assumed that, as with previous surveys, I could easily identify the most "popular" challenge and then direct our content toward that topic. I sure was wrong.

We conducted the survey and, low and behold, the readers' responses were all over the map. I had to create an Excel spreadsheet (not my forte) to keep track of all the problems you all run into daily. Dozens of readers reported multiple miscues, missteps, and mishaps, including "simple" board-level issues, DFM, signal integrity, and EMI.



WORD SEARCH PUZZLE SOLUTION

The survey comments were particularly illuminating:

- Engineers don't understand the process required to create a layout that meets everyone's requirements
- Lack of communication between designer and EMS provider
- DFM combined with strict HDI designs
- DDR routing techniques
- How to handle different offshore vendors when they can't get the same material spec on the layer stackup
- EMI and SI
- Component footprint issues, DFM, DFT, DFA, and supply chain management

I think the last response sums it up for most PCB designers: They're typically dealing with more than one challenge simultaneously. And some of these issues are out of the designer's control.

The most concerning aspect about these design challenges is that many of these issues have been bees in the designer's bonnet for decades. These problems are not stopping most designs, but they're naggingly consistent over time.

When I shared these survey results with our contributors, most of them concurred, and then they added several more problems that they contend with on each design project. It was then that I realized this issue was going to be a kind of potpourri of articles—a hodgepodge, if you will—focusing on a variety of PCB design issues.

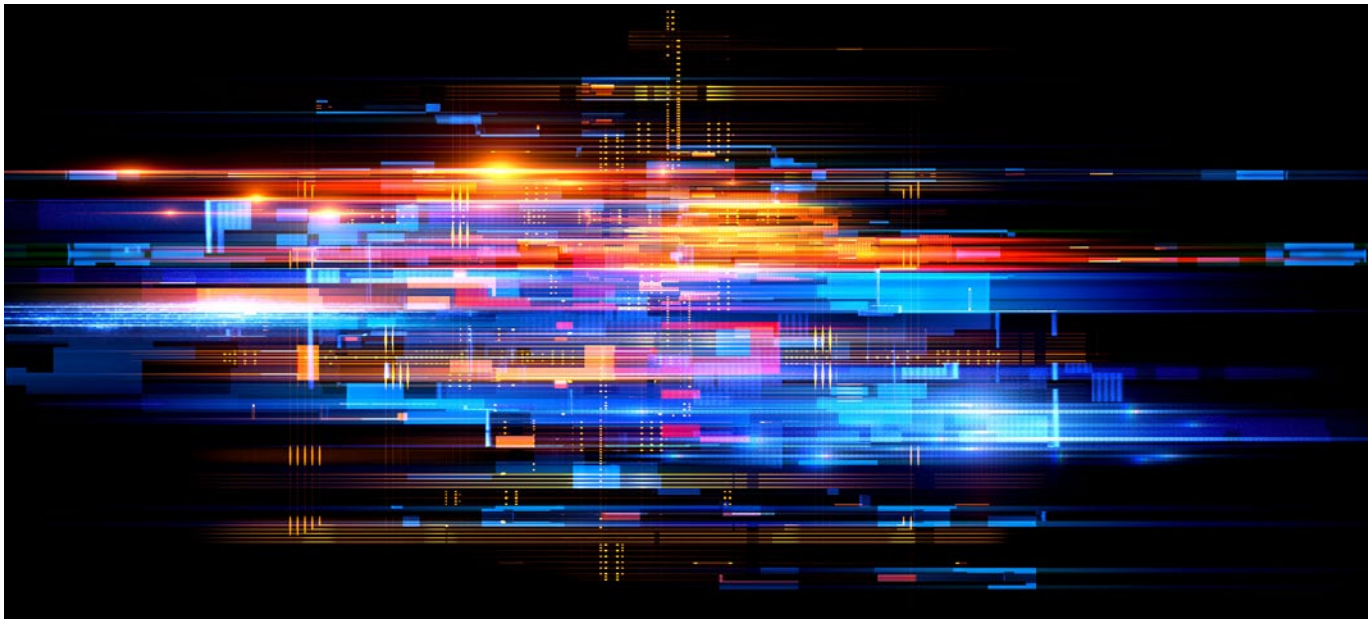
Remember, we're mainly nipping and tucking around the edges here. Overall, today's PCB designers do a fantastic job, often while working with multiple unknowns. The PCB designer is not unlike a maestro conducting an orchestra while blindfolded, or a pilot flying on instruments at midnight. If you're a PCB designer or design engineer, you get to be really good at handling variables. But for many of you, these challenges are what make your job fun in the first place.

Well, if you like challenges, you're in luck! This month, we asked a select group of expert designers and design engineers to discuss some of the ongoing problems they face with each design. We kick off with a conversation about DDR design techniques featuring columnist Barry Olney and consultant Rick Hartley. They cut through the fog surrounding DDR design, and explain why design engineers should get their DDR data straight from JEDEC, not datasheets. Ken Wyatt of Wyatt Technical Services discusses the top five reasons that products fail EMI testing, and how to keep your board from bringing home an F. Next, columnist Mark Thompson details his top six design challenges. Because Mark spent decades in CAM and is now designing PCBs for Monsoon Solutions, he offers a wide perspective.

Then, columnist Chris Young delves deep into design cycle time optimization. If you've ever found yourself running out of time during a design, Chris has a few approaches that may help you stay on schedule. PCEA's Kelly Dack shares his professional journey toward complete understanding of the DFM process, and he offers tips on working with domestic and offshore manufacturing partners. Stephen V. Chavez of Rockwell Collins explains how PCB reuse can stop many design problems before they start. And columnist John Talbot discusses a new via-in-pad technique for high-density flexible circuits; this process fills flex vias with a special kind of copper plating. We also bring you an article from Siemens EDA that explains the new PCBflow online DFM environment, along with plenty of columns from our regular contributors.

It's hard to believe it's May already. Where does the time go? Until next month, take care! **DESIGN007**

Andy Shaughnessy is managing editor of *Design007 Magazine.* He has been covering PCB design for 20 years. He can be reached by clicking here.



PCB Design Challenges: Designing With DDR

Feature Interview The I-Connect007 Editorial Team

Longtime signal integrity experts Rick Hartley and Barry Olney join the I-Connect007 Editorial Team for a discussion around DDR and the complications board designers inevitably face when they design for DDR. If, as Rick and Barry explain, the DDR design process is not that much more complicated than that of a typical high-speed board, why does DDR cause design engineers so much grief? Much of this comes down to following the process, running simulation, and not relying on reference designs.

Andy Shaughnessy: I thought maybe one of you could explain why DDR is used so often. What is the advantage of using DDR?

Barry Olney: It's the fastest technology we have for memory. With each new version there is a dramatic increase in device data rates and bandwidth; for instance, DDR4 has a maximum data rate of 3200 MT/s whereas DDR5 peaks at 6400 MT/s.

Rick Hartley: I have not used DDR5, but it's not just double data right now; it's quadruple data.

Olney: Yes, DDR5 has only recently come out. A few of the chip manufacturers in Taiwan have it, but I have not seen it myself yet, so I'm looking forward to it.

Shaughnessy: What does this look like? What does this entail? When someone says, "We've got a design for this DDR," what are we talking about? Is this a physical thing?

Hartley: Like any bus technology it has data, address, clocks, control lines, it has all the things that most bus technologies have. It's source-synchronous clocking, meaning that the clock is launched with signals so you're not launching a clock and then depending on the signals to arrive at the receiver within a given timeframe. You launch all of them together and if all the data, for example, is set up within a certain timeframe relative to the clock/strobe, everything functions as it should. And the same is true for the clocks of the address. It is source-synchronous, which makes it a much, I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Barry Olney

think, easier technology to use. What are your thoughts, Barry?

Olney: It is easier to use. Especially with the DDR3, DDR4, and DDR5, now you have the write leveling which synchronizes the clocks to the address, command, and control lines. You must realize that with DDR, there are two sets of clocks. There is the main clock of the two, and there are also the strobes that trigger the data capture. Basically, the clock and strobe must be at the longest delay of all signals because the address and data must settle before the data is captured.

Hartley: The key is to route the strobe to the longest so that it has the greatest delay and arrives last.

Olney: Exactly, and that's what a lot of people don't do. They have the strobe arriving first and then the data last, and you get all the reflections and noise. You don't know whether it's going to capture the correct data.

Hartley: The first time I did a DDR2 design was at L3 in 2012, and the next one we did was also DDR2 in 2014. One of our engineers did a timing analysis of the design in 2014. He came up with a number that nobody believed. Everybody in engineering said, "Oh, this can't be right, because all the app notes say that DDR timing is so critical." We came up with a number that said, for example, that the address line only needed to be ±125 mils from some optimal length, which is basically ± 3 mm. Everybody said, "This can't be right." Yet shortly after that, I ran into a note that I found from Keysight Technology, written by an engineer named Chang Fei Yee, who wrote:

"Maximum DDR2 skew of trace length to meet timing margin. In order to be compliant with the JEDEC specification, the maximum skew among all signals shall be less than ±2.5% of the clock period drew in by the memory controller. All signals of the SDRAM are directly or indirectly referenced to the clock, for example in normal FR-4 material with a dielectric constant of approximately four, a differential clock-rate of 1.2GHz, the maximum skew shall be ±125 mils, or ± 3 mm."

This is precisely the number we came up with, even though half the engineers in our department said it couldn't be right. I intentionally mismatched the length of some of these lines just to keep them within that quarter of an inch distance from one another, and the thing worked perfectly. That was when I first realized how noncritical this really is.

Olney: I have a table on that, Rick. For 166 MHz, the interconnect margin is 155 picoseconds.

Hartley: Yes, which is huge!

Olney: That relates to about 75 mils.

Hartley: I know, it's crazy. And people route these things within ±5 mils or ± 0.1 mm.

Olney: I guess I'm one of those crazy people because I'm a PCB designer, and the way I see it is everything has to be done properly. Whether it's a really fast DDR4 or a slow 200 MHz DDR, I route them all the same. I route them all to 10 picoseconds delay and it doesn't take any extra time to do that. People say, "Why should I have it so accurate?" Well, if you just do it out of habit every time then your design works perfectly. If it is 125 out, it might work on the test bench, but if you put it in the field and temperature cycle it, it will fall over. To make it reliable and performing efficiently, you need to have it spot on, and it takes little extra effort to do it that way.

Hartley: That is exactly what we did on the result. We intentionally misrouted a few of them in the prototype because I just wanted to see how it would function. We straightened it up in the final design, but we didn't go to these crazy lengths to make things ridiculously tight the way a lot of people do; we just routed them. We put serpentining in a couple of them to get them all within a reasonable skew margin and they worked perfectly. They worked perfectly in the field—and this is avionics, where it had to go through tremendous temperature cycling. There are many of these nav systems flying around in the world today, and the last I heard they were all working perfectly.

Barry Matties: Did you do any simulation on those, Rick?

Hartley: After the timing analysis we did simulation to verify that the timing analysis was right, and it said that it was right also. That was kind of a double blessing, and as Barry pointed out, DDR3 is even more forgiving, because it balances the lines. With DDR2, you had to do some amount of branch routing to get things to be timed correctly. With DD3, you don't have to do that. You simply route things in daisy-chain fashion, and it sends out a test pulse to

Rick Hartley

figure out what the line links are, and then calibrates everything to be at the right time. There's a more sophisticated way to say that, but you get the point.

Olney: Also a lot of people think, Rick, that you can't use fly-by routing with DDR2. That's not correct, I have done it before, it just needs you to hard code the clock delays to each chip from the strobe. So, the data is captured at exactly the right time as the clock passes on the fly-by. If you hard code them manually you'll be doing the same thing as your auto-leveling would do in DDR3c.

Hartley: Yes, DDR3 is automatic. That's interesting. I did know that was possible with DDR2.

Olney: Fly-by routing is a lot easier to route than T-topology because you have a lot more room to route around the outside of the chips instead of going straight through them point to point.

Hartley: I agree, no doubt about it. With the first DDR3 design we did, I realized we could do fly-by routing. What a blessing; that made life so much easier. And I've never done DDR4, so I don't know this for sure, but doesn't it signal the receiver that certain bytes upon receive have to be launched high?

With the first DDR3 design we did, I realized we could do fly-by routing. What a blessing; that made life so much easier.

Olney: I don't really get into that side of it, that's more the firmware of the chips, but I believe it does do that.

Hartley: The advantage is that you don't have a drain on the power bus. The instantaneous L(di/dt) drops in the power bus can lead to switching noise. If you're not switching as many lines at once from the driver, this won't happen.

Olney: Exactly, that was the idea of fly-by to start with so that all the signals weren't clocked at the same time. There's not as much simultaneous switching noise.

Shaughnessy: We get a lot of views on any article with DDR in the title. In our surveys with designers, they say they're having a hell of a time with DDR. You both have said in the past that DDR isn't really that difficult if you just follow the process, so why do so many designers and engineers have trouble with it?

Olney: I think it's uncertainty. They're not sure if it will work and they don't have simulation tools to confirm it, so it's up in the air. They hope it works, but they're not sure.

Hartley: That's a very good point. I think you hit the nail on the head. Lee Ritchey has a term called "design by fear." A lot of people aren't sure, so they take the worst possible case and figure, "I had better do this just to make sure it's going to work."

Olney: The main issue that I see with DDR routing is that people don't choose the right impedance. DDR3 needs to be routed to 40 ohms single-ended and 80 ohms differential impedance. A lot of people still route to 50/100 ohms single-ended/differential. They just can't get in their heads that it's 40 ohms and 80 ohms. That's all to match the drivers. The drivers are normally 34 ohms. They have the wrong impedance to start with, which gives them more reflections. If you are routing to 50/100 ohms, you are going to get more reflections coming back. Data lanes must be routed on the same layer, generally the stripline layer. All the data lanes can be routed on one embedded stripline layer if the pinout of the FPGA is correct. The pin assignments should facilitate routing. You can order them so that the routing can just flow out and into the memory chips then the data with the strobe can be routed in each byte line out to the memory chips on one layer.

Then, the fly-by—the address—can go on that same layer because the address lines are on the other side of the memory chips away from the FPGA. You need to break out from the FPGA with two layers of the address and clock and take it around to where the fly-by traces come through; then they can branch down to the same layer as the data. You only need two layers to route it on.

Matties: This might be kind of a silly question, but isn't all this available on Google? I Googled DDR and the first thing that came up was that the clock needs to be longer. It needs to arrive after the data.

Olney: Google is smart but not always right.

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Hartley: There's so much on Google that people don't know what to believe.

Shaughnessy: I read an article that you wrote six years ago, Barry, and you explained that DDR specs can be downloaded from JEDEC.org. If you want the real specs, go to JEDEC.org and get them. Why don't people just do that?

Hartley: DDR3 is the JEDEC-793B standard, so just download and read it and you'll know exactly what to do. Right, Barry?

Olney: That's right. But there is a lot of data to go through. I should also point out that Andy and I were talking about datasheets always being wrong the last time we spoke, and it's the same with DDR specs. If you go to Micron, they have one spec, one timing analysis; JEDEC has another, and Xilinx has another. They're all different. There's not one spec that's the same.

Hartley: Right. That's a good point. Here's a comedic story about that: The first time I ever did DDR2 (I won't say whose device we were using as the controller), in the app note section for DDR2 for that device, they actually said, "We had such a hard time getting this thing to work that if you don't design it exactly as we did, we won't guarantee it will work." They said, "We'll give you our Gerber files, and if you're a Cadence user, we give you the design file, and if you don't copy it exactly, we make no guarantees."

And I thought, "Who are these people?" The lead engineer called me up and said, "Rick, did you read this? This is terrifying; are you going to do that?" Knowing he was the nervous type, I said, "We will take care of it, don't worry about it. Everything's good." I didn't do anything they said in the app note, and it all worked perfectly.

Olney: Reference designs are always bad designs.

Hartley: Almost always. I don't think I've ever seen a reference design that was really good. I really don't.

Olney: I've seen DDR2 routed on four-layer boards in reference designs, and how they get it to work I'll never know.

Matties: It sounds like it's not that complicated if you do your homework.

Olney: If you follow a methodology, you can't get it wrong, really.

Shaughnessy: So, designing DDR involves a few slightly different steps than a typical high-speed board?

Olney: Each technology has different constraints, so you want to keep the technologies apart. If you have a 5-volt or 3-volt technology next to a memory that's 1.5, then you're going to get more crosstalk because it's a higher voltage; there's separation. You have technology rules, and you have the rules that separate the technologies.

You have technology rules, and you have the rules that separate the technologies.

Hartley: I've told people for years that whenever I would do a circuit board with multiple powers driving different technologies—let's say 1.5, 2.5, 3.3, and 5 volts—I make sure that I place the parts, as much as possible, so that they each have their own power distribution sections, for several reasons. One, you have fewer power planes because you can divide the plane up into multiple pieces; second, you're not routing 1.5-volt or 1.8-volt lines next to

3.3-volt lines, which will severely increase crosstalk into the lower voltage line.

Olney: The last design I did had 35 different power supplies.

Hartley: Now that becomes tougher.

Olney: How do you put 35 different copper pours in? The main processor BGA has four or five different supplies that must connect to other circuitry; that blocks your routing channels and makes it really challenging: "We'll fit them in here or there on plane or signal layers." But when you start routing it, pushing traces around and trying to get around these copper pours, it's very difficult.

Hartley: It is very challenging, I agree.

Olney: One of the nice things about DDR is that it's source-synchronous, and so you can route it to a 4-mil trace with 4-mil spacing. You don't have to worry about crosstalk because the data and address arrive at the memory chips and it has time to settle before the clock and strobes come along and capture that data. Providing the clock is a little bit longer, it all works without crosstalk and reflections. You just don't want to get the data and address mixed up.

Shaughnessy: Barry, in your columns you talk about the benefits of using a router for DDR3 and that designers typically don't like autorouters, but you said they can be very useful here and you can drive the router with the schematic.

Olney: Absolutely. If you set up the constraints properly in the schematic then you can drive the router from the schematic, which I do. First, when you select a chip—maybe from the main processor or a part of that, mainly just the memory bus—you fan out from that, generally from the top layer to internal layers so you don't have to route on the external microstrip layer, which can radiate a lot of EM; it's also faster speed so you don't have to worry about the difference in propagation delay, between different layers. Stripline traces also have less crosstalk which means you can route in closer proximity. I fan out first, and then I'll select the first data bus going to the first memory; I will route that with the router, so I route it bit by bit and as I do it, I clean it up. If it doesn't do it quite perfectly, I can push and shove it around and get the signals almost right.

Once you've basically routed it and you've made sure you've got a little bit of room for serpentines, then you can apply the fine tuning, the auto-tuning of the routes. Cadence and Altium can route to delay, so you don't route to length anymore. Length and delay are two totally different things, depending on which layer you're on, so if you're routing to delay, you're getting the exact numbers, the exact flight time, to every chip in comparative flight time.

Shaughnessy: Do designers run into trouble with the other serial links like PCI Express? Or is that just a different animal?

Olney: Generally, PCI Express goes to a connector, so they're spread out to start with and you just follow the pattern and basically route them in order. You can have them tightly together, and you must in most cases.

Hartley: It is a different animal, and it's like ethernet or any of those things; they generally go to a connector.

Shaughnessy: But DDR can be employed anywhere. That's the beauty of it, I guess.

Olney: It can also go to a connector. You may have onboard memory, or if you could have SODIMMs, for instance. When you're routing to SODIMMs, it's quite a different strategy than routing to onboard memory. In onboard memory, you generally don't have series terminators on your data. With plugin memory,

then you need the series terminators to prevent reflections on the long data lines.

Matties: Over the years, expert designers have told us that with high-speed design, there really is no substitute for experience. How does a young design engineer become an expert at DDR?

Hartley: They make a lot of mistakes. I certainly did early on.

Olney: My wife says to me when I'm writing my articles, "Why are you giving all of your secrets away?" I say, "Because nobody can remember them. I can't remember them." (Laughs) You've got to try to recall it all.

Hartley: My wife asked me that about the classes I do, "Why are you telling everybody all the stuff you know?" I told her, "Well, I'm not going to live forever, for one thing, and I want the world to get as much of this as we can give them."

Matties: Is there a role for EDA tools that helps in this regard? When does the tool come in and really help take the heavy load?

> You can't just hand someone a simulation tool and expect them to simulate a board. They have to know how it all works and understand it.

Olney: First, you need to understand the technology behind it. You can't just hand someone a simulation tool and expect them to simulate a board. They have to know how it all works and understand it. It is the same with routing, placement, and positioning power supplies—they have to understand why they're doing certain things. You have to teach them, but it's also experiences—you have to gain the knowledge over time. It doesn't matter how good your tool is if you don't know how to drive it.

Hartley: To make matters worse, as we all know, there are not more than two universities on the planet that teach circuit board design. Young people coming out of school have no understanding of this stuff, and young engineers are being pushed into board design. In our day, you could choose a path. Today, almost all the young engineers are doing the circuit design and the board design, and they're thrown into it with no knowledge of the things Barry is talking about; they've got to figure it out quickly.

Shaughnessy: Could you guys teach a new EE how to do DDR design in one month? Or six months?

Hartley: I think it is possible within one design cycle. What do you think, Barry?

Olney: Yes, I've trained many PCB designers. I have taught a lot of people how to design high-speed boards and they usually become excellent after a year; I check their work and they make no mistakes; they just follow the process. They probably need at least two design cycles to be a proficient independent designer, as each board is different.

Hartley: If you want to learn the whole high-speed design philosophy, it takes about a year. But if you just want to learn how to design DDR, you will have that down in one or two design cycles.

Olney: If you want to simulate it, that's a different story altogether as there are a lot of issues. Models are the biggest issue, and I've actually developed software that can help me, in par-

ticular, to extract sub-models from models because, quite often, models won't work. It's pretty straightforward: You extract the topology, the transmission line into the simulation tool from the board layout, and then you attach the IBIS models to each end, but when they don't work, what do you do? You've got nothing. Now, I have software that extracts the sub-models from a non-working model, and it creates a new model that I can use.

The other issue is a lot of signals like PCI Express and Ethernet go off the board, so what then? You have a connector on the end of the board that all your signals go to. The trick there is not to use the connector model but to use the driver model in reverse and use the driver model so you can simulate the actual board. You can't control what happens off the board, you can only make the board perfect and then someone attaches a mile of cable to it.

Hartley: That's the other thing—you basically have to simulate that cable at its impedance to determine how to design the board to drive that cable properly.

Olney: Not really, because the impedance of the receiver, if you stick it in place of the connector, you will have the right impedance.

Hartley: The receiver will, yes, but what if it's a long cable? Long enough that you care about its impedance?

Olney: That's what I'm saying: You can't control what happens off the board; you can only deal with what's on the board.

Shaughnessy: What final advice would you give to someone who is working with DDR and is having a hell of a time with it? Any tips or tricks? Anything?

Olney: Basically, you need to read a lot and educate yourself. With DDR3, 4, and 5, it is important to use the correct impedance of 40/80 ohms, and check the timing and channel isolation. Simulate the clocks/strobes and the two worst nets of each group as you don't have time to evaluate each individual signal. Then compare the flight times of each signal to the clocks/strobes, which is a lot quicker.

Understand at what point a transmission line becomes distributed vs. lumped and how you treat it. You must control its impedance.

Hartley: I would say read a lot. If you have access to good simulation tools, use them. Understand at what point a transmission line becomes distributed vs. lumped and how you treat it. You must control its impedance. Usually with DDR, of course, you must control impedance; that's true of any high-speed design. If it's short enough you don't have to worry about it, but if it's a distributed link, of course you do. I treat all lines as if they are distributed, assuming they may route long enough to be distributed. If they're not distributed, then we simply don't terminate.

Matties: This is great, guys. We appreciate so much your time, thoughts, and insights. Thank you both.

Olney: Thank you. Great speaking with you guys, and Rick, nice to chat with you.

Hartley: Thank you, Barry. I read your column every month. I'm glad we had the chance to talk. DESIGN007

The Top Five Reasons Products Fail EMI Testing

Feature Article by Kenneth Wyatt
WYATT TECHNICAL SERVICES

Introduction

The three top product failures I see constantly in my consulting practice are radiated emissions, radiated susceptibility, and electrostatic discharge. After reviewing and testing hundreds of products over the years, I've come to the conclusion that products fail these tests for five common reasons (somewhat in order of incidence):

1. **PCB design**—Poor layout and layer stack-up.
2. **Cable shield termination and pigtails**—Cable shields are not terminated to enclosure or lack of common mode filtering for unshielded products, plus shield pigtails used.
3. **Gaps in the return path**—High-frequency clocks or signals crossing gaps in the return path.
4. **Power distribution design**—Poor power distribution network (PDN) design.
5. **Shielding design**—Apertures or slots in the shielded enclosure that are too long.

1. PCB Design

The single most important factor in achieving EMC/EMI compliance revolves around the printed circuit board design. It's important to note that not all information sources (books, magazine articles, or manufacturer's application notes) are correct when it comes to designing PCBs for EMC compliance—especially sources older than 10 years or so. In addition, many "rules of thumb" are based on specific designs, which may not apply to future or leveraged designs. Some rules of thumb were just plain lucky to have worked.

PCBs must be designed from a physics point of view and the most important consideration is that high frequency signals, clocks, and power distribution networks (PDNs) must be designed as transmission lines. This means that the signal or energy transferred is propagated as an electromagnetic wave. PDNs are a special case, as they must carry both DC current and be able to supply energy for switching transients with minimal simultaneous switching noise (SSN). The characteristic impedance of PDNs is designed with very low impedance (0.1 to 1.0 ohms, typically). Signal traces, on the other hand, are usually

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designed with a characteristic impedance of 50 to 100 ohms.

Understanding PCB design is all about two important concepts: all currents flow in loops and high frequency signals are propagated as electromagnetic waves in transmission lines. These two concepts are closely related and coupled to one another.

Currents Flow in Loops

Circuit theory suggests that current flows in loops from source to load and back to the source. In many cases of product failure, the return path has not been well defined and in some cases, the path is broken. The problem circuit designers often miss is defining the return path of a high frequency signal back to the source. If you think about it, we don't even draw these return paths on the schematic diagram—we just show it as a series of various "ground" symbols.

So, what is "high frequency"? Basically, it is anything higher than 50 to 100 kHz. For frequencies less than this, the return current will tend to follow the shortest path back to the source (path of least resistance). For frequencies above this, the return current tends to follow directly under the signal trace and back to the source (path of least impedance) as shown in Figure 1.

To reduce EMI, we need to minimize the area of these loops. Undefined return paths often result in large current loops from source to load and back to source. These large current loops start to look like loop antennas, coupling noise currents to "antenna-like" structures, such as cables, in your product or system.

Where some board designs go wrong is when high dV/dt return signals, such as those from low frequency DC/DC switch mode converters or high di/dt signals from digital logic and clock return signals get comingled with I/O circuit return currents, sensitive RF modules (especially receivers), or sensitive analog return currents. Just be aware of the importance of designing defined signal and power supply return paths. That's why the use of solid return planes under high frequency signals and then segregating digital, power, and analog circuitry on your board is so important.

How Signals Move

At frequencies greater than about 50 to 100 kHz, digital signals start to propagate as electromagnetic waves in transmission lines. A high-frequency signal (Figure 2) propagates along a transmission line (circuit trace over return plane, for example), and the wave front induces a conduction current in the copper trace and back along the return plane. Of

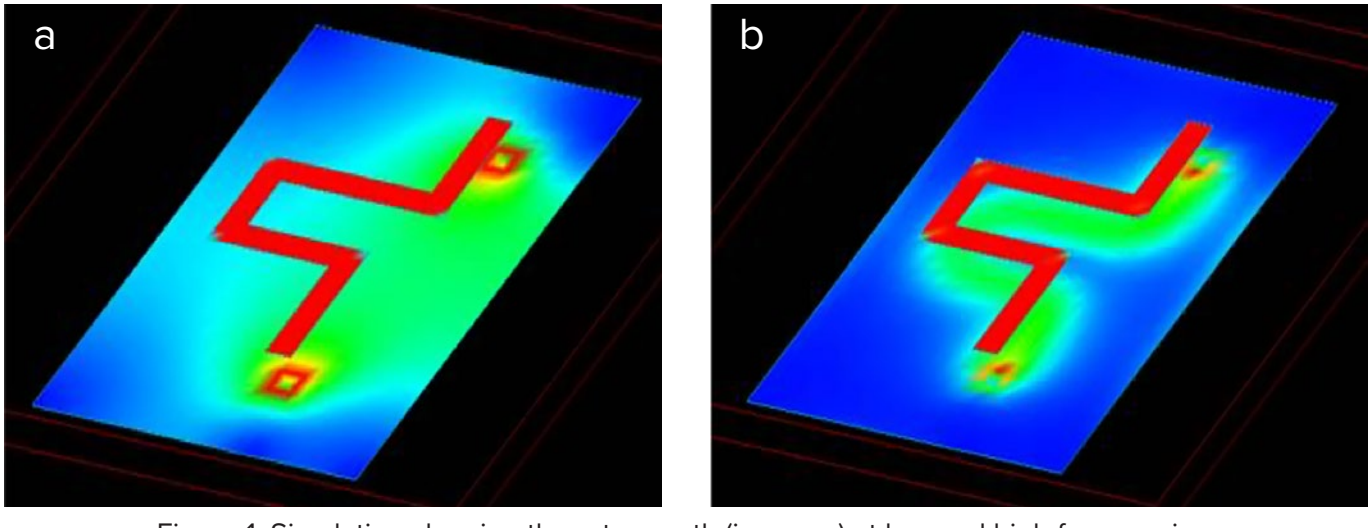

Figure 1: Simulation showing the return path (in green) at low and high frequencies. (Image source: Keysight Technologies)

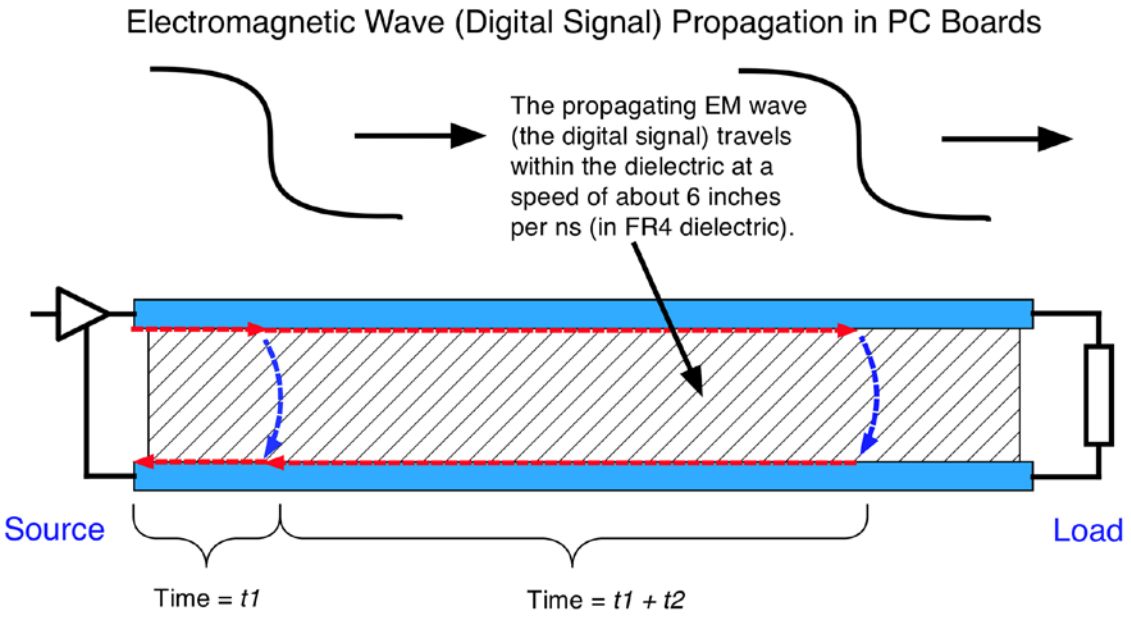

Figure 2: A digital signal propagating along a microstrip with currents shown. (Image source: Eric Bogatin)

course, this conduction current cannot flow through the PCB dielectric, but the charge at the wave front repels a like charge on the return plane, which "appears" as if current is flowing. This is the same principle where capacitors appear to "pass" AC current, and Maxwell called this effect "displacement current."

The signal's wavefront travels at some fraction of the speed of light, as determined by the dielectric constant of the material, while the conduction current is comprised of a high density of free electrons moving at about 1 cm/second. The actual physical mechanism of near light speed propagation is due to a "kink" in the E-field, which propagates along the molecules of copper. The important thing is that this combination of conduction and displacement current must have an uninterrupted path back to the source.

A high electric field is generated by high frequency digital signals occurring between the microstrip and return plane (or trace). If the return path is broken, the electric field will "latch on" to the next closest metal, which will not likely be the return path you want. When the return path is undefined, then the electromagnetic field will "leak" throughout the dielectric and cause common mode currents to flow all over the board. The uncontrolled field will also cause cross-coupling of clocks or other high-speed signals to dozens of other circuit traces within that same dielectric through coupling to vias within the dielectric layer. The resulting common mode currents will tend to couple to "antenna-like structures," such as I/O cables or slots/apertures in shielded enclosures, resulting in EMI.

Circuit Board Stack-Ups

Most of us were taught the "circuit theory" point of view and it is important when we visualize how return currents want to flow back to the source. However, we also need to consider the fact that the energy of the signal is not only the current flow, but an electromagnetic wave front moving through the dielectric, or a "field theory" point of view. Keeping these two concepts in mind just reinforces the importance of designing transmission lines (signal trace with return path directly adjacent), rather than just

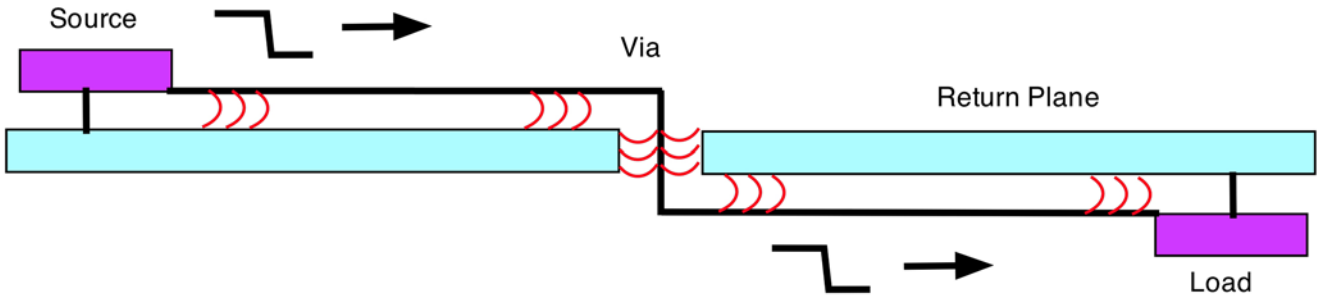

Figure 3: A signal trace passing through a single reference plane.

simple circuit trace routing. A successful PC board design accounts for both viewpoints.

In order to satisfy both the circuit and field theory viewpoints, we now see the importance of adjacent power and power return planes, as well as adjacent signal and signal return planes. Signal or power routes referenced to a single plane will always have a defined return path back to the source. Figure 3 shows how the electromagnetic field stays within the dielectric on both sides of the return plane. The dielectric is not shown for clarity.

On the other hand, if a signal passes through two reference planes (Figure 4), things get a lot trickier. If the two planes are the same potential (for example, both are return planes), then simple connecting vias may be added adjacent to the signal via. These will form a nice defined return path back to the source.

If the two planes are differing potentials (for example, power and return), then stitching capacitors must be placed adjacent to the signal via. Lack of a defined return path will cause the electromagnetic wave to propagate throughout the dielectric, causing cross coupling to other signal vias and leakage and radiation out the board edges as shown.

For example, let's take a look at a poor (but very typical) board stack-up that I see often (Figure 5). Notice the power and power return

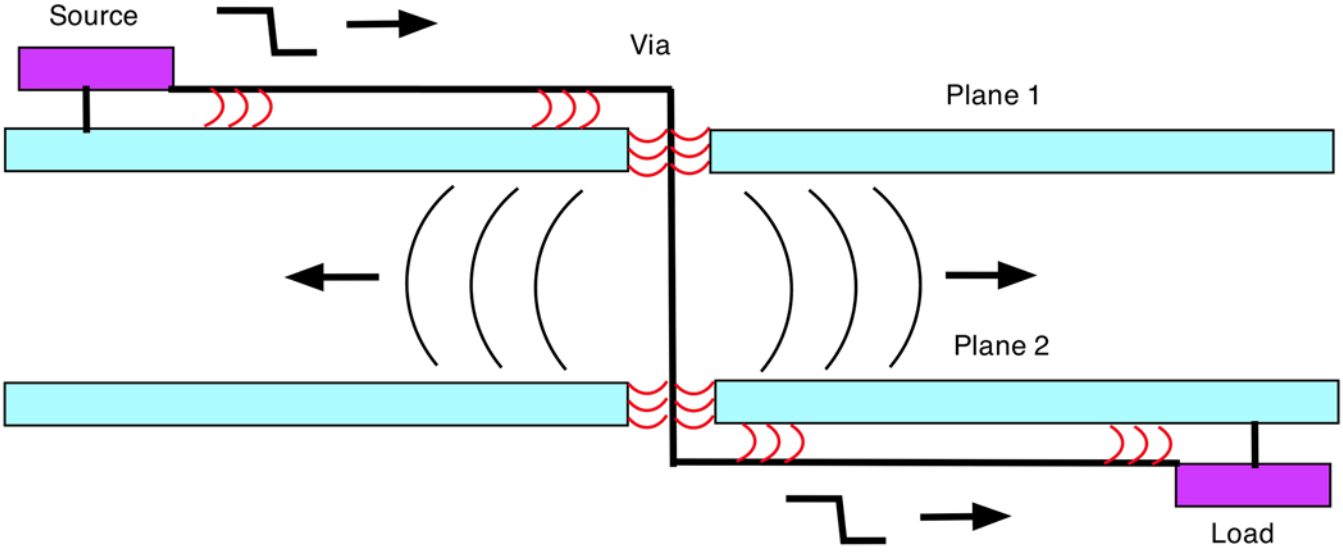

Figure 4: A signal trace passing through two reference planes. If the reference planes are the same potential (signal or power returns, for example), then stitching vias next to the signal via should be sufficient. However, if the planes are different potentials (power and return, for example), then stitching capacitors must be installed very close to the signal via. Lack of a defined return path will cause the electromagnetic field to leak around the dielectric, as shown, and couple into other signal vias or radiate out board edges.

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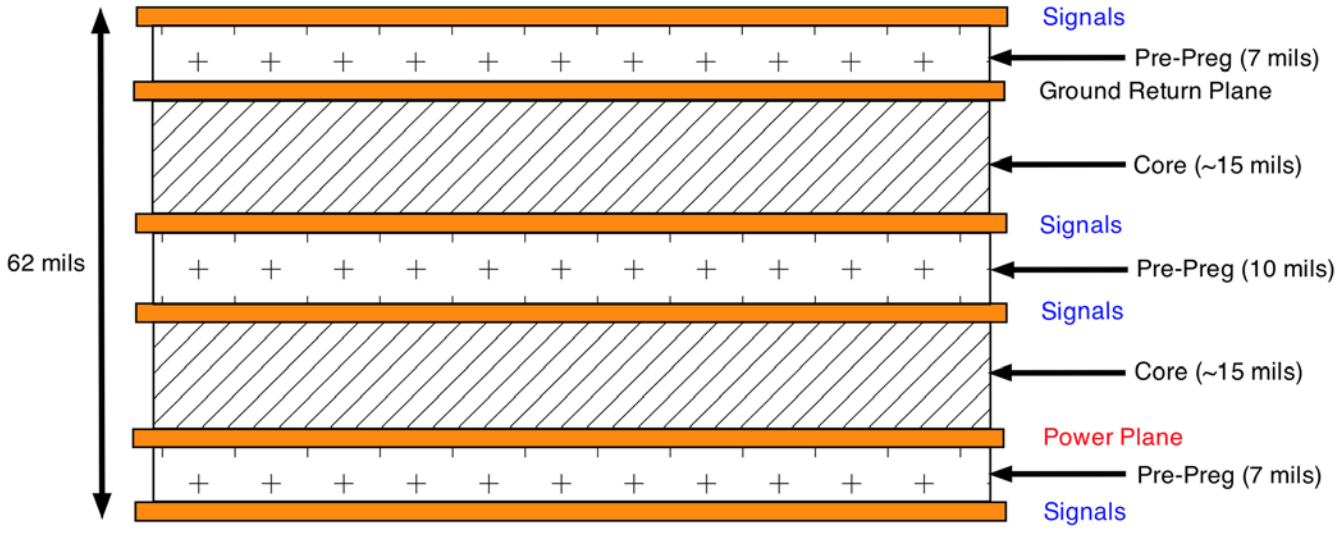

Figure 5: A six-layer board stackup with very poor EMI performance.

planes are three layers apart. Any PDN transients will tend to cross couple to the two signal layers in between. Similarly, few of the signal layers have an adjacent return plane, therefore, the propagating wave return path will jump all over to whatever is the closest metal on the way back to the source. Again, this will tend to couple clock noise throughout the board.

A better design is shown in Figure 6. Here, we lose one signal layer, but we see the power and power return planes are adjacent, while each signal layer has an adjacent signal (or power) return plane. It's also a good idea to run multiple connecting vias between the two return planes in order to guarantee the lowest impedance path back to the source. The EMI performance will be significantly improved using this, or similar designs. In many cases, simply rearranging the stack-up is enough to pass emissions.

Note that when running signals between the top and bottom layers, you'll need to include "stitching" vias between the return planes and stitching capacitors between the power and power return planes right at the point of signal penetration in order to minimize the return

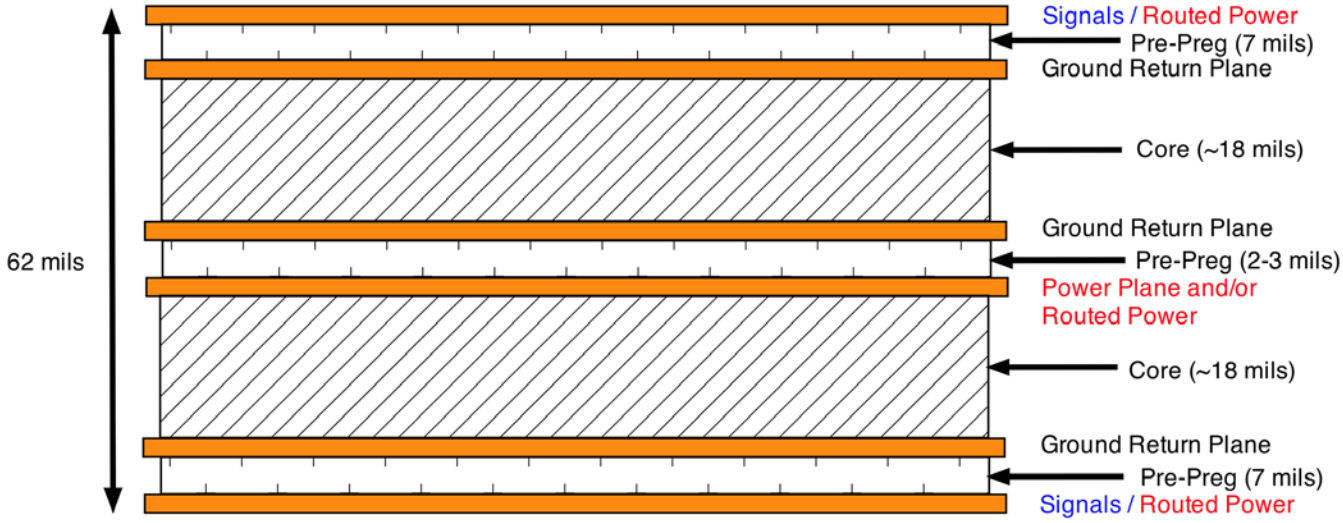

Figure 6: A six-layer board stackup with good EMI performance. Each signal layer has an adjacent return plane, and the power and power return planes are adjacent.

path. Ideally, these stitching vias should be located within 1 to 2 mm of each signal via.

Other Tips

Other design tips include placement of all power and I/O connectors along one edge of the board. This tends to reduce the high frequency voltage drop between connectors, thus minimizing cable radiation. Also, segregation of digital, analog, and RF circuits is a good idea, because this minimizes cross coupling between noisy and sensitive circuitry. Of course, high-speed clocks, or similar high-speed signals, should be run in as short and as direct a path as possible. These fast signals should not be run long board edges or pass near connectors.

Refer to the end of the article[1-4] for further details on PCB design and how fields move through transmission lines.

2. Cable Shield Termination

Cable Penetration

The number one issue I find when tracking down a radiated emissions problem is cable radiation. The reason cables radiate is that they penetrate a shielded enclosure without some sort of treatment—either bonding the cable shield to the metal enclosure or common mode filtering at the I/O or power connector (Figures 7 and 8). This occurs frequently, because most connectors are attached directly to the circuit board and are then poked through holes in the shield. Once the cable is plugged in, it is "penetrating the shield" and EMI is the usual result.

There are four combinations or cases that must be considered: shielded or unshielded products and shielded or unshielded cables. Power cables are usually unshielded for consumer/commercial products and so require power line filtering at

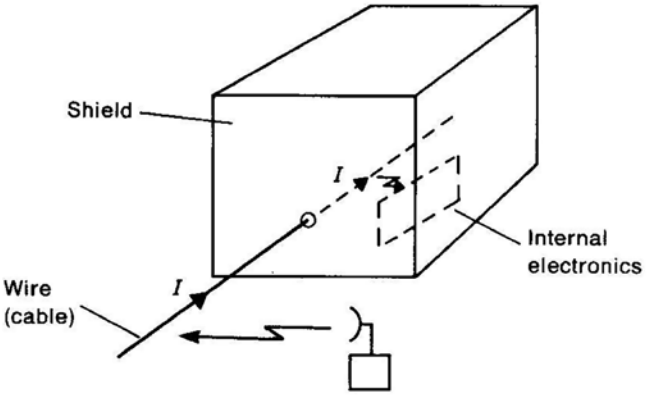

Figure 7: Penetrating the shield with a cable defeats the shield. This example shows how external energy sources can induce noise currents in I/O cables, which can potentially disrupt internal circuitry. The reverse is also true, where internal noise currents can flow out the cable and cause emissions failures. (Image Source: Henry Ott)

the point of penetration or at the connector of the circuit board. Shielded cables must have the shield bonded (ideally in a 360-degree connection) to the product's shielded enclosure. If the product does not have a shielded enclosure, then filtering (usually common mode) must be added at the point of penetration or at the I/O connector of the PCB. Figure 8 shows the usual result when connectors simply poke through a shielded enclosure.

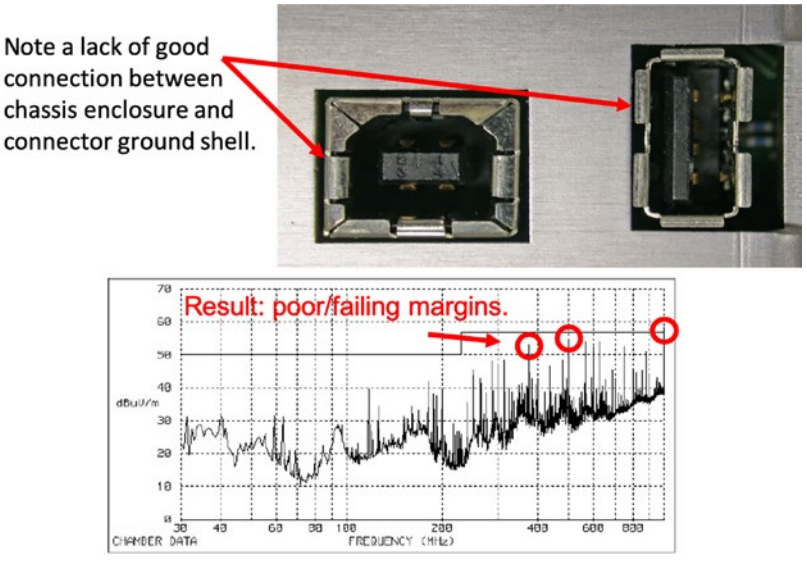

Figure 8: Result of a penetrating cable through a shielded enclosure, because of un-bonded I/O connectors to the shielded enclosure.

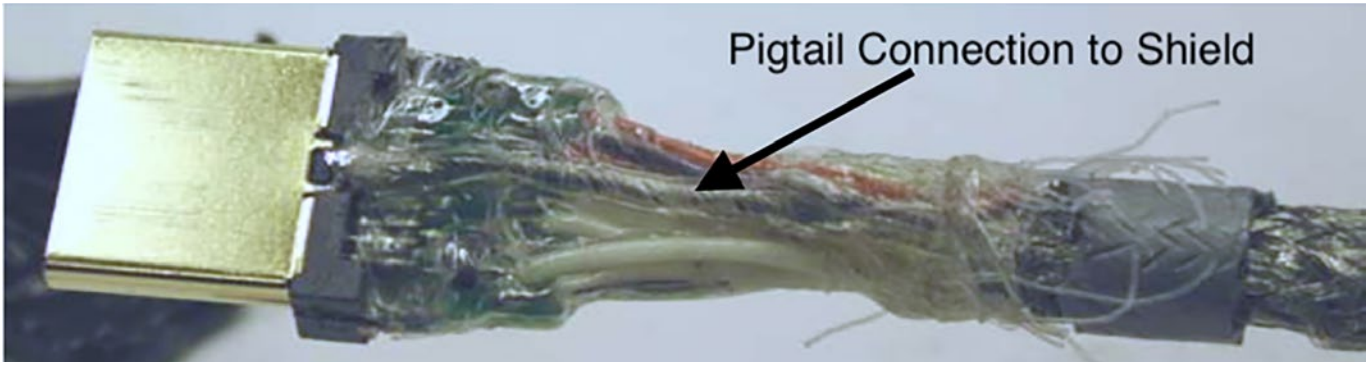

Figure 9: An example of a poor cable shield termination in an HDMI cable. (Image source: Dana Bergey)

Cable Shield Terminations

Another potential issue is if the I/O cable uses a "pigtail" connection to the connector shell (Figure 9). Ideally, cable shields should be terminated in a 360-degree bond for lowest impedance. Pigtails degrade the cable shield effectiveness by introducing a relatively high impedance. For example, a 1-inch pigtail connection has 12 ohms impedance at 100 MHz and gets worse the higher you go in frequency, thus defeating the cable shield.

This is especially problematic for HDMI cables, because the HDMI working group[5] failed to specify the method for terminating the cable shield to the connector. Fortunately, they are aware of the issue and will better define a proper termination method in the next revision of the standard. In the meantime, there is no guaranty that a particular cable, when used for formal certification testing, will work well, or not. Trial and error of several brands is recommended.

Here are the results in testing eight different brands of HDMI cable (Figure 10). Each was driven with a signal generator and measured in an EMI chamber while sweeping the frequency, and is detailed in a report.[6]

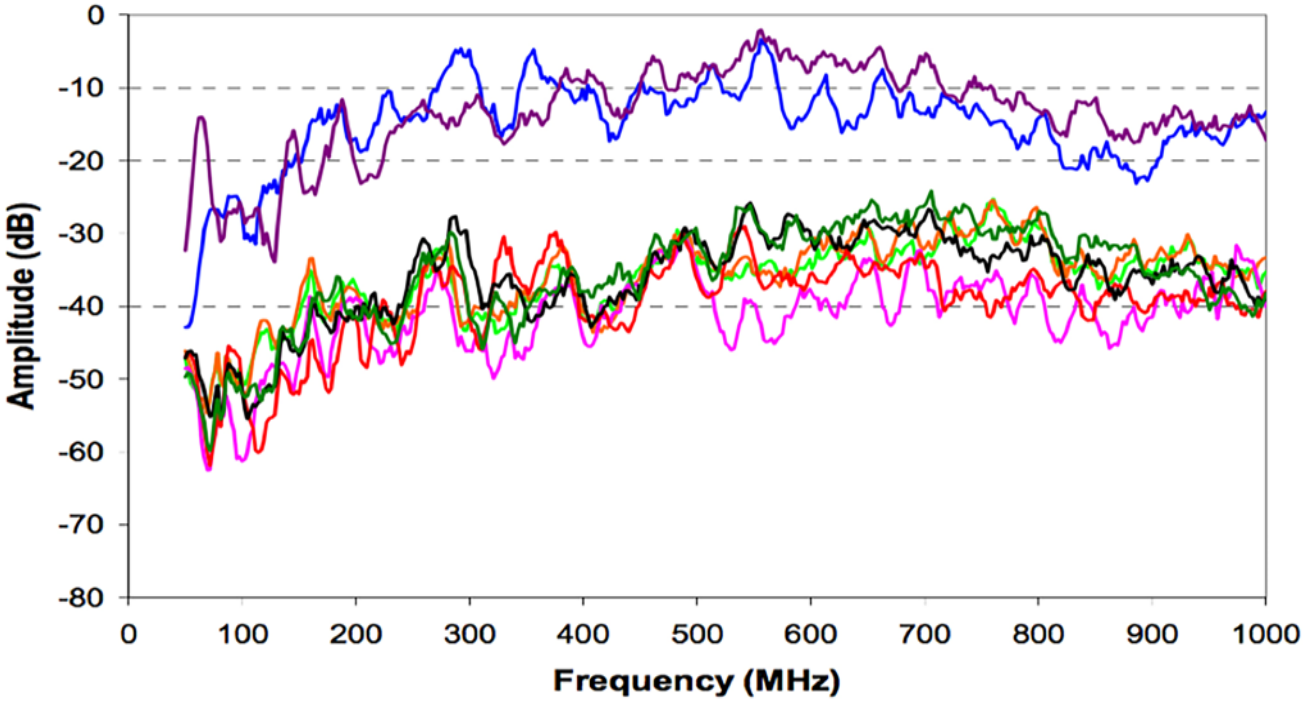

Figure 10: The results of testing eight HDMI cables from 30 to 1,000 MHz. As you can see, two of these exhibited 25 dB worse emissions across the band. (Image Source: Dana Bergey)

3. Gaps in The Return Plane

Breaks or gaps in the return path are major causes of radiated emissions, radiated susceptibility, and ESD failures. Let's come back to the issue of a gap or slot in the return plane mentioned earlier and show an example of why it's bad news for EMI. When the return path is interrupted, the conduction current is forced around the slot, or otherwise finds the nearest (lowest impedance) path back to the source. The electromagnetic field is forced out and the field will "leak" all over the board. I have an article and good demonstration video of this and how it affects common mode currents and, ultimately, EMI (Figure 11).[7] This would be a great demo to construct and show your own colleagues!

The difference between the gapped and un-gapped traces is shown in Figure 12. Note the harmonic currents are 10-15 dB higher for the gapped trace (in red). Failing to pay attention to the signal and power return paths is a major cause of radiated emissions failures.

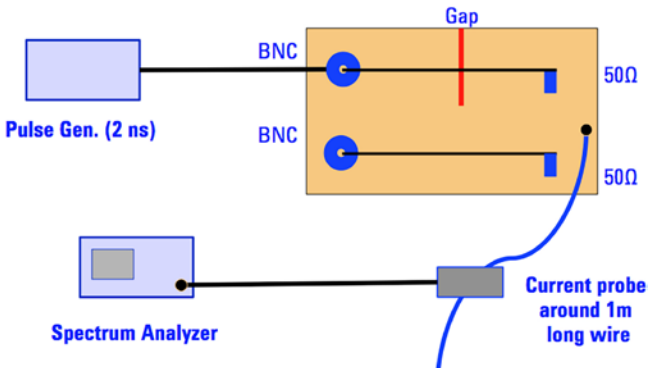

Figure 11: Shows a demonstration test board with transmission lines terminated in 50 ohms. One transmission line has a gap in the return plane and the other doesn't. A 2 ns pulse generator is connected to one of the two BNC connectors in turn and the harmonic currents in a wire clipped to the return plane are measured with a current probe.

4. Power Distribution Network Design

Power distribution network (PDN) design requires a low impedance (0.1 to 1.0 ohms, typically) transmission line through at least 30 MHz. The purpose of a PDN is to transfer energy from the power source (often a volt-

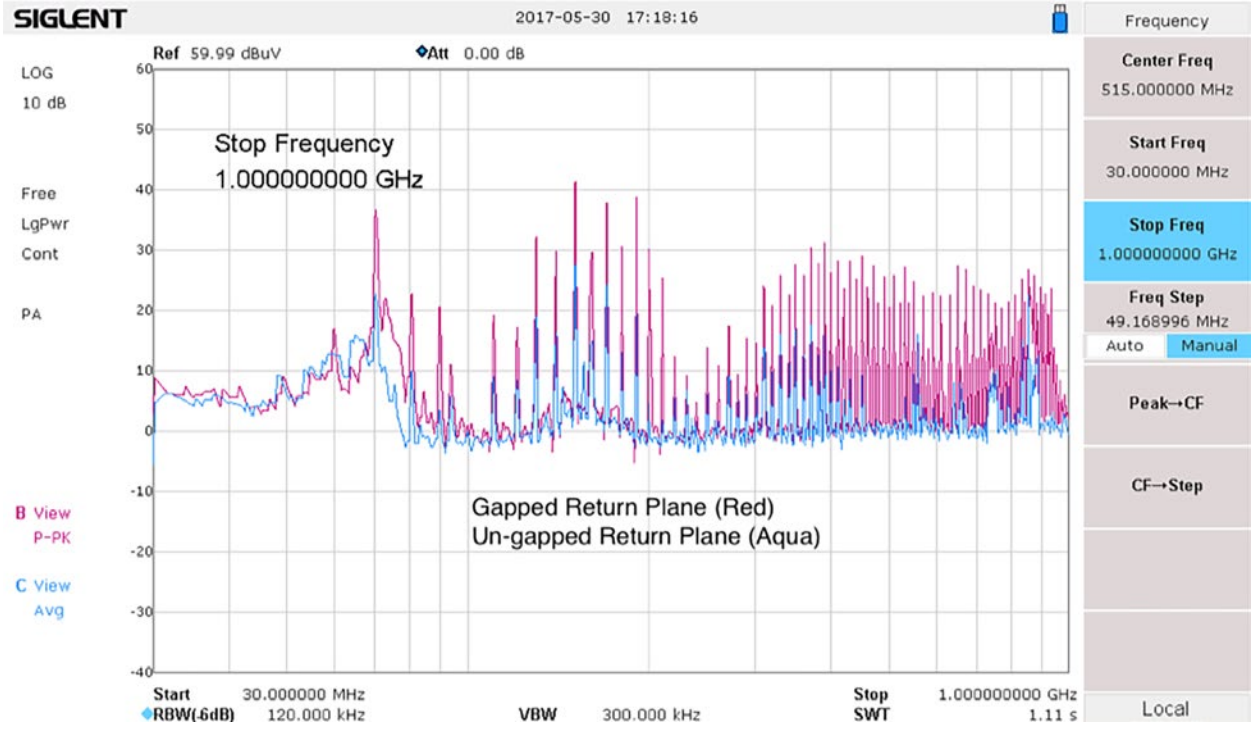

Figure 12: The resulting common mode currents on an attached wire as measured with a current probe. The trace in aqua is the un-gapped return path and the trace in red, the gapped return path. The difference is 10-15 dB higher for the gapped return path. These harmonic currents will tend to radiate and will likely cause radiated emissions failures.

age regulator module on the PC board) to the switching IC as fast as possible.

When the output stage of a digital IC switches from high to low or from low to high, there is a period when both output devices are partially turned on. This causes a large current pulse between the supply rail and power return pin of the IC. This "shoot through" current pulse tends to lower the supply voltage, causing what's known as simultaneous switching noise (SSN) on the power rail. This SSN tends to propagate throughout the PCB. A well designed PDN minimizes this SSN.

Capacitors, in the form of bulk, decoupling, and board capacitance, are used to store enough energy to overcome the tendency of the power rail voltage to decrease. Figure 13 shows a typical circuit model of a PDN with the power source on the left, supplying energy to the IC on the right. In between, we have a series of energy storage capacitors and transmission lines (PC traces). Unfortunately, it takes significant time to transfer the required energy from the power source to the IC. It has been shown that it takes about 600 ps to transfer an amp of current across 1/16th inch of die bonds.[11] That's why it's especially important to keep PDNs short and direct as possible.

Ideally, the total energy demand will be met by the "on-chip" capacitors, if any, plus the energy stored in the power plane capacitance. However, these are seldom enough storage, so we depend a lot on nearby decoupling capacitors to supply the remaining energy demand. It is critical for the decoupling capacitors to have as little series inductance (in the form of internal inductance and trace inductance) as possible. The greater this series inductance, the harder it is to supply the required energy to the load and SSN results with related noise coupling throughout the PCB.

Assuming the decoupling and any built-in capacitance of the PCB can supply the energy needs, then the job of the bulk capacitor is to "recharge" the energy of the downstream capacitors in between switching transients. For the fastest recharge times, the PDN must be in the form of low impedance transmission lines.

The bulk capacitors (4.7-10 μF, typ.) are usually placed near the power input connector and the decoupling capacitors (1 to 10 nF, typ.) nearest the noisiest switching devices. To achieve the lowest series inductance, all decoupling capacitors should be mounted as close to the IC to be decoupled as possible and right over (or close to) the connecting vias. Multiple vias should be used for each end of the capacitor to further reduce series inductance. More on PDN design may be found in the reference section.[8-10]

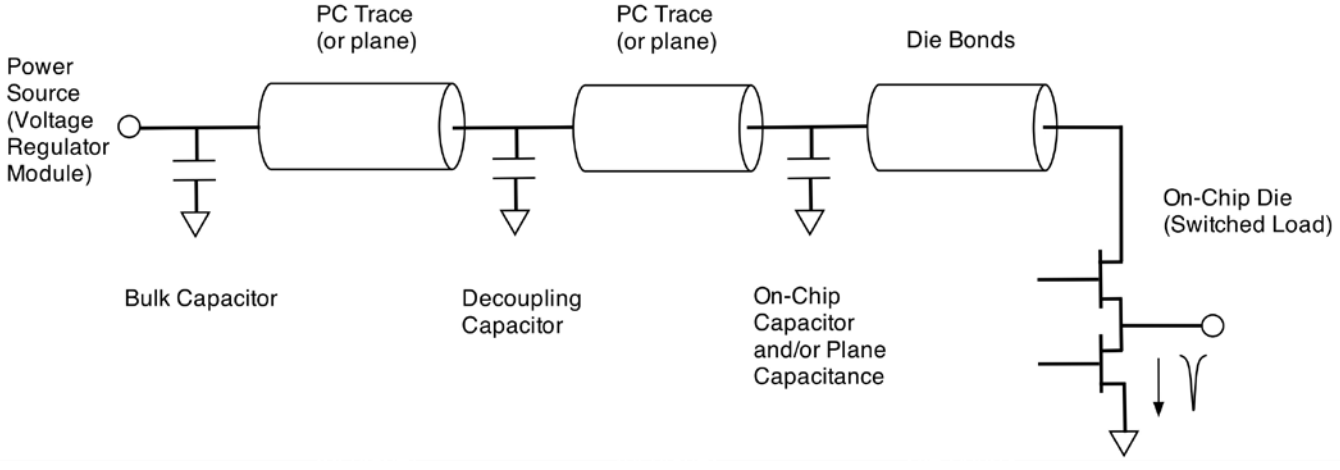

Figure 13: A typical circuit model of a power distribution network (PDN).

5. Shielding Design

The two issues with shielded enclosures are getting all pieces well-bonded to each other and to allow power or I/O cable to penetrate it without causing leakage of common mode currents. Bonding between sheet metal may require EMI gaskets or other bonding techniques. Figure 14 shows a handy chart for determining the 20 dB attenuation of a given slot length. For example, if a product design requires at least a 20 dB shielding effectiveness, then the longest slot length can be just one-half inch.

Slots or apertures in shielded enclosures become issues when the longest dimension approaches a half wavelength. Figure 15 is a chart of wavelength vs. frequency. For example, a 6-inch (15 cm) slot has a half-wave resonance at 1000 MHz. Generally, ventilation holes should be patterns of round holes no more than 1/4-inch diameter. Patterns of slots may be used, but they should be no longer than a half-inch in order to preserve an adequate shielding effectiveness.

See References 11 and 12 for more detail on shielding.[11-12] Interference Technology also has a free downloadable 2016 EMI Shielding Guide with excellent information.[13]

Summary

Paying attention to these five product design faults will go a long way towards lowering the risk of EMI failure during formal compliance testing. Considering a proper EMC design early in project development will save tons of time and money in the end. **DESIGN007**

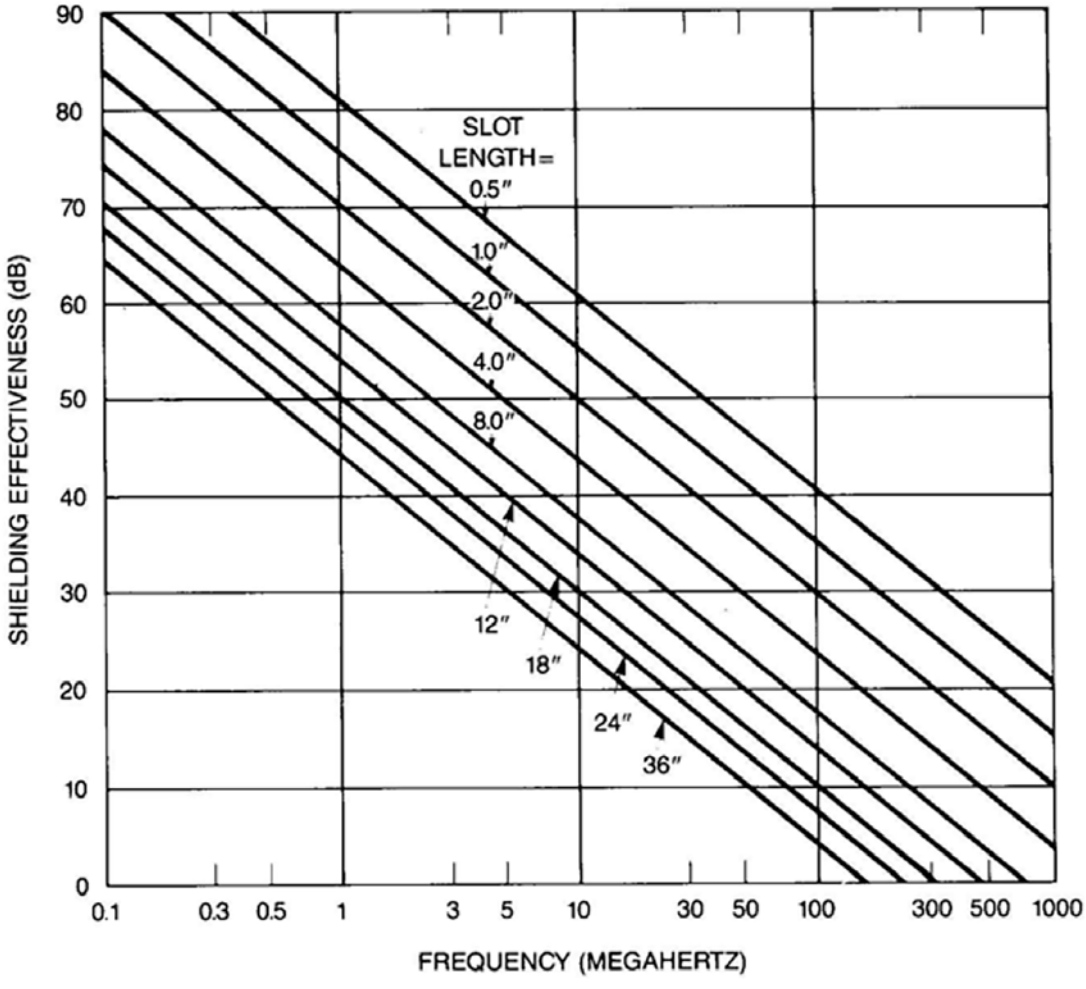

Figure 14: A chart of attenuation versus slot length. (Image source: Henry Ott)

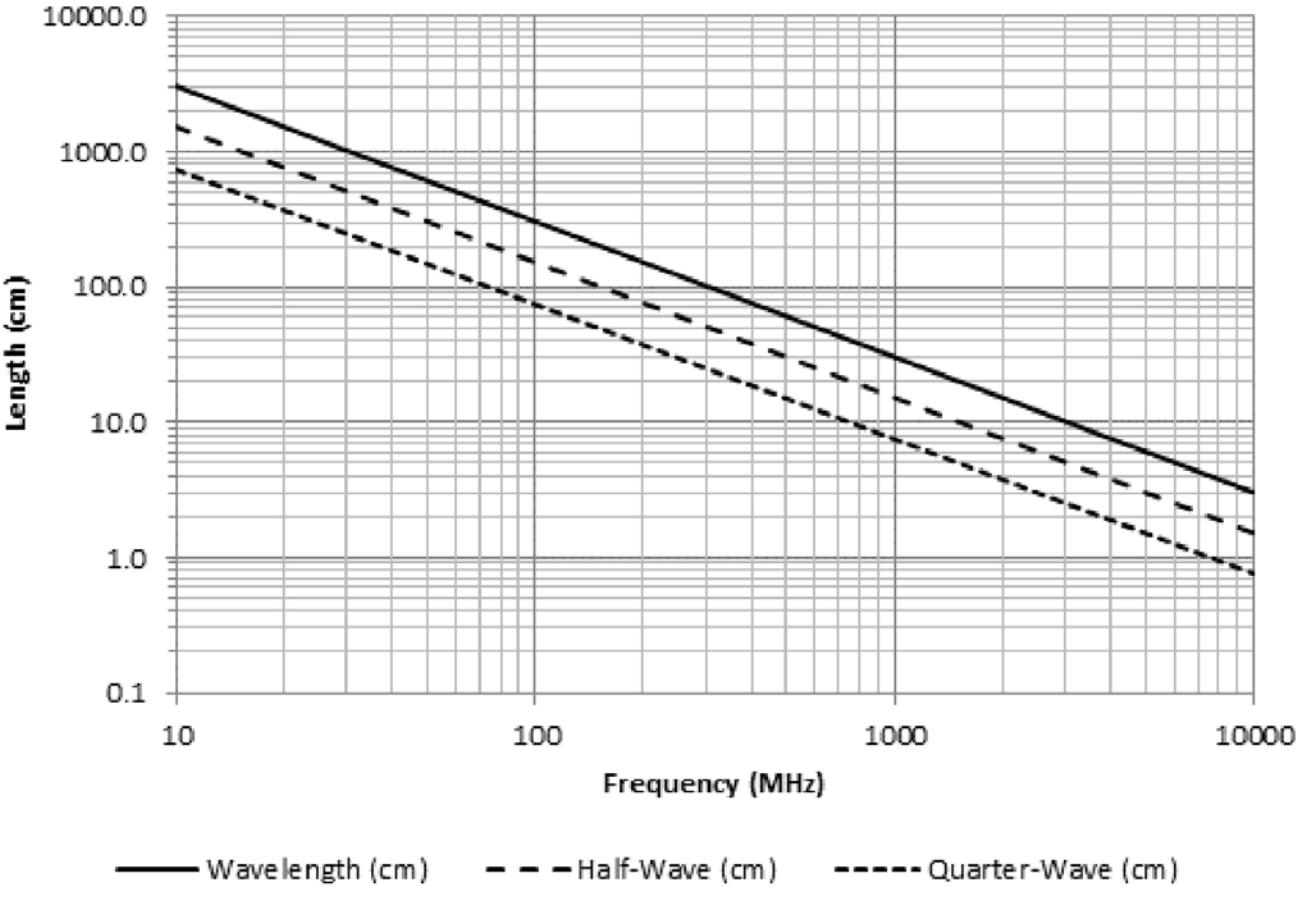

Figure 15: A handy chart for determining resonant frequency vs. cable or slot length in free space. Half-wavelength slots simulate dipole antennas and are particularly troublesome. (Image source: Patrick André)

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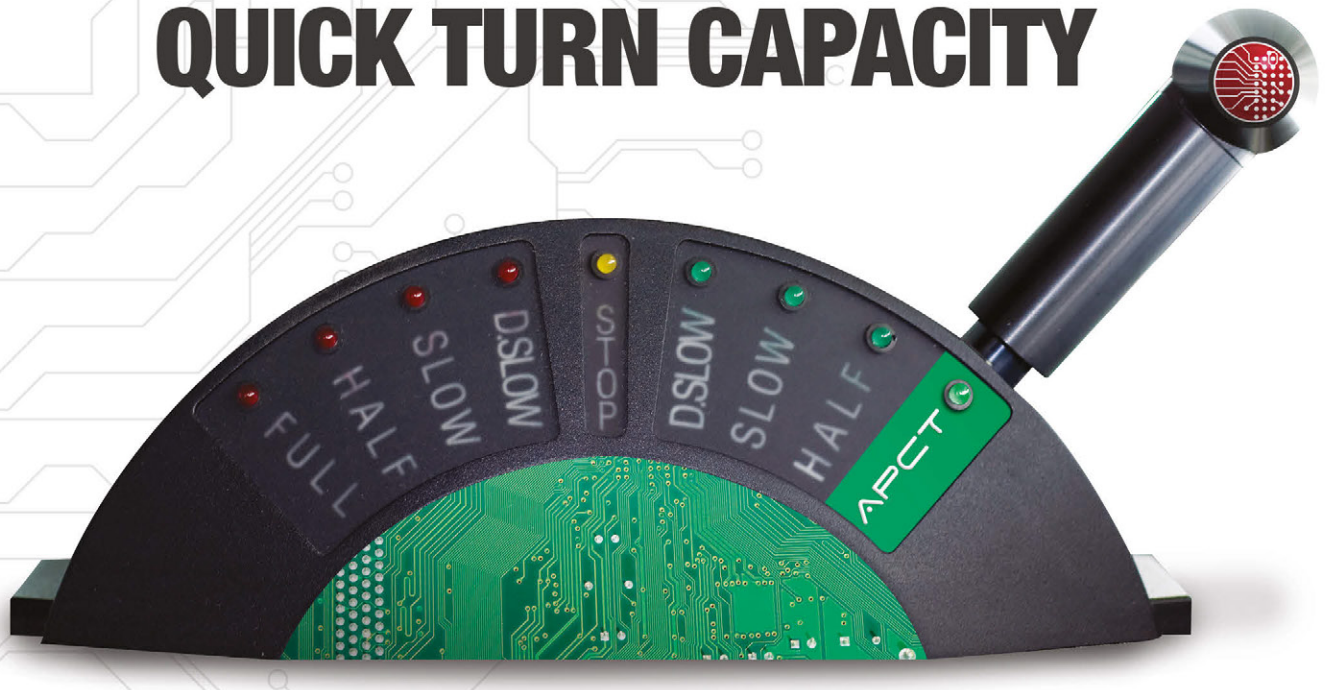

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A Closer Look at Surface Finish

Connect the Dots

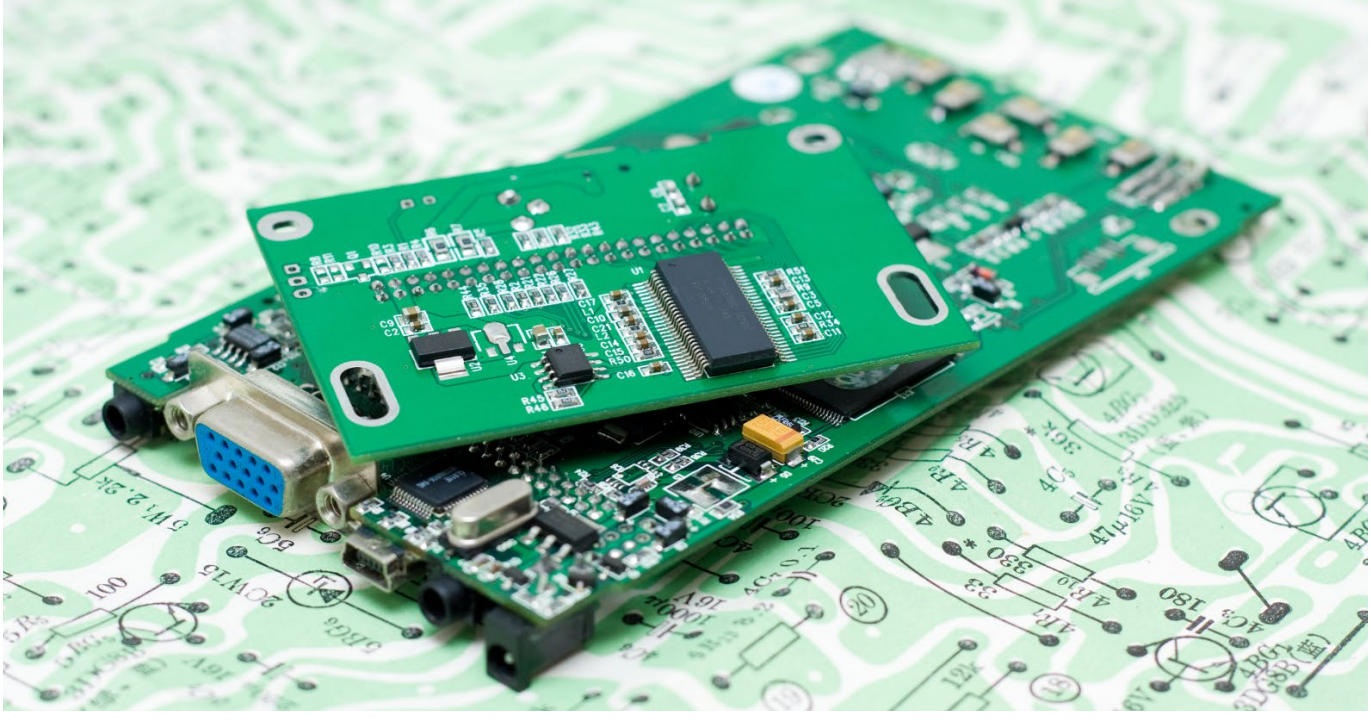
by **Matt Stevenson,** SUNSTONE CIRCUITS

The final surface finish of a PCB is an important consideration. This coating between your components and the bare board is applied to ensure solderability and protect any exposed copper circuitry. Selecting the right type of surface finish can be daunting, and for good reasons.

Designers need to consider whether the selected surface finish will provide an adequately reliable solder connection for the application. Is it the best fit for the type of components used in the design? Is it cost effective? Does it meet compliance requirements like the Restriction of Hazardous Substances Directive (RoHS) and the Waste Electrical and Electronic Equipment (WEEE)?

There are many choices out there and some are better than others at meeting each of these needs. Today, we will explore three of the most common surface finishes—examining how they are applied in manufacturing and looking at the pros and cons of each.

Once your board has been processed through solder mask and silkscreen, it is ready for surface finish application. At this stage of production, the PCB is fully functional, at least in theory. The solderable surfaces are copper. In an open environment, an oxidation layer will quickly form, keeping the solder from doing its job. That's why we apply a surface finish like solder, immersion silver, or electroless nickel immersion gold (ENIG) to protect the copper



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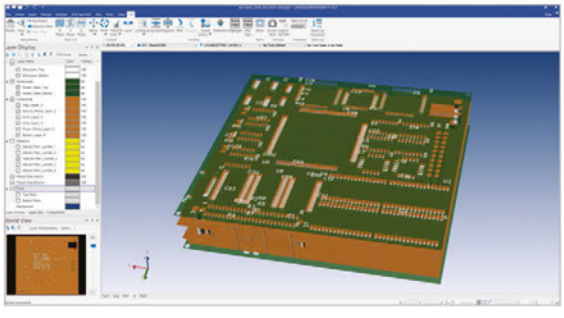

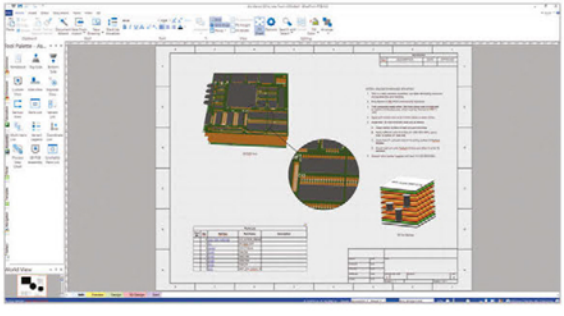

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from oxidation and corrosion, as well as give the assembly a nice solderable surface for your parts.

Solder

Solder application is typically done through a hot air solder leveling process, frequently called HAL or HASL. Historically one of the more popular surface finishes because of its durability, manufacturability, and cost effectiveness, the process can leave uneven surface finishes and is not suitable for fine-pitch components. For many applications, solderability is a higher priority, making this process a battle-tested choice for manufacturers.

The process begins with cleaning the copper surface chemically and presenting a fresh copper surface for all the solderable pads and holes. A layer of flux is added to the panels to further clean the copper. The flux also alters the surface tension of the molten solder which helps during the soldering process.

The freshly fluxed panel is then immersed in a pot of molten solder where the solder coats the copper surfaces, creating an intermetallic bond. After dwelling in the pot of hot liquid solder for a few seconds, the panel is rapidly pulled out and passed between two high pressure air knives which blow off excess solder and level the deposit on the surface. The panels are cooled, washed, inspected, and moved on to the next step of the production process.

Though not the perfect choice for every application, there is a reason this process has been used for many years. It produces a good quality product that makes assembly smoother, especially for through-hole parts. After all, nothing solders quite like solder.

Immersion Silver

Immersion silver is a chemically applied surface finish. While more expensive than solder, it has become a more popular choice since it is RoHS and WEEE compliant. It's also an ideal choice for fine pitch components.

The process also starts with a good cleaning of the copper surface. This time, the cleaned panels are immersed in the silver bath. Through the magic of chemistry, specifically a displacement reaction, copper atoms across all the surfaces are effectively displaced with a silver organometallic compound. It is a very efficient and effective reaction that produces a surface as planar as the copper deposit below it. After the reaction has completed, the panels are rinsed, dried, inspected, and moved to the next step of the process.

It's important to recognize during this stage of production that the immersion silver panel can be sensitive to contaminants and environmental conditions, and it should be packaged as soon as possible.

ENIG

ENIG (electroless nickel and immersion gold) is another chemically applied surface finish that is done by immersing the panels in several chemical baths. It offers a double layer metallic coating. Nickel serves as both a barrier to the copper and a surface to which components are soldered.

In this process, the panel surface is again cleaned to create a pristine copper layer where we will apply the ENIG deposit. Unlike immersion silver, the first chemical step is an electroless deposition reaction from the electroless nickel (EN). In this electroless deposition reaction, nickel ions in the solution are chemically reduced (autocatalytically) to nickel metal and deposited directly on the copper surface and subsequent nickel deposits. This deposit can be built up to a thickness capable of protecting against copper migration.

Once the nickel deposit has been applied and rinsed, it quickly moves to the immersion gold (IG) part of the process. This reaction is similar to the immersion silver process above as it is a direct displacement reaction, displacing the nickel atoms in favor of the gold layer. After the reaction is complete the panels are rinsed, dried, inspected, and moved to the next step in the process.

ENIG offers a surface finish that is ideal for complex surface components that cannot tolerate uneven surfaces. It is also lead-free and durable. The process can be more expensive and comes with some risk. Phosphorus has been known to build up between the gold and nickel layers, sometimes resulting in fractured surfaces and faulty connections, often called black pad. Many of the newer chemistry formulations have all but eliminated this possible defect.

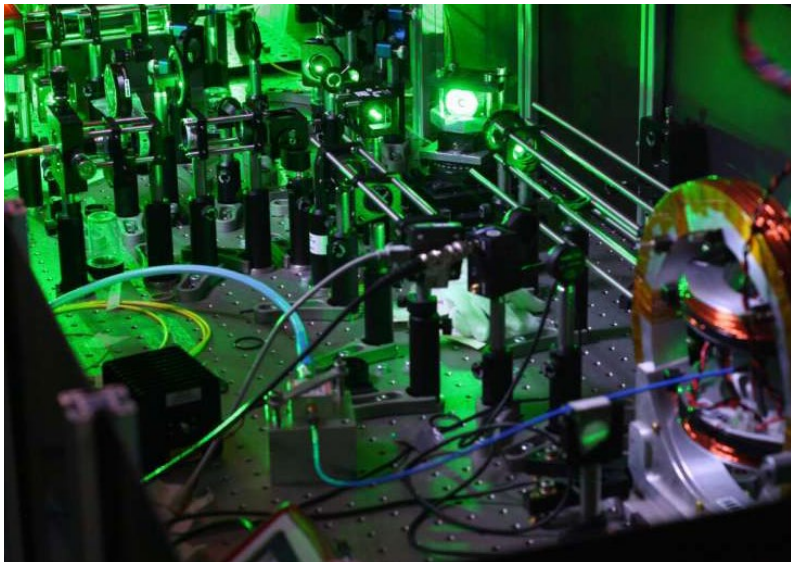
Whether your priority is cost-effectiveness, manufacturability, compliance, or some combination of the three, any of these surface finishes will allow a good solder joint to be formed. Which method you choose will be a function of your application's requirements. **DESIGN007**

Matt Stevenson is the VP of sales and marketing at Sunstone Circuits. To read past columns or contact Stevenson, click here.

Machine Learning Algorithm Helps Unravel the Physics Underlying Quantum Systems

Scientists from the University's Quantum Engineering Technology Labs (QETLabs) have developed an algorithm that provides valuable insights into the physics underlying quantum systems—paving the way for significant advances in quantum computation and sensing, and potentially turning a new page in scientific investigation.

In physics, systems of particles and their evolution are described by mathematical models, requiring the successful interplay of theoretical arguments and experimental verification. Even more complex is the description of systems of particles interacting with each other at the quantum mechanical level, which is often done using a Hamiltonian model. The process of formulating Hamiltonian models from observations is made even harder by the nature of quantum states, which collapse when attempts are made to inspect them.



In the paper, "Learning Models of Quantum Systems From Experiments," published in Nature Physics, quantum mechanics from Bristol's QET Labs describe an algorithm which overcomes these challenges by acting as an autonomous agent, using machine learning to reverse engineer Hamiltonian models.

The team developed a new protocol to formulate and validate approximate models for quantum systems of interest. Their algorithm works autonomously, designing and performing experiments on the targeted quantum system, with the resultant data being fed back into the algorithm. It proposes candidate Hamiltonian models to describe the target system, and distinguishes between them using statistical metrics, namely Bayes factors.

Excitingly, the team were able to successfully demonstrate the algorithm's ability on a real-life quantum experiment involving defect centres in a diamond, a well-studied platform for quantum information processing and quantum sensing.

"This level of automation makes it possible to entertain myriads of hypothetical models before selecting an optimal one, a task that would be otherwise daunting for systems whose complexity is ever increasing," said Andreas Gentile, formerly of Bristol's QETLabs, now at Qu & Co.

(Source: University of Bristol)

My Top Six Design Challenges

The Bare (Board) Truth

Feature Column by Mark Thompson, CID+, MONSOON SOLUTIONS

Greetings! This month, I'm offering my top six design challenges, with some additional feedback from Jeff Reinhold, one of the owners at Monsoon Solutions.

Narrowing it down to the top six was tough, because there are so many challenges for today's board designers—from incomplete information and footprint generation to power routing constraints. These are just some of my thoughts and is by no means a complete list of all of today's design challenges. Every designer has his or her own challenges; what is easy for some may be a challenge to others. I will be interested in reading the different approaches to this topic. Here's my countdown:

Jeff Reinhold

#6: Inaccurate or Less Than Helpful App Notes or Part PDFs

As a board designer we are constantly referring to component datasheets and app notes for information helpful to layout and design. Many of these datasheets are very short and do not have enough information regarding device layout; they may have some technical app notes and a pinout but little information other than that relative to board design. Even worse, some are over 300 pages long, and most of the information is more relevant to an EE than to a board designer, thus requiring the designer to weed through the mountain of data to glean what they really need.

In my short time as a board designer, I have seen both. Many do show layout solutions and design suggestions, but some are not really the best way to place the parts such as resistors and capacitor location suggestions. So why are these datasheets so often misleading or less than helpful? Here are some possible reasons:

- Understanding that everything is application-based and the engineer writing these app notes cannot possibly cover every contingency plan or every possible application.

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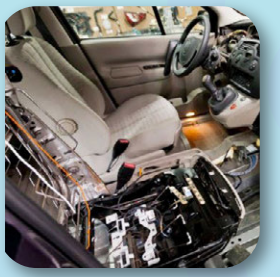

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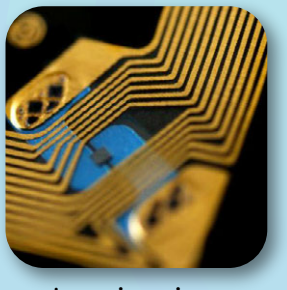

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- There may be left out or missing information. Here you should seek a second or third source to find the information you need.
- Misprinted information. This one is quite common. Frequently the datasheet itself was translated from its original language and as we all know, this can result in sentences that make no sense, with some that are downright hilarious.
- There could be measured data that was misinterpreted and therefore useless to anyone looking to use that information.

Due diligence on the part of the designer is always required. Know what you want, what your customer wants, and how to get it.

Due diligence on the part of the designer is always required. Know what you want, what your customer wants, and how to get it. This requires amassing information about your design's purpose.

At Monsoon Solutions, we do this in a "kick-off" meeting with the customer to ask specific questions. We cover things like power needs, mechanical constraints, fixed components, and thermal considerations, just to name a few, Even the best laid plans do not always cover everything you need to know about your design in the kick-off meeting, and follow-up conversations are usually necessary. Do not be afraid of asking more questions (within reason) to get your design right.

I also encourage you to learn and read more. Of course, be careful not to believe everything you read, either online or in print. Testing everything you read to prove the concept to yourself sometimes means you will also have to prove it to the customer. Be ready for that.

#5: Large PMICs

A power management IC is a power IC solid-state component that distributes the required measure of voltage to all other parts, which is usually accomplished using a low on-resistance MOSFET placed between the source and the load. The PMIC controls the MOSFET and thus its resistance. The PMIC manages the turn on/off rate by timing these MOSFETS, one per rail. It's typically used in battery operated devices such as cellphones, laptops, and portable media players to decrease the amount of space required due to limited board real estate.

About this, Jeff Reinhold said:

"The reason I put PMICs above other circuits is we typically get a lot of information on how to lay out certain circuits (not just PMICs), including impedance, length, matching, clearance, and placement info. In addition, there may be pictures of completed placement/routing and even reference boards. The more complicated the circuit, the more information we might get. Very often, the parts and connections we have don't match the input(s) exactly. It may just be that parts are sized differently, but very often the circuit is slightly different as well.

"For anything that isn't a large PMIC, if I follow the input well, there is a good chance I won't have to change anything after it gets reviewed and/or simulated. If I do, it's typically minor. That has never happened with a large PMIC (small ones are easier to get right on the first try). I had one instance where I was able to follow the reference/input very closely and I thought it would be good, but it still needed some difficult work to get it right. Adding or moving caps and trying to squeeze more copper area or vias is often not easy to do in crowded areas."

#4: 'Scale' or Available Space for Design

Many times as designers, we run into restrictions on available space and board real estate issues, based on a number of things, such as the number and size of components needed for a given design. I can tell you that looking at

the available space where all the components are to be placed, and then looking at the extent of the board itself, can be daunting on some very small boards; remember that most boards (without having to go to truly embedded components to minimize de-coupling caps, for instance) only have their external layers available to be populated with components.

In many cases the customer may not want any components on one side or the other, further limiting the available space. Perhaps the back side must lay flat against another board.

Components cannot be simply placed wherever they fit on a given design—for example, bypass caps that need to be as close to the power pin they are associated with. In a low frequency/DC context, a bypass cap opposes changes in the voltage line by charging or discharging. The capacitor functions like a low impedance battery that can supply small amounts of transient current. In a high frequency context, the capacitor is a low impedance path to ground that protects the IC from high-frequency noise on the power line.

Consider also trace and space limitations based on power functions: The greater the power the greater the voltage; this requires wider tracks that also eat up board area.

Assembly also eats up board space. Auto insertion devices can place components extremely accurately, but they still require enough room to operate in. In addition, parts that cannot be placed by automated placement equipment must be hand placed, requiring additional space for the technician and access to get his or her fingers (or tools) within. An example would be devices such as switches or connectors. Additional space is also required for de-bugging or reworking by the technician.

IPC has some great information on guidelines for space such as IPC 2221B—the spec that deals with design—and it has solid information on voltage spacing and other electrical considerations.

- **IPC-A-610:** This is the generic acceptability/rejection spec and covers how hardware is to be assembled onto PCBs.
- **IPC 7351B:** This is the land pattern spec for surface mount parts with details on pad size and spacing pertaining to PCB design.

Finally, test—namely test point access—must also be considered. There needs to be enough room to probe the test points.

#3: Information Not Initially Covered by the Customer and Changes on the Fly

This one is inevitable and generally happens after the board has gone back to the customer for part placement and/or final route review. It might be information either not shared by the customer in the kick-off meeting or information you as the designer did not ask about. Frequently, previously unforeseen things pop up and need to be dealt with. Additionally, there may be some feedback from different engineers on the project; mechanical and power engineers may have different ideas on what they would like to see or imagine they would like to see from the design. More on this topic later.

In conjunction, there may be physical changes that the customer may require, such as new components due to part availability or part obsolescence. This one is quite common as components can be hard to find and a substitute must be used. It is the board designers' responsibility to incorporate these changes with a minimal effect and loss of time.

#2: Requests for Things that 'Don't Play Well Together'

What I mean by this is things like small/tight pitch BGAs with high copper for high current. Sometimes the customer wants things that are just not possible from either a design or fabrication standpoint; for example, three- or four-ounce finish with 0.003"/0.003" trace and space, or very tight pitch components with

space not adequate between SMD pads to be able to have higher copper. These both happen frequently and must be leveraged to have a good design solution.

Those of you who have read my columns when I worked in board fabrication know this is something I feel strongly about and is a bit of a soapbox for me. Even 0.003"/0.003" trace and space on a half-ounce foil to start can be a fabricator limitation. Some fabricators will then ask to start on one-quarter or 3/8th-ounce foil to be able to deal with the trace and space that low, remembering that starting on even a half-ounce will require a half-mil etch compensation, taking the space down to 0.0025". At this point, most fabricators require starting on the lighter copper weights of either quarter or 3/8 ounce. These are such light copper weights that most fabricators' etchers can easily etch that thinness of metal without an additional etch compensation digging into the available space.

Finally, by far the most important...

#1: Reading Our Customers' Minds

About this, Jeff Reinhold said:

"We often have many inputs to deal with. Some are more difficult to decipher than others, but if they are available, we can read them. What we can't read is our customer's minds. When we get right down to it, this is what our job is—create data that can be used to build a circuit board, and that meets or exceeds our customer's expectations for how that should be implemented (i.e., read the customer's mind). I used to say that there are 500 ways to lay out a board and all of them will work, but only one of them fits what is in the customer's head. That is still true but now the number is probably more like 20 than 500."

In short, good design makes a product useful. It has to satisfy certain criteria—not only the functional, but also the psychological and aesthetic. Good design emphasizes the usefulness of a product while disregarding anything that could possibly detract from it.

Jeff continues:

"Our customers invariably have some picture in their head (or collective heads) of what they think the layout should be or will look like. Not only do we have to figure out what that is, via additional conversations or use of the tools at our disposal, we must balance that with our own knowledge of best practice for the given circuit and our customer's ideas on implementation, and then be able to create something that meets their expectations, even if it must be something different than what they thought it would be."

Jared Spool, the American writer, researcher and usability expert, said:

"Good design when it's done well, becomes invisible. It's only when it's done poorly that we notice it."[1]

Another favorite quote about design comes from Steve Jobs:

"Design is not just what it looks like and feels like. Design is how it works."[2]

But my favorite quote comes from "Wind, Sand and Stars" by Antoine de Saint-Exupéry:

"A designer knows he has achieved perfection not when there is nothing left to add, but when there is nothing left to take away."[3] **DESIGN007**

References

1. Lesson From A Good Bad Design.
2. "The Guts of a New Machine," The New York Times Magazine, Nov. 30, 2003.
3. "Land of Men," Antoine de Saint- Exupéry, 1939.

Mark Thompson, CID+, is a senior PCB technologist at Monsoon Solutions Inc. To read past columns or contact Thompson, click here. Thompson is also the author of *The Printed Circuit Designer's Guide to... Producing the Perfect Data Package.* Visit I-007eBooks.com to download this book and other free, educational titles.

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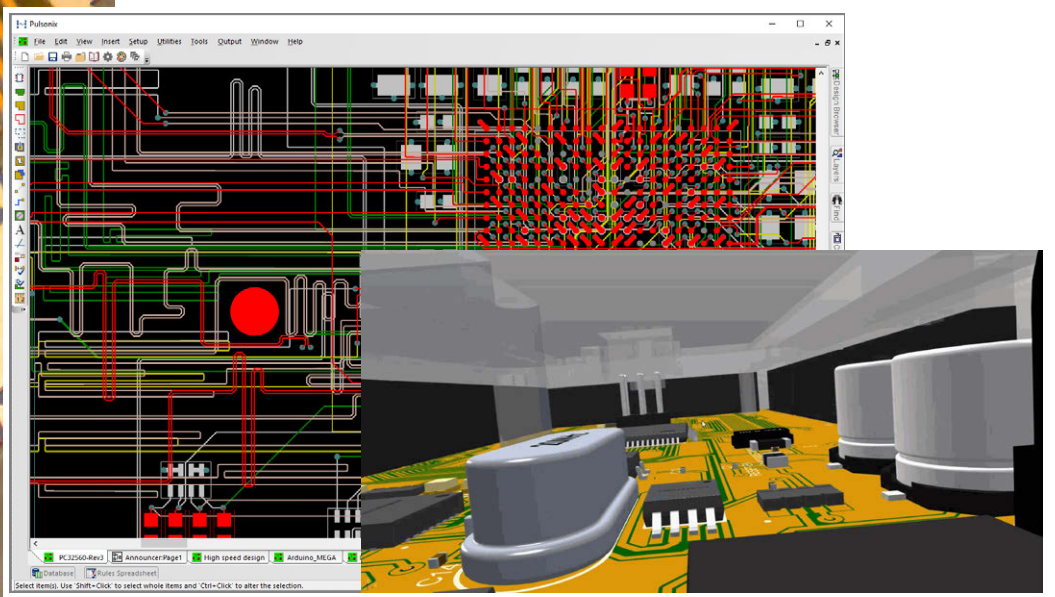

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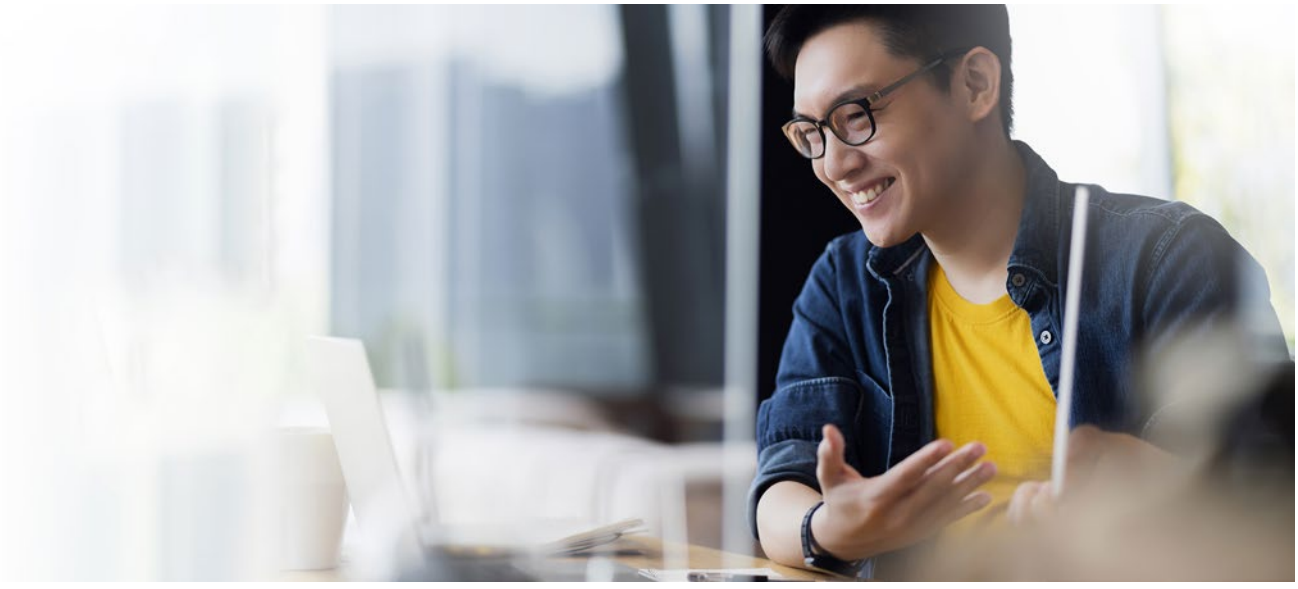

Planning and Communication: Key to Optimizing Your Design Time

Feature Article by Chris Young
THE GOEBEL COMPANY

How many times in your career have you been asked, "Can we pull in the schedule?" Whenever you hear that question, can't you feel the hair on the back of your neck standing up?

This type of question can be hard for us to hear simply because it is the wrong type of question. The core issue, most often, is how to best use our time during the design phase of a project. Optimizing design time consists of managing internal and external elements within our control and influence. Internal factors we have control over are our skills, time, and behavior. External factors we have influence over are requirements, design reviews, and stakeholder interactions.

Personal skill management is the foundation of being an effective designer. The more ideas and methodologies that you encounter/use, the more depth and breadth of knowledge you will have to make well-informed decisions. Here are two general rules of thumb to help guide personal skill development regarding design efficacy.

1. Generalists should be well versed enough to convey requirements, design decisions, and interdisciplinary tradeoffs to specialists.

Early in my career I was working on a project designing a mixed digital/analog IO board and needed to communicate to the power supply engineer what my power requirements were for my board. The good news was I had a previous design to base my design on and could take measurements from that board to give a reference. The bad news was I did not know what was important to communicate to the power supply designer. I took average voltage/current measurements, added some fudge factor and handed them over to him. He asked me how I got the numbers, and I replied that they came from the previous design—with additions based on increased circuitry on the new design. The measurements I made were static and did not account for any dynamic power draw.

It turns out the -15V had an average current draw of tens of milli-amps and a peak of nearly

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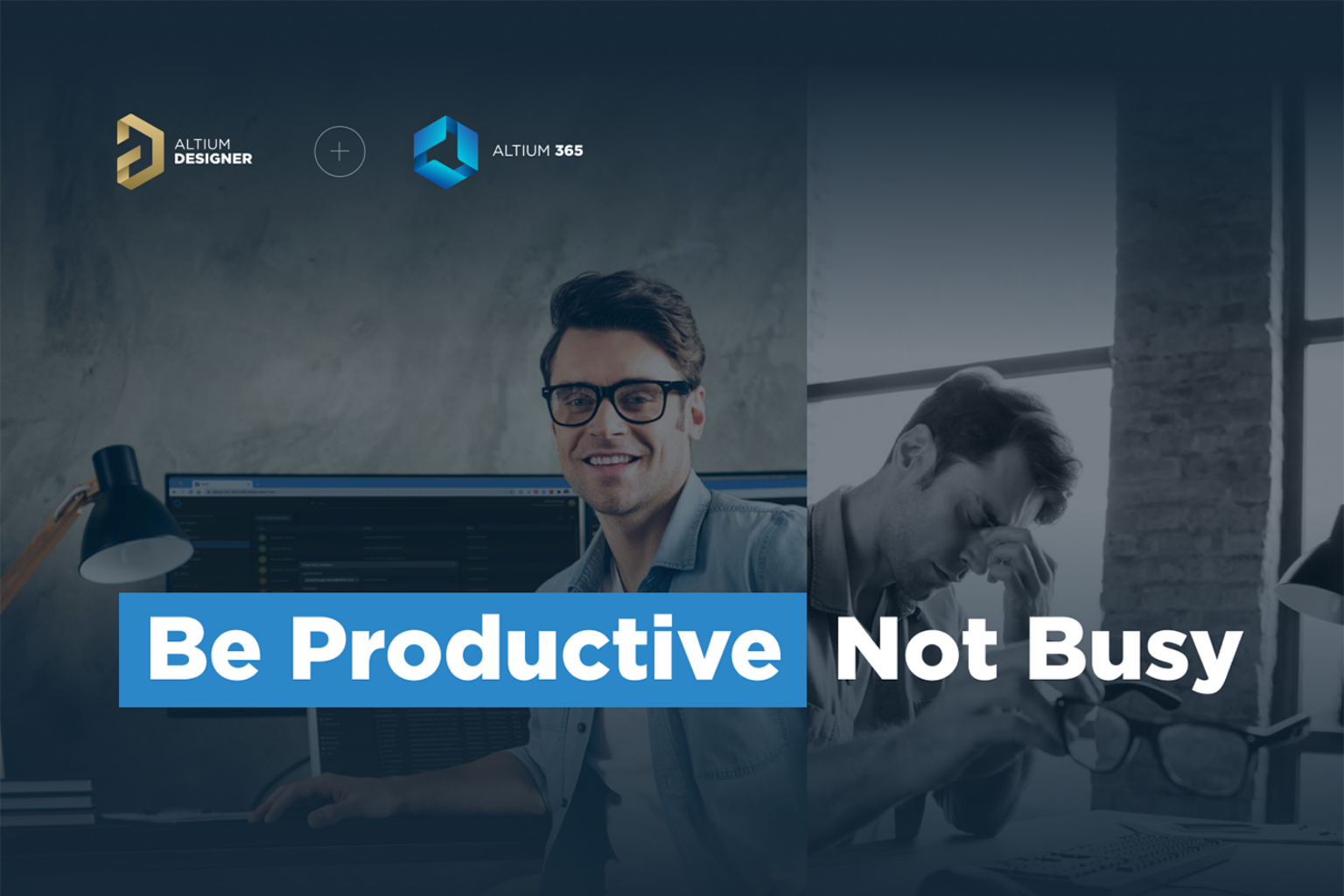

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500 mA. The power supply engineer designed a cross-regulated power supply with two outputs: +15V and -15V. The power supply regulation was based on the +15V since its current draw was about two orders of magnitude that of the -15V. When the -15V was hit with sourcing 500 mA, it would sag significantly. The power supply monitor would then indicate a fault and the associated circuitry on the processor IO board would not work as required. The result was a re-design of the power supply due to my lack of understanding of what the specialist (power supply designer) needed from me.

2. Specialists should know the boundaries of their expertise and how to communicate requirements, specific implementations, and design decisions to generalists.

I once observed a high-power RF design specialist learn how to code in Visual Basic to show an FPGA designer how to set a digital potentiometer (used for transistor biasing) during different high-power transmission scenarios. He put together a rudimentary setup and showed the FPGA designer on a logic analyzer what needed to happen during each specific scenario. The design integration went off without a hitch and no design modifications were needed for either the RF power amplifier or the associated FPGA code modules.

3. Make time to learn new skill sets and keep your skills sharp and current. Become an avid collector of rare gems and golden nuggets of information.

Time management is a critical factor in being an efficient and enduring designer. Partition and budget the time you need to do your work in a manner that you can sustain. Who likes to start and/or end a project with a death march? I remember being told as a young engineer "What doesn't kill you makes you stronger," and I lived this mantra in my 20s and early 30s. I was pulled aside in my mid-30s by one of my mentors and was given the following advice: "As you age, what doesn't kill you wears you down."

There are a lot of time management programs out in the world today. Pick one, try it for six weeks, and if it does not work, pick a different one and try, try, try again. Do not give up until you find one that works for you. Use key performance indicators to evaluate your time management strategy's effectiveness. Are you completing your tasks on time? Are you satisfied with your performance? What are your energy levels? Let us agree we want to develop practices and processes which make us more efficient designers.

You Get More Bears With Honey

We must have control over our own personal behaviors. Regardless of your feelings, do not criticize, stonewall, or be contemptuous with others. There is a difference between complaining or questioning and being critical. Criticism manifests itself in comments like, "You are wrong. This is incorrect. That is not right." Instead, try saying, "I'm not sure this is correct; can we take a closer look at it?" Appropriate questions and complaints will allow you to work out an issue or problem with a teammate without causing them embarrassment or to be defensive.

Stonewalling usually ends up isolating teammates or yourself and cutting off essential communication needed in a design project. How can you be effective if you are not communicating with the others in your team?

The short answer is you're not. By far, the most harmful behavior I have encountered and engaged in is speaking with contempt, either interpersonally or rhetorically. Contemptuous speech can come out as, "I can't believe someone did this. Why on earth would you do this? My way is the only way to design this circuit." It also can manifest itself in the tone of voice you are using or the expression on your face. I was once asked to participate in review of a project and the lead engineer made the following comment about a list of my questions

regarding the product's power dissipation: "If you need to ask these questions, then you don't know what you are doing." This statement was made as a manner of posturing himself as the lead and to discourage others from questioning him.

I spoke up and indicated these power dissipation questions were directly related to the standard size envelope the product could fit into. These questions were ignored, and the product was designed to fit in the smallest form factor possible. In the end, the product design failed because of several fatal flaws: The product's peak power dissipation exceeded its size envelope, and there was no room in the customer's application for the product to increase in size. The worst-case outcome had occurred, the design was not viable, and thus had an earned value of zero.

You get zero points for optimizing your design time if your design fails. Work hard to behave in a manner that is generally respectful to others around you, because it helps foster productive communication and cooperation in your design team. I understand this can be extremely difficult at times, but I also believe that the rewards of being a more effective team outweigh any short-term euphoria from telling someone off, stonewalling, or self-posturing.

Understand the Requirements

Crucially, we have influence in the design process over the requirements upon which we base our designs. It is important not to gloss over this step in the process to work on implementation. A well written requirement is something that is needed, can be verified, and is reasonably attainable. A requirement should only be issued based on items like customer needs, marketing analysis, regulatory requirements, and internal/derived needs.

Requirements really need to be verifiable. How do you demonstrate to a customer or regulatory entity that you meet a requirement if you cannot verify it? A requirement is also no good if you cannot make it happen within the constraints of the project. Can you implement the design requirement within schedule? Is the requirement technically infeasible or made of unobtanium? Well-written requirements reduce assumptions made by designers and consequently reduce project risk. As I've heard many times from seasoned systems engineers, "An ounce of good requirements is worth a pound of re-design."

Design reviews are another area in which our designs can be helped or hindered. First and foremost, take your design reviews seriously and do not turn them into a rubber stamp approval session. You should have a panel of appropriately selected stakeholders present based on the level and type of review. Review topics should show how the design meets the requirements—or does not.

Do not omit the issues/problems with your design in your reviews. This can be a great opportunity to get help from another colleague or at least demonstrate to management that you need additional resources. Also, do not let a reviewer stonewall you with disapproval during a meeting. It is not helpful if someone disapproves of your design without giving you reasons that can be related back to the requirements, measured, or demonstrated. A successful design review should demonstrate the design meets its applicable requirements, design changes are needed, or course corrections need to be made in terms of scope, schedule, or cost.

Speak Your Managers' Language

Effective communication to your design stakeholders reduces delays in resource acquisitions. First, do not assume that other people are specifically aware of what you are doing and what you need. For example, let's assume you need a logic analyzer to verify the timing of waveforms produced by an FPGA in your design and the scope of work needed justifies your need to purchase one. You were able to get the instrument on the approved capital expense list and filled out the purchase request

stating your specific need. As your project moves forward, you notice your purchase requisition has not been approved and all inquiries indicate it is and has been at the desk of the vice president of your organization for some time now. Why has it not been signed? You were very specific about what you needed and why.

The reason: You did not communicate to your VP in a way that VPs make decisions. A lot of companies use key performance indicators (KPI) at higher levels of management to measure the status of a project. A vice president is typically responsible for general oversight of multiple projects and company initiatives and typically uses KPIs to help make decisions. Two common KPIs are the schedule performance index (SPI) and cost performance index (CPI). I suggest having justifications that are relevant to the stakeholders from whom you are seeking approval. You have to speak their language, so to speak.

A justification for a purchase requisition requesting approval from your direct manager, director, and vice president may look more like the following: "Purchase of a logic analyzer is needed to verify FPGA design requirements on project X. Purchase and delivery of this item is needed by mm/dd/yyyy to maintain projected project SPI and will not affect project CPI as it is a planned expense. Please see attached references to capital expenditure approval list, item number TBD and project schedule X."

In conclusion, optimizing design time is about effectively managing internal and external elements of the design process. It is a journey about self-improvement and becoming more influential. Don't forget to bring your maps, compass and a handy-dandy metal detector. **DESIGN007**

Chris Young is owner/lead engineer of Young Engineering Services LLC and chief hardware engineer at The Goebel Company.

Canon Medical Expands AI-Based Image Reconstruction Technology

Canon Medical is bringing the power of accessible artificial intelligence (AI) for improved image quality to more patients with expanded clinical indications for 3T MR. Advanced intelligent Clear-IQ Engine (AiCE) Deep Learning Reconstruction (DLR) can now be used for 96% of all procedures using the Vantage Galan 3T MR system, expanding from previously FDA-cleared brain and knee indications to a vastly larger number of clinical indications, from prostate to shoulders, including all joints, cardiac, pelvis, abdomen and spine.

AiCE was trained using vast amounts of high-quality image data, and features a deep learning neural network that can reduce noise and boost signal to quickly deliver sharp, clear and distinct images, allowing clinicians to boost image quality, performance, productivity and throughput on a whole new scale.

"With this expansion of AiCE, Canon Medical now offers advanced AI technology on its 1.5T and 3T MR systems," said Mark Totina, managing director, MR Business Unit, Canon Medical Systems USA Inc.

As part of the original AiCE Challenge, radiologists and technologists were asked if they could tell the difference between images taken on the Vantage Orian 1.5T system using AiCE with standard 3T MRI images with the same acquisition protocol for both scanners. Half of the time respondents had difficulty differentiating between 3T images without AiCE and Orian 1.5T images with AiCE applied. This next phase of the challenge will focus on body imaging, where the previous challenge focused on brain and knee images. (Source: Business Wire)

Design problems solved!

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DDR Routing—and Other Big Fish in the Lake of Technology

Tim's Takeaways

by Tim Haag, FIRST PAGE SAGE

If I can pull you away from your latest layout for just a moment, I would like to tell you a fish story. We have heard tales about the "big one that got away," but here's one about the "big one that got away that I never saw." Does that sound intriguing? Well, here's what happened:

Many years ago, a friend and I went out of our way to try the fishing at an obscure lake somewhere in southern Oregon. There weren't many people there, locals mostly, and they were all fishing from a tall platform that extended into the lake. I don't know what the platform was used for, but we joined them on it anyway. The folks there were pulling in fish after fish, but we weren't having any luck at all. After a couple of hours, we finally decided to throw in the towel and call it a day. As I was pulling my line in, I was furthered annoyed to discover that it had snagged, so I started pulling harder to free it up. Imagine my surprise when the line started pulling back. I wasn't snagged; instead, I had hooked into a really large fish.

Trying to be as gentle as possible, I started reeling in my line while slowly backing away from the railing. All this commotion caught the attention of the other people on the platform, and they quickly gathered around our spot for a better view. As the fish came within reach, my friend could see that the hook was precariously set, so he grabbed the line to swing it in over the rail. This proved to be too much stress on the line unfortunately, and the fish tore loose from the hook and plunged 25 feet back down toward the water. With my view completely blocked by all the people gathered around the railing, I didn't get to see any of this—includ-

PCBs are complex products which demand a significant amount of time, knowledge and effort to become reliable. As it should be, because they are used in products that we all rely on in our daily life. And we expect them to work. But how do they become reliable? And what determines reliability? Is it the copper thickness, or the IPC Class that decides?

Every day we get questions like those. And we love it. We have more than 490 PCB experts on 3 continents speaking 19 languages at your service. **Regardless where you are or whenever you have a question**, contact us!

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ing seeing the fish. I did, however, hear their collective "gasp" when the fish tore loose, followed a moment later by what seemed like the loudest "kerplop" in recorded history as this Moby Dick-sized fish hit the water. This was a sad final salute from the biggest fish that I almost caught, but never saw.

The locals were very sympathetic for my loss, describing in agonizing detail how that fish had been one of the largest they had ever seen, while ripping my friend a new one for grabbing the line too aggressively. I have always felt bad for him because he really was trying to do his best to help—but that's not going to stop me from sending him a link to this story. After all, a little fresh salt in the wound is good for the soul—said no one ever—but that is what friends are for. Right?

Anyway, there are two points to take away from this story, and the first one is to always bring a net with you when you go fishing. The second is more important—even though this particular fish got away, there's plenty more to be caught. After all, there is always a bigger fish.

This theme of "there is always a bigger fish" is very common in our culture and literature, as both Jonah and Ahab can attest to.

This theme of "there is always a bigger fish" is very common in our culture and literature, as both Jonah and Ahab can attest to. It also encompasses much more than just the realm of ichthyology, however, and can be applied to almost all areas of our lives. Take our industry of designing circuit boards, for example. No matter how much your latest design may have pushed the envelope of technology, there will always be another design that will present an even greater challenge waiting for you tomorrow. There's always a bigger fish.

I've been in the PCB layout business for a long time now. When I first started, we were laying out very simple boards with through-hole parts using 12-mil traces and spaces. I still remember vividly the first board that came through our department that required specific routing topologies and trace lengths. None of us really understood any of this at the time, and the designers assigned to the job instead created a beautiful layout with the best-looking bus routing you have ever seen; it was something the rest of us marveled at. All this hard work, however, was promptly rejected by the customer because even though it looked great, it wasn't going to come close to working the way it was intended to. We all went back to the drawing board and learned about measured lines, the proper positioning of terminating resistors, and how these trace topologies were really supposed to be connected. We were pretty proud of ourselves—until we got our first taste of DDR memory routing.

There's always a bigger fish.

Soon we became experts in what was required to successfully complete a design with DDR memory routing. We had to restructure our designs for the correct stripline layer configurations, as well as to allow enough room for all the escape routing. Component placement became more important than ever as we designed the entire signal path instead of just looking for the shortest connections between pins. We also learned very quickly how to work with different routing patterns such as T-topologies and fly-by topologies, as well as how to best tune our traces to achieve the correct signal timing. You would think by this point we would have deserved some well-earned pats on the back, but it was not to be.

There's always a bigger fish.

Whether it's hybrid designs, flex circuits, or something else equally intriguing, there will always be newer and more challenging circuit board technologies that designers will have

to learn and become fluent in. You may even find yourself having to refresh your knowledge of past design technologies that you haven't worked with for a while in order to satisfy the requirements of a new project. The key to all of this isn't so much in what you already know, but in your ability to quickly adapt, learn, and be ready for the next new design that will be coming your way. There's always a bigger fish, especially in our industry, so let's come up with some ideas on how to be ready to land the big one safely—without it getting away. Here are a few thoughts to use as a starting point:

Be Ready for Change

I realize that this sounds like a cheesy motivational phrase, but I know of several people who have missed out on some great opportunities because they weren't mentally prepared for it. Whether it's emerging design technologies or next-generation systems and tools, it's going to be different, and we've got to be ready. Sadly, many will avoid changes in what they are doing to stay with what they know and are comfortable with. Inflexibility can be a career-killer, though, and it's one sure way of letting the big one get away.

Rise Above the Fear

The thought of learning and doing something new can also bring with it a lot of fear. It is not at all unusual for this apprehension to build in our minds and make the task seem much more difficult than it really is. Yes, it may take some time, a lot of extra effort, and perhaps even banging your head against the wall a few times in frustration. With perseverance, though, you will be rewarded with another technological capability that you can add to your tackle box of design skills. Too often we spend time trying to convince ourselves that something can't be done, instead of just sitting down and doing it.

Keep Your Finger on the Pulse

To explore new ideas, you need to know what ideas are out there to explore. We are fortunate in our industry that there are many different resources that can help with this. Design007 Magazine, for example, explores a different industry topic each month, along with many other design-related subjects covered in its different articles and columns—and that is only one of the many resources available out there. With newsletters, white papers, seminars, classes, and conferences, there is no shortage of information on the newest design technology pools that you can fish from.

Expand Your Network

I would never have had the story about "the big one that got away that I never saw" to tell you if my friend hadn't suggested that we try fishing at that obscure little lake that I had never heard of before. Having people in your network that can expose you to new ideas and help you when you are stuck is essential to staying on top of your game. And I'm not just talking about other designers either; connect with anyone who can shine new light on a previously darkened area: customers, managers, competitors, friends, and experts from other industries as well. Just as iron sharpens iron, connecting with others in our network can help us learn and improve as we, in turn, help them.

How about you? What do you do to keep yourself ready for the changes in technology that come your way? If nothing immediately comes to mind, then give it some thought. It's always good to be prepared for the next bigger fish before we find it pulling on our line. And with that, I think it's time for me to prepare something for dinner: chicken, burgers, pizza—anything but fish! Keep on designing everyone, and I'll see you next time. **DESIGN007**

Tim Haag writes technical, thought-leadership content for First Page Sage about his long-time career as a PCB designer and EDA technologist. To read past columns or contact Haag, click here.

Feature Article by Kelly Dack
PCEA

For the past five years I have spent the first several hours of each working day communicating with a wide variety of offshore manufacturers about customer PCB design issues. I must say, it has been an eye-opening experience. Not only have I learned a lot about PCB manufacturing capabilities and challenges around the world but also about the design for manufacturability (DFM) attitude and aptitude of a wide cross-section of North American PCB designers and design engineers.

I have been working for a Pacific Northwest electronic manufacturing services (EMS) provider since 2015. A critical part of the business is helping companies that seek to move their electronics products from working prototypes to offshore volume production, all to meet cost-down goals.

I have felt up to the task, as I've been on my own journey toward the optimum DFM process for decades. Allow me to share some of the valuable lessons learned—along with the horror stories and successes—that have helped me hone my DFM skill set over the years.

Captive Designers: Gambling With Zero DFM Review

Years ago, I designed PCBs for a Nevada gaming company. Part of my job as a captive PCB designer was to evaluate incoming "engineering queries" (EQs) about our PCB designs as they transitioned from our internal, low-volume assembly line operation to high-volume PCB manufacturers in Asia and for assembly in Mexico. As the only PCB designer in our company who had completed the IPC CID and CID+ programs, I considered myself a staunch advocate for DFM. I had learned of the importance of considering the needs of the other PCBA project stakeholders, and I took every opportunity to learn about their jobs and capabilities.

But our designs were occasionally falling short of important DFM attributes required for a trouble-free assembly experience. In short, we had no peer review process. We were three unique PCB designers with three different

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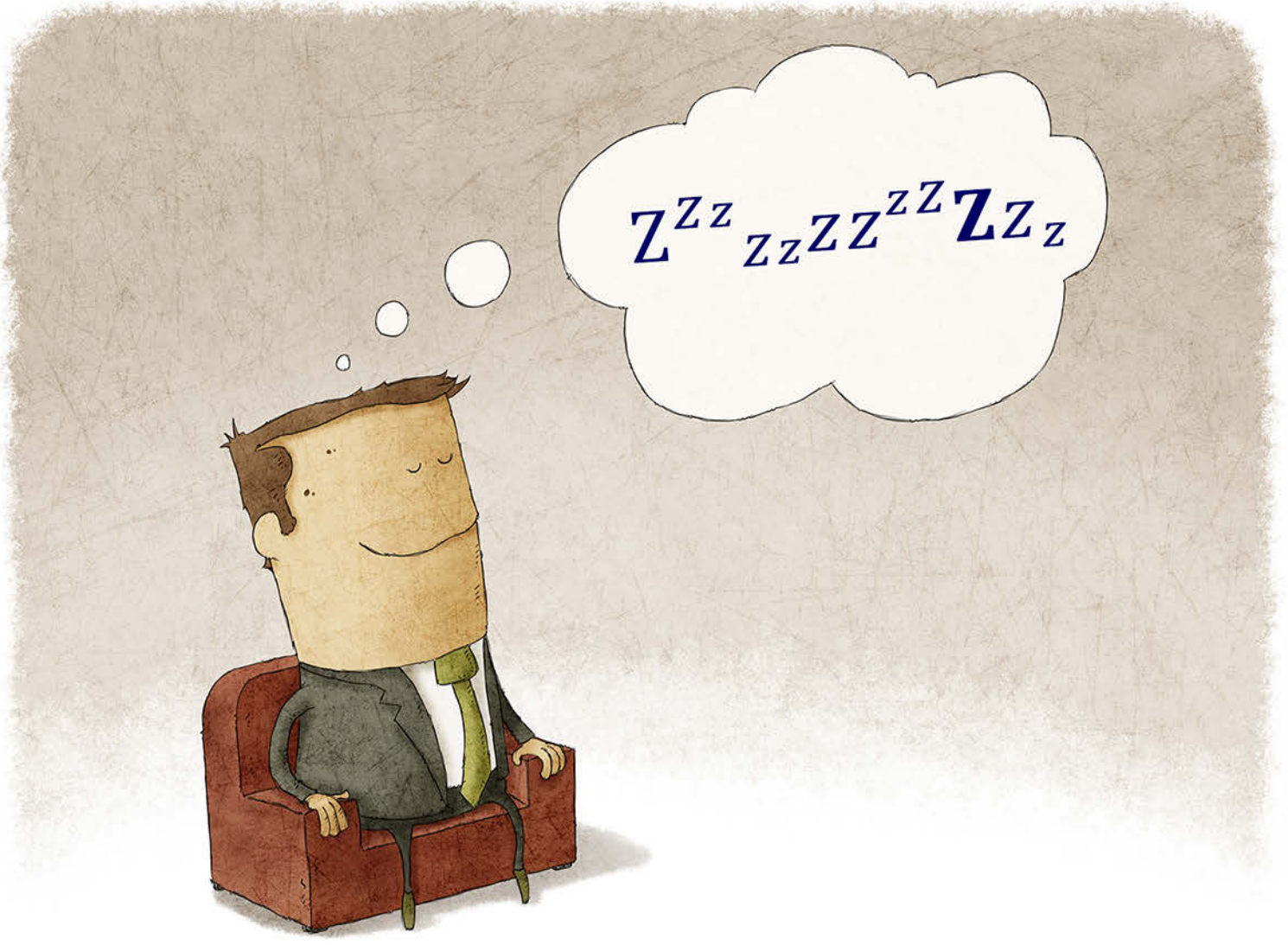

Did you know that two seemingly unrelated concepts are the foundation of a product's performance and reliability?

- Transmission line impedance and
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philosophies and our own individual processes for achieving design success. We were occasionally notified by email when our assembly counterparts had to stop the line and reset for another job due to a problem with one of our designs:

- "Missing fiducial marks on the bottom side"
- "The parts are placed too close together"
- "The panel is warping after first-pass reflow"
- "The stencil opening is too large"
- "The pizza cutter isn't working with this V-score"

Of course, upper management was copied on these internal cries for help. However, once the problems were worked through, the PCB assemblies usually performed well. The electronics engineering manager was happy and design engineering quickly forgot about the desperate cries from our assembly group.

One day, our disregard for DFM review came to an end. Our PCB layout group was suddenly placed under the leadership of the manager of engineering services, a gentleman named Mark who, not coincidentally, also managed the PCB assembly group. Suddenly, the exclamation point-laden frustration notifications from our assembly group stopped.

I'm ashamed to admit it now, but our PCB design group actually thought that our new engineering services manager had set the PCB assembly group straight on their role in the PCB development process. We believed that our philosophy was working.

Had Mark really retrained the PCB assembly group to adapt to a new manufacturing for design (MFD) philosophy? Au contraire! As it turned out, his wisdom was to have a profound effect on my design career.

During the time that the PCB assembly group had seemingly gone dark, our engineering services manager had been coaching them to collect data on our designs. When problems arose, a simple spreadsheet was used to record the date, the class of problem, and the amount of downtime it caused before it could be fixed.

After several months, Mark scheduled a meeting between the PCB design group and the PCB assembly group to discuss the data that the assembly team had collected. After hearing from the PCB assembly group, it soon was clear that reoccurring DFM issues were overly present on far too many of our designs. The minor DFM issues were stopping our assembly lines. DFM workarounds were adding up to hundreds of hours of lost time. No less than 23 separate issues were found over this measurement period.

It would have been easy for the assembly group to point fingers at us, but they did not. Mark had been coaching them with the book *The 4 Disciplines of Execution,* written by Chris McChesney and Sean Covey. During this time, the assembly team had adopted a "wildly important goal" of improving PCB assembly line performance by identifying and solving problems. They had gotten busy, using the book's four disciplines:

1. They focused on the wildly important.
2. They acted upon lead measures.
3. They kept a compelling scoreboard.
4. They kept a cadence of accountability.

In our meeting, the PCB assembly group gave a stunning presentation of how the program worked. They were able to gather and present compelling data which had an impact. Next, our savvy manager invited us to participate in the program. We all received copies of *The Four Disciplines of Execution.* We chose a wildly important goal of reducing DFM defects affecting our assembly stakeholders by 90% within six months.

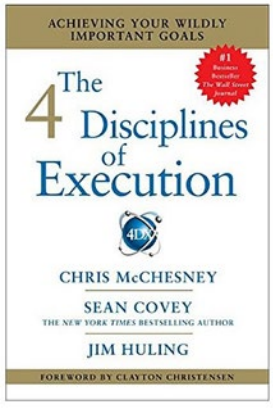

Figure 1: *The 4 Disciplines of Execution,* written by Chris McChesney and Sean Covey, provided us a framework to move forward with a solid DFM process.

Using the data our PCB assembly group had collected, we analyzed all the DFM issues that had been recorded. We noticed that many were obscure and happened infrequently or only once or twice.

We compared the DFM issues to each of our own design rule-checking routines and checklists. Amazingly, some of the DFM issues appeared on one or more of our personal checklists. What could this mean? It meant we were each doing a bad job of checking for DFM issues. Our manager asked why.

One of the most striking reasons was that one of the designers had compiled a checklist of 200 things before release, yet nobody was signing up for peer review and reporting on the 200 items on each other's PCB layouts. Our manager asked, "Why do you think you need to check 200 items?" That's the moment when my life changed.

Mark showed us how to leverage our PCB assembly stakeholders' data to solve our problems. We identified the top eight DFM problems identified on the spreadsheet. We referred to this list as the Great Eight and it became our new checklist. We instituted a new DFM process requiring our designs to be peer reviewed by another designer half an hour before release. Through communication, our overlooked DFM issues and "oopsies" were quickly identified and updated before release.

We kept a scoreboard. When a DFM issue was found during check, it was logged on our own spreadsheet. Each week we reviewed

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z	AA	AB	AC	AD	AE	AF	AG	AH
			MATERIALS									COPPER							HOLES / SLOTS									SOLDR MASK					
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Figure 2: An example of capability issues from offshore suppliers as recorded on an engineering query (EQ) tracker. Often, this requires customer approval.

our findings in a team meeting and discussed how we could improve further. Each week we received a copy of the DFM review data from our PCB assembly group. We compared these scorecards and could see that collecting data and tracking it had instituted a cadence of accountability within our two groups. Our two groups were compelled to work together to become one.

We were able to almost eliminate the DFM issues in just a short time, but it took data, communication, and buy-in from everyone involved. We worked for a captive shop, with every process (more or less) under our control. How would my enlightened DFM perspective serve me in a commercial manufacturing situation?

A DFM Complication: Offshore Suppliers

As I mentioned, I started working for an EMS company in 2015, and over the next five years my eyes were opened to new DFM challenges from PCB design customers. But this time the DFM challenges involved boards being built offshore in quantities of a million per year. I was awakened to the fact that offshore PCB suppliers have an entirely different set of DFM values, and their access to materials and processes is limited. Our offshore partners were experiencing daily frustration due to an alternate form of disregard for DFM.

If I could establish close contact with our offshore suppliers, as well as tour and audit their facilities, I knew I could implement my DFM plans. At these volumes, if I could convince one customer to make one DFM change to save a dollar on a PCB design, I could begin saving millions of dollars each year. All I needed was that positioning and some empowerment.

A large EMS company runs much differently than a captive OEM. There are many customers and various PCB designs. Designs are quoted and assigned to myriad PCB suppliers by a large quote team. Once a customer design is quoted and is assigned to a particular supplier, a steady list of requests to change the design or substitute materials begins to arrive from the supplier (EQs). Sometimes, to shave cost, the EQs request a simple change to an item, like changing solder mask material from matte finish to glossy. This can be an easy concession. But many times, even though quoted as such, the supplier will balk at providing a full amount of finished copper per the fabrication drawing spec. Sometimes it becomes apparent that the design would be un-manufacturable anywhere in the world using standard processing.

We occasionally receive a design composed of 3-mil lines and spacing on an outer layer with a specified base copper thickness of 1 ounce and plating requirement of a full 1 ounce. The current-carrying capacity of the outer layer power lines are calculated to carry a specified amount of current at 2 ounces with no room to modify the widths. There are some serious DFM issues going on here. The PCB was quoted three weeks before for a certain price, which then was passed on to the customer. Who is going to tell them that we lost three weeks, the board must be re-quoted, and the price will likely increase?

Sadly, at the scale and pace a large EMS company moves, putting a PCB designer in close

3	Circuit Design (Design Rules (Other))	See attached image, some circuit is the same net and the spacing between them is 5 mil. As the base copper thickness is 2OZ, the spacing is so small for us to build them.	☐ We suggest to fill the spacing which smaller than 8 mil.

Figure 3: Example of an engineering query from an offshore supplier.

touch with offshore bare board manufacturers and an outside PCB design customer for an idealistic "lunch 'n' learn" is almost impossible. In retrospect, it is easy to see that positive change can take place more easily in smaller groups. Think globally and act locally, as the saying goes.

DFM: Philosophy, Process, and More

Philosophy is defined as "love of wisdom" and those who design printed circuits with the manufacturer in mind must seek out wisdom through the philosophical methods of questioning, critical discussion, and rational argument. Systematic presentation of compelling data was employed to show our design team what was missing in the ability of our engineering department to perform at full potential.

How about you? Is your design philosophy based upon designing to the capabilities of the valuable manufacturing professionals who are going to be faced with fabrication or assembly of your layout? Will they be able to submit a competitive bid for volume production at incredibly low prices with staggeringly low margins for profit? If your layout encompasses all the guidelines and considerations for DFM, the transition should go well.

PCB design is also a process, a workflow. Using all the known information at the time of the start of a project, a designer will organize it into a database to begin the PCB layout. Incorporating effective DFM into a layout requires a sound process that must include a free and open communication link between the PCB designer and all manufacturers to collect manufacturing capability constraints.

Ideally, the process requires a PCB designer to tour the facilities that will be producing the PCB and PCB assembly. A tactile, hands-on relationship must be cultivated for design rules checking to be meaningfully set up in a design database. An understanding of all PCB manufacturing steps must be understood and acknowledged, including material availability, CAM, drilling, plating, etching, finishes and

Q5	如fig05附图所示，贵司的GERBER设计中的VIA孔孔径0.89mm，说明文件内要求塞孔，由于此类孔径太大，生产时容易孔内残留油墨 As shown in the attached figure of fig05, the VIA hole size in the GERBER file is 0.89mm, which are required to be solder mask plugging in the production document. As the hole size is too big, it may easy to cause solder mask inside holes.	1.按GERBER资料制作，接受孔内残留油墨。 2.按图2#的方式所有VIA孔加比孔整体大0.2mm的阻焊开窗 3.将0.89MM的过孔更改为0.4MM,过孔按塞孔制作 1. Make according to GERBER's data, and accept the residual solder mask ink in the hole. 3. Change the via hole size from 0.89mm to 0.4mm, and conduct solder mask plugging.	fig05附图五

Figure 4: Another example of an engineering query from an offshore manufacturer.

coatings, compensations, and all assembly conveyor processing steps. After a solid relationship is made between the PCB designer and the manufacturers of PCBAs, an appropriate design review process must be implemented.

Design rule checking setups within PCB CAD tools cannot remain set to their defaults. DRC values must be dynamically adjusted to match the manufacturing capabilities of the production manufacturer. Once a layout is complete it must be audited for conformance to these values along with the other important electrical performance values to certify the design for its transition to the manufacturer.

There is also an ongoing effort to standardize DFM. Within the past few years, DFM guidelines have been gathered into the IPC-2231A Guidelines for DFX standard by IPC. The document provides a DFX process framework to establish a discipline of design review necessary to perform a detailed analysis of manufacturability attributes commonly found in electronics hardware for fabrication and around which to model a printed board assembly.

The first goal of IPC-2231A is to use a multidiscipline engineering assessment tactic on elements influencing DFX. The second goal is to allow the user to establish standardized DFX checklists for major design elements such as bare printed board fabrication, printed board assembly manufacturing, electrical testability, and elements influencing product reliability, reuse, and impact on environment.

But until PCB designers can have instant, unbridled access to understanding the manufacturing capabilities of the service stakeholders who will be struggling to build their boards, DFM will continue to be a challenge. Educational outlets that focus on DFM will always summarize their overviews with a statement like, "Always check in with your PCB supplier prior to designing this or that on your PCB." This is not bad advice, but it may not be complete advice.

I am seeing two to five different PCB designs per day which are failing DFM as they move offshore for volume production. PCB designers must be given the visibility to see where their designs are headed. If the PCB or PCBA is destined for offshore manufacturing, a designer must be put in touch with the offshore supplier for a DFM (and DFC, design for cost) reality check so the design constraints can be set accordingly.

I look forward to the evolution of the IPC-2231 DFX Guidelines as a useful resource to aid visibility in PCB manufacturing capability and DFM expectations as we move forward. **DESIGN007**

Kelly Dack, CIT, CID+, serves as the communications officer for the PCEA and is a passionate PCB educator, writer, and owner of a family beef cattle ranch. By the time you read this, Kelly will have transitioned to a new position as a PCB designer at a Northern Idaho OEM specializing in products that support the Human Machine Experience (HMX).

PCB007 Highlights

Rooting Out an 'Us vs. Them' Mentality: An Interview with Laura Kriska ▸

Earlier this year, I-Connect007 columnist Dan Beaulieu submitted a book review on "The Business of WE: The Proven Three-Step Process for Closing the Gap Between Us and Them in Your Workplace." As a follow up to that review, Dan has interviewed the book's author, Laura Kriska.

I-Connect007 Releases Special Annual *Show & Tell Magazine* ▸

I-Connect007 is proud to announce the release of our special 2021 edition of *Real Time with... IPC APEX EXPO 2021 Show & Tell Magazine.* This unique publication provides you with in-depth coverage of this year's virtual IPC APEX EXPO 2021.

EPTE Newsletter: Ten Years After Fukushima ▸

Dominique Numakura remembers back to the devastating earthquake, tsunami, and nuclear disaster in Japan 10 years ago and what that has meant for him and his country. Scientists continue to ponder when it will happen again.

Punching Out: 'If I Were 20 Years Younger' ▸

We hear a lot of business owners say, "If I were 20 years younger, I would...," meaning they would make major investments or strategic changes if they had the time to realize the return on investment. Other reasons for not making investments are the lack of funds, lack of energy, etc. However, we feel that the return on investments does not always take as much time, money, and energy as owners think.

Technical Conference—Balancing Conventional and Disruptive Technologies ▸

I thought the three keynotes given by IPC President and CEO John Mitchell, Industry Week Editor-in-Chief Travis Hessman, and IPC Chief Economist Shawn DuBravac, were spot on. They all spoke to the fact that the way products are conceived, designed, manufactured, and used is changing rapidly. While the keynotes had different focus areas, I noted an important similarity—they all underscored the need for increased industry collaboration to help bring the factory and supply chain of the future to life.

Trouble in Your Tank: Process Defect Anomalies, Part 1—The Case of Etch Resist Attack ▸

Troubleshooting process related defects is not as simple an exercise as we would like to believe. The PWB fabrication process is a complex set of mechanical and chemical processes containing multiple steps. When even one of the process steps is not in control, end results can be disastrous. For now, the author presents a view of some defects that at first glance the origins are not obvious.

Testing Todd: Homing in on the Target ▸

Although electrical testing provides a beneficial safeguard against an electrically inferior product reaching a customer, it does require adherence to critical processes.

Analyzing Complex High-Density PCBs With Online DFM

By Pol Ghesquiere, SIEMENS TECHNOLOGY, **and Oren Manor,** SIEMENS SOFTWARE

The new software-as-a-service tool named PCBflow™ was created with the intent to reduce the number of iterations between the designer and the PCB fabricator, supporting the delivery of first-time-right designs. This cloud-based tool requires no installation and hardware. Designers can upload ODB++Design and IPC-2581 files into the secure cloud environment (additional formats are expected to be supported in the future) and select one or more manufacturers to apply process capabilities to the DFM analysis. Users are then guided through design violations, providing an interactive, web-based analysis and a downloadable PDF report for sharing.

Because specific knowledge about the manufacturers' processes is integrated into the software, designers can run DFM analysis on specific manufacturing constraints at any point during product development. The combination of being able to run DFM earlier in the process and easily working with a capable manufacturer allows the production of better new products more quickly. For the manufacturer, design-executed DFM based on specific manufacturing requirements translates into fewer callbacks and higher yields.

This software uses the Valor NPI DFM engine. Manufacturers can publish their DFM profile in a secured account and specify in a controlled way who can access and use their DFM profile. This allows designers to run a DFM analysis against a real manufacturer profile that fits their preferences. The manufacturer's constraint set is stored in their secured account. OEM layout designers upload their design to their secured account to run DFM analysis on a selected manufacturer's profile. Manufacturability violations are sorted and prioritized according to the level of severity to guide the designer through images and locations on the product for easy discovery and immediate correction. The result is fewer, if any, redesigns and the final design is much higher quality, maximizing yield.

The system quickly qualifies potential manufacturers based on their competencies

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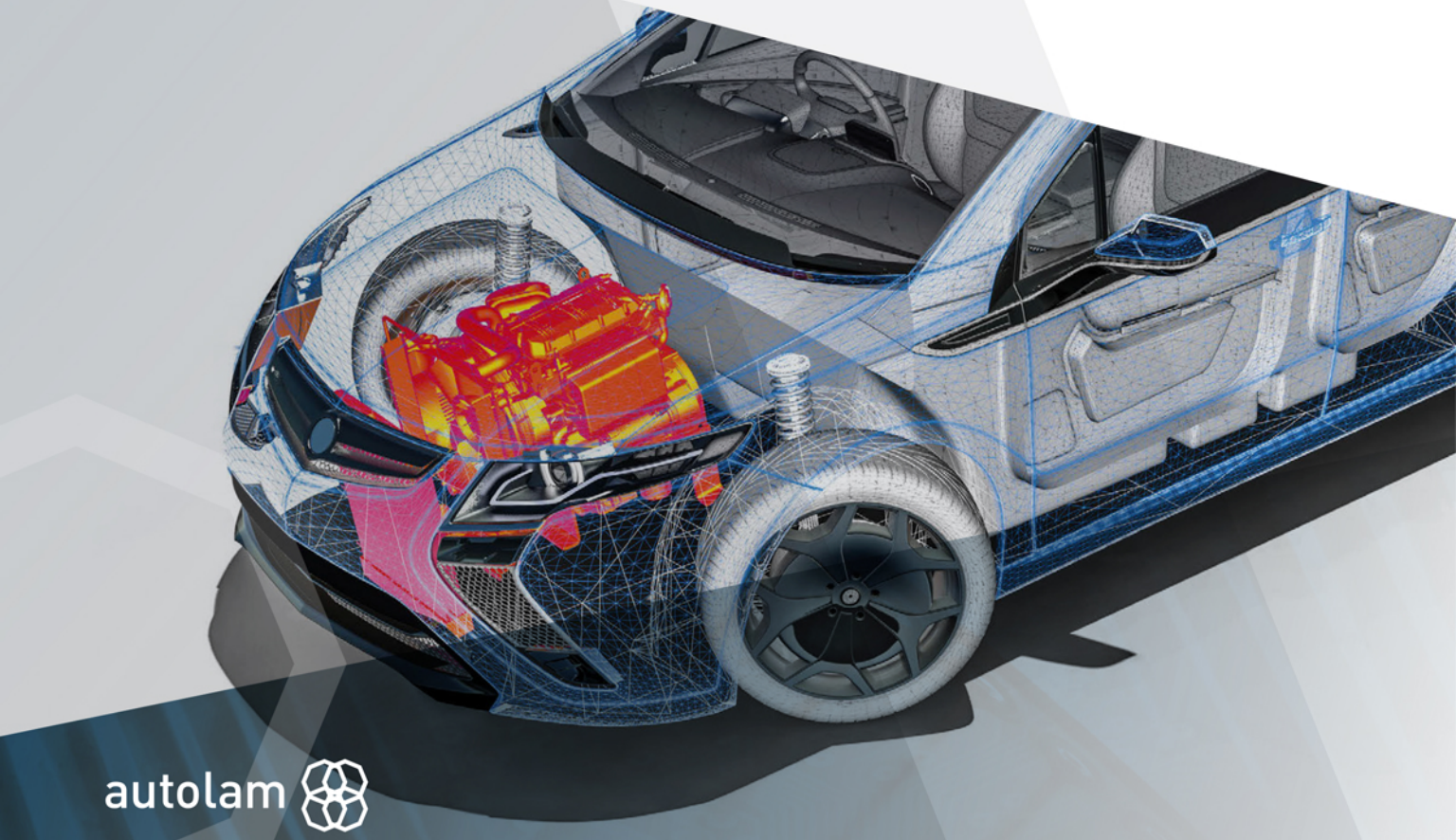

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Automotive electronics technologies are evolving at an increasing rate. Paying attention to the properties of materials at the substrate level is the first step towards achieving the most stringent performance targets of today's automotive manufacturers. autolam offers the solutions demanded by the diverse and unique requirements of automotive applications today and in the future.

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as matched to designers' requirements, so there is no need for lengthy research or email exchanges. This way, designers can know they are teaming up with a capable manufacturer and streamline their DFM flow. It is designed to easily guide layout designers to the manufacturability violation location in the design, along with images, tool tips, and measurements.

When logging in, each registered organization is assigned a unique ID, and all their data in the system is tagged with the organization's ID. This multi-tenant system isolates resources from access by other tenants. Each request is signed with an access token, which contains information on the tenant's identity, association, and authorized actions. Requests are forwarded to the PCBflow services.

When a file is uploaded via a web browser, an HTTPS connection is established, which secures the connection to the services for any type of communication, including uploaded data. This means that files remain encrypted until they have reached the service. Upon arrival to the cloud service, the data is decoded and forwarded to secured storage.

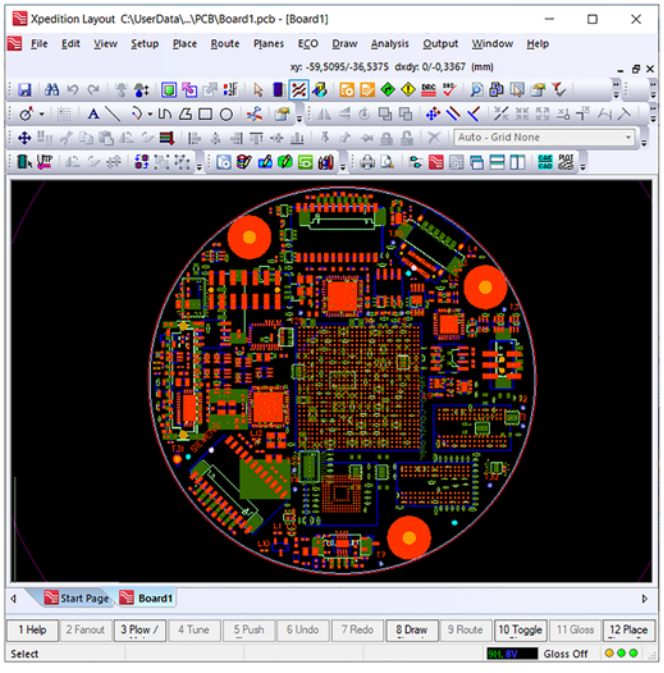
When it reaches secured storage, the file is again encrypted, using an encryption key that is generated specifically for the tenant ID. The key is managed by a separate service and can only be accessed by an authorized tenant. The file is then stored in a separate, dedicated folder that is associated with the key ID.

When you make an access request—for example, to download the file again—the system checks the request against the defined privileges, and if the action is permitted, a relevant request for the tenant key is created.

DFM Testing Time

At the Siemens R&D facility in Munich, we ran different PCB designs through PCBflow. We found that DFM testing time was very short, even with highly complex HDI designs. Based on the results, we were able to enhance the quality of the designs substantially regarding manufacturing at improved yield.

The following is an illustrative description of our first test using a control PCB, which is the central controlling unit in a system with many sensors and mechanical components. Because



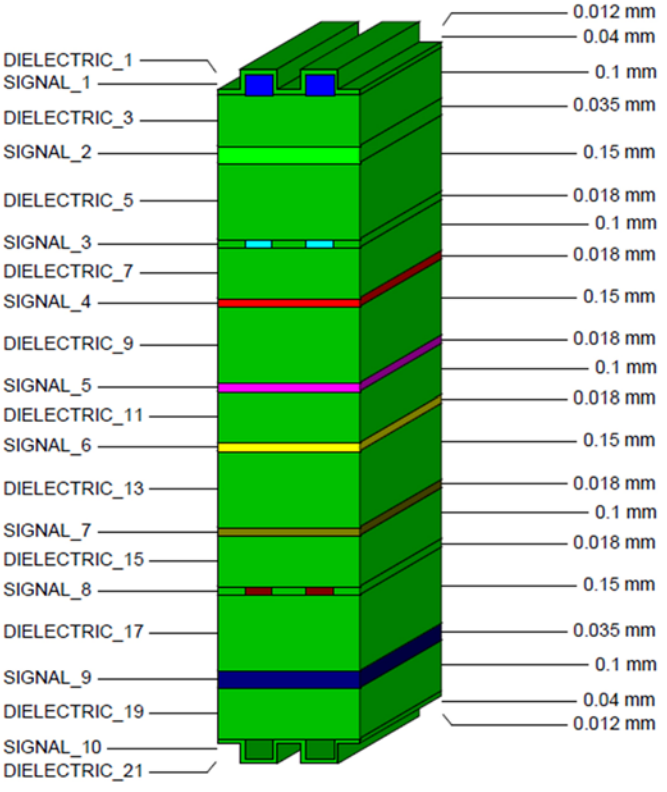


Figure 1: The control PCB featured 550 components on top and bottom side (above) and 10-layer board stackup (right).

of space limitations within the system, the circuit board contour is round with a 70.5-mm diameter. On this small disk, 550 components with 2,838 pins must be placed on both sides. To route this many components, which consists of a mixture of fine pitch active devices (ball grid array down to 0.5-mm pitch) and small passives (down to 0201 package size), a high-density board (HDI) construction was mandatory.

Figure 1 shows the placement of the components and the board construction, an eight-layer core with one sequential buildup layer on each side. Blind vias provide the connection from top and bottom layers to the core; buried vias connect the inner layers within the core.

We then validated the PCB design against a DFM profile before sending the data out to a PCB supplier. We uploaded the design, which was saved as an ODB++ compressed file, and then selected a DFM profile of a preferred PCB manufacturer. The manufacturer dashboard displays the company and location as well as the name and status of the DFM profile. Profiles with the status "public" are available to all users. Profiles with the status "limited" belong to companies that we are connected to within the network.

The next step was to click the RUN DFM button to start the analysis process. Once the DFM analysis progress bar reached 100%, the DFM report was presented automatically. The complete analysis for this complex HDI board took only 90 seconds. The DFM report shown in Figure 2 is interactive and allows filtering as well as scrolling options. The DFM report

Figure 2: DFM report with information pane (left) and analysis results per layer (right).

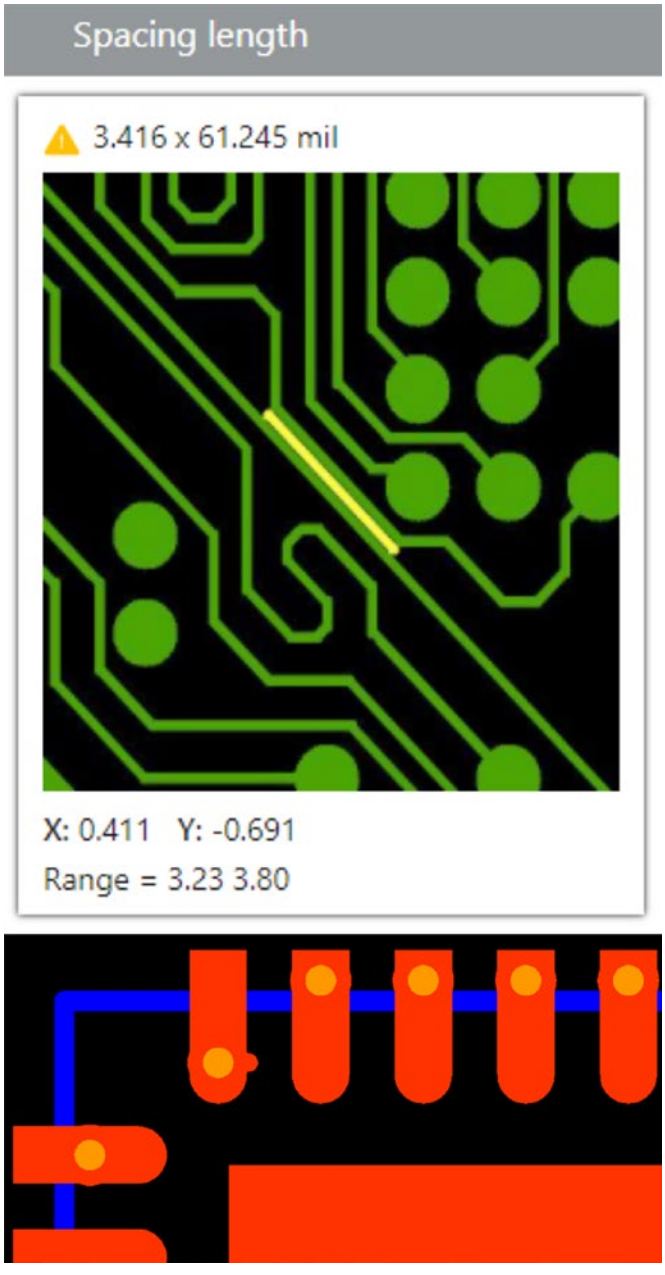


Figure 3: Top: Spacing length issue as reported in the DFM report. Bottom: Copper stubs on outer layers.

consists of two panes. The information pane contains general information about the board as well as error statistics derived from the ODB++ design data. The results pane displays the analysis results as a tree and provides controls for viewing and exporting the results.

Our DFM check of the control PCB identified a set of issues that could create problems during the production or assembly of the boards. Let us look at the selection of warnings and violations in more detail.

First, we can see a reduced copper spacing over a long distance between two tracks was reported on signal layer 3. Detailed information such as actual value (3.416 x 61.245 mil) and the X,Y location of the error is provided (Figure 3, top). A feature that we appreciated is that you can see a description of the constraint when pushing the information button. According to the constraint tolerance range, the severity is assessed "yellow = warning." This tells us the PCB manufacturer could have severe yield issues caused by electrical short circuits unless the distance between the tracks is enhanced. The DFM analysis detected several unwanted stubs on the outer layers (Figure 3, bottom).

Because the distance between the adjacent copper structures is larger than the value set in the design rule check (DRC), those routing artifacts were not recognized during the layout of the board. And, because the pitch

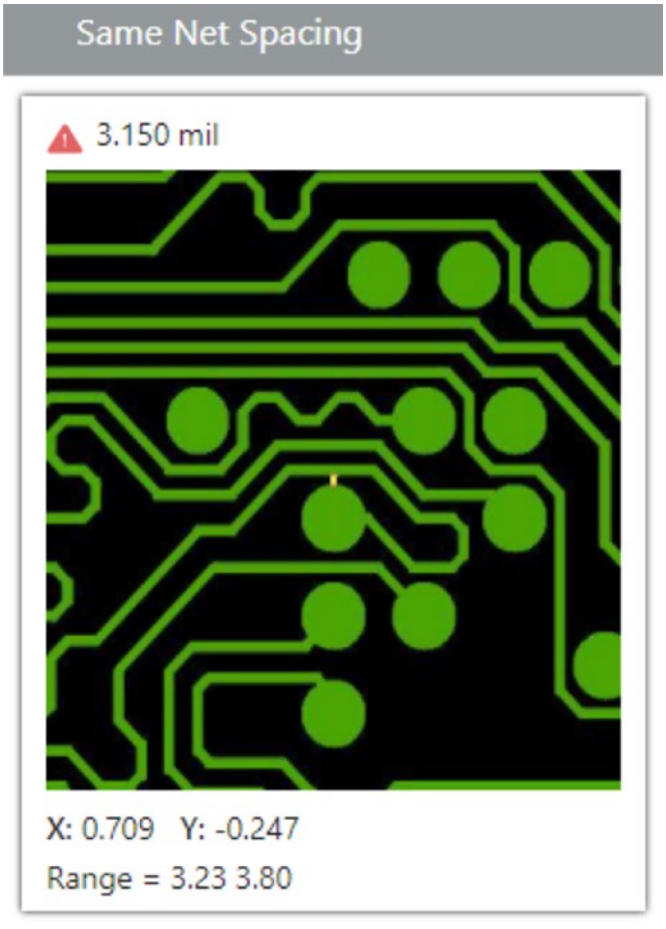


Figure 4: Constraint "same net spacing."

of the SMD pads is only 0.5 mm, those copper "noses" can result in solder bridges during assembly of the components. As a result, we removed all reported copper stubs.

Several warnings for stubbed vias were also reported. Buried vias between layer 2 and 9 of the core were only connected on one side. Those vias are useless, can cause a significant signal degradation, and lead to higher drilling cost. We could improve the quality of our design by removing those buried vias.

A violation against the constraint "same net spacing" was reported on layer 3 (Figure 4). The small space between copper structures of the same net creates an acid trap. An acid trap has the potential to trap chemical etchants used to strip excess copper from a board during the manufacturing process. When the etching solution pools in a certain area, there is a risk for corrosion of traces and creation of faulty connections or open circuits. So we changed the routing, keeping in mind the length-matching requirement.

Our experience with running DFM analysis with PCBflow on this board, and many other experiments, illustrated that we could improve the design in a very short time without any interaction with the PCB manufacturer during the layout phase. **DESIGN007**

Pol Ghesquiere is a project manager with the Technology Department of Siemens in Munich, Germany.

Oren Manor serves as the director of business development for Valor Division of Siemens Digital Industries Software.

Scientists Glimpse Signs of a Puzzling State of Matter in a Superconductor

Unconventional superconductors contain a number of exotic phases of matter that are thought to play a role, for better or worse, in their ability to conduct electricity with 100% efficiency at much higher temperatures than scientists had thought possible—although still far short of the temperatures that would allow their wide deployment in perfectly efficient power lines, maglev trains and so on.

Now scientists at the Department of Energy's SLAC National Accelerator Laboratory have glimpsed the signature of one of those phases, known as pair-density waves or PDW, and confirmed that it's intertwined with another phase known as charge density wave (CDW) stripes—wavelike patterns of higher and lower electron density in the material.

Observing and understanding PDW and its correlations with other phases may be essential for understanding how superconductivity emerges in these materials, allowing electrons to pair up and travel with no resistance, said Jun-Sik Lee, a SLAC staff scientist who led the research at the lab's Stanford Synchrotron Radiation Lightsource (SSRL).

The existence of the PDW phase in high-temperature superconductors was proposed more than a decade ago and it's become an exciting area of research, with theorists developing models to explain how it works and experimentalists searching for it in a variety of materials.

The researchers said these results not only demonstrate the value of the new RSXS approach, but also support the possibility that the PDW is present not just in this material, but in all of the superconducting cuprates.

(Source: SLAC National Accelerator Laboratory)

Test for Design—How Do You Measure Up?

The Digital Layout

by Kelly Dack, CIT, CID+, PCEA

Introduction

In this month's column, I convey the value of honing a skill set and the importance of being able to measure that skill set. Next, I hand it off to our PCEA Chairman Stephen Chavez, who offers a positive outlook on PCEA activities over the summer months. Again, I am happy to provide our readers with a growing list of events which are coming up in 2021.

PCEA Updates

How do you hone your printed circuit engineering skills? Are your skills measurable? We work in an industry which relies on analysis, checking, measurement, feedback, and adjustment to improve process and products.

When we think about PCB engineering, we tend to consider product success in terms of people setting up process steps—people defining analysis criteria and people working to make the product more useful, efficient, and more valuable.

But let's pause for a minute and ask the question: Who or what is making the people who pull the levers on all these attributes more useful, efficient, and valuable?

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Upcoming class:

8/30 to 10/6

Rigid-Flex Boards

Upcoming classes:

5/25 to 7/1

8/30 to 10/6

Extreme Environments

Upcoming class:

7/5 to 8/11

Look for these new courses soon!

- Introduction to PCB Design for Manufacturability
- PCB Design for Manufacturability
- PCB Design Embedded Components
- PCB Design RF Boards
- PCB Design for Printed & Wearable Devices

Learn more about our PCB Design Courses.

Anyone who has visited a PCB manufacturing facility should have been amazed not only by the speed of the operations, but by the accuracy of the equipment dedicated to forming physical parts out of raw materials using design data. A tour through a fabrication facility may begin in the raw materials department. From there you may take a stroll down the aisle of a high-speed PCB drilling department and then traverse the building over to the plating and etching operations. Perhaps you will move on to view the large-scale lamination press area where the operators "stack" the processed layers for insertion into a massive press which uses heat and pressure to laminate the separate layers of the PCB together into a single unified board.

You will be learning to use all your senses and therefore retain much more knowledge and understanding.

Throughout a tour such as this, your eyes will see, your hands will feel, and your nose will smell things that a large percentage of the PCB engineering community has never experienced. You will be learning to use all your senses and therefore retain much more knowledge and understanding. Your value as a PCB engineer will increase because you are reaching out to understand the jobs and processes of the important stakeholders of the PCB product. You will observe that the operators of the machinery do not specialize in every manufacturing process. You may notice that, about their jobs, our manufacturing counterparts are very attentive to meeting the design and manufacturing specifications for a particular task. They check their equipment. They measure and provide feedback to management and adjust their machinery as required. They are dialed in.

We in the PCEA salute our fellow PCB manufacturing stakeholders and consider the PCEA a place for us to join to collaborate, educate, and inspire each other.

A significant point always jumps out at me at the end of a manufacturing facility tour: Our manufacturing stakeholders take a great deal of time training and then executing their day-to-day processes and not a single process step moves forward without inspection, measurement, and adjustment.

Our manufacturing community stakeholders are measured, evaluated, trained, and re-trained on different incoming job requirements most every day.

I must ask of those who are involved in designing and engineering printed circuits: At what point are you required to adjust because your design will not move on to the next step of manufacturing? Who facilitates your training and re-training? Who is measuring and evaluating you?

As a PCB designer myself, I reflect deeply and sincerely on these questions often.

Aside from an automatic design rule of checking in our software which we have likely set up to suit our perception of what our other stakeholders need, it is very likely that a holistic measurement for success in our task of laying out a printed circuit assembly will not be available for weeks or months—not until the design is built and moves on to production. It is very likely that we will not receive all the important feedback because the PCB manufacturing industry takes no pleasure in complaining about our design deficiencies. Unfortunately, it is sometimes considered bad for business.

At PCEA, we seek to contribute to a design and manufacturing culture which considers that the burden for the measurement of our PCB engineering skill set is on each of us individually, and upon our organization. We feel that an important key to PCB engineering success is to support education of the PCB design commu-

nity and help to support definition of measurable skill sets to complement the PCB industry.

If you have caught yourself wondering what you can do to help your designs flow smoothly down the conveyors of both the bare board and assembly manufacturers; if you detect an empty void in your ability to discuss what is required to solve EMI challenges in your design layout before it becomes a significant problem; if you are tired of answering manufacturing queries regarding materials, processes, and documentation when they must get clarification; perhaps design training with a certification program for measurable success is right for you.

Many of us who began the PCEA are deeply involved in supporting and teaching the materials and certification programs offered through the IPC. The IPC Certified Interconnect Designer (CID) and advanced CID+ programs have been around for a long time and have served as the electronics industry go-to programs for measurable design and manufacturing knowledge. CID and CID+ certification is commonly cited as a requirement for a progressive company's PCB designer job postings. You can find out more about the IPC CID and CID+ designer certification training programs here.

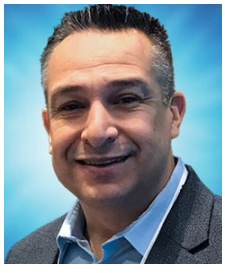
Additionally, the IPC has initiated new, in-depth, hands-on design training program modules covering introduction to PCB design, advanced packaging, design for rigid-flex boards, design for mil-aero applications, extreme environments, and another on design for micro modules. You can find out more about these training modules here.

Recently, some of our own PCEA founders have authored and launched a new Printed Circuit Engineering Designer professional development program as a comprehensive curriculum specifically for the layout of printed circuit boards. The five-day course is being offered online by EPTAC corporation, can be scheduled in the day or evening, and includes a comprehensive textbook. The program helps to prepare a student to become a candidate for optional certification as a Certified Printed Circuit Designer (CPCD.) The PCEA is happy to have been selected as the certifying body for this new Printed Circuit Engineering Designer program. You can find out more about this program here.

All these programs aim to help those of us in printed circuit engineering to see what is possible, what is missing, and how to adjust accordingly for continued PCB engineering success.

Message from the Chairman

by Stephen Chavez, MIT, CID+



This month, I'm excited about our positive membership growth along with new PCEA chapters being established both domestically and internationally. As our chapters gain momentum in 2021, educational materials continue to be the driving force bringing both existing and new members together, as well as creating excitement, positive energy, and member interactions. We continue to gain sponsorships and industry affiliations that add to the overall PCEA collective. These gains add to the strength of the PCEA collective and, more specifically, with our new educational content. Local PCEA chapters are collaborating with our industry sponsors to offer outstanding educational content to their respective local members and to those members who have chosen to be affiliated virtually with those respective chapters.

As we integrate and collaborate with our sponsors over these next few months, we will be rolling out more educational content. As per our mission statement of "Collaborate, Educate, and Inspire," this collaboration allows us to bring to the table even more outstanding educational content for anyone involved in printed circuit engineering; they can "feast" as they see fit.

We continue to remain in the virtual world as many industry events remain online. Unfortunately, some major industry events have simply cancelled and will not take place. PCB

East, another "hot" event, is currently set for an in-person event, but time will tell if it holds true, moves into the virtual world, or simply gets cancelled. PCEA will have some presence as several members will either attend or be active participants. Time will tell as these next few months unfold.

Even still, we are in full stride as we serve up awesome online virtual chapter events. Our education committee works to provide great industry content, so watch our website for new content and new activities for 2021.

If you have anything to do with printed circuit engineering, I highly recommend you get involved with and join the PCEA collective. This industry waits for no one and it evolves so quickly, so keeping your skill set and education up to date and relevant is key to your career success. It's important to stay on point and continue your professional development. By joining the PCEA collective, your percentage of long-term professional development increases significantly. We each control our own destiny and how our careers unfold. As one of my longtime mentors told me early in my career:

"You are your own best investment. You will only be as good as how much you invest in yourself. It is your responsibility alone, and no one else's, to continue to grow and develop as you strive to achieve success in your career."

So, with that said, I highly recommend you take advantage of the PCEA collective and all it has to offer; it can potentially set you up with a better opportunity for success.

Refer to our column and the PCEA website, pce-a.org, to stay current on up-and-coming industry events. There are many free webinars, so take advantage of these opportunities. If you have not yet joined the PCEA collective, I highly encourage you to do so.

I wish everyone and their families health and safety. Best of success to all as we head into the summer months.

Warmest Regards,
—Steph

Next Month

Spring has sprung and PCB engineers are on the move. It appears companies are hiring as they seek to fulfill the open positions left by those laid off earlier in the year or those who have relocated out of the busy cities. We will take a look at the hiring scene and see how some PCEA engineering folks are emerging from their cocoons and flying off to new opportunities.

Upcoming Events

Here is a growing list of upcoming events to look forward to. Do your best to follow CDC guidelines and take the precautionary measures—including hand washing, masking and vaccination—to squash the spread of COVID-19 and its variants. We're still in this together!

Del Mar Electronics and Manufacturing
June 2–3, 2021
Del Mar Faigrounds, Del Mar, California

Zuken Innovation World 2021
Europe: June 8–30 (Virtual)
North America: August 4-5 (Virtual)
Asia: Date TBD

PCB East
~~June 15–17, 2021~~ *CANCELED*
Marlborough, Massachusetts

DesignCon 2021
August 16–18, 2021
San Jose, California

SMTA International 2021
November 1–4, 2021
Minneapolis, Minnesota

productronica
November 16–19, 2021
Munich, Germany

PCB Carolina 2021
November 10, 2021
Raleigh, North Carolina

Spread the word. If you want to announce a significant electronics industry event, please send details to kelly.dack.pcea@gmail.com, and we will consider adding it to the list.

Conclusion

My seventh-grade woodshop teacher said, "Measure twice, cut once," and I've never forgotten it. Sometimes we get caught up on measuring the accuracy of others to our own standards when we should be adjusting and calibrating our standards to others. Collaboration requires action, communication, and a consistent set of standards. May we all seek to reach out and understand the challenges of others first, then measure our own outputs to compare whether we need to adjust and calibrate our knowledge, workflows, and processes to move ahead.

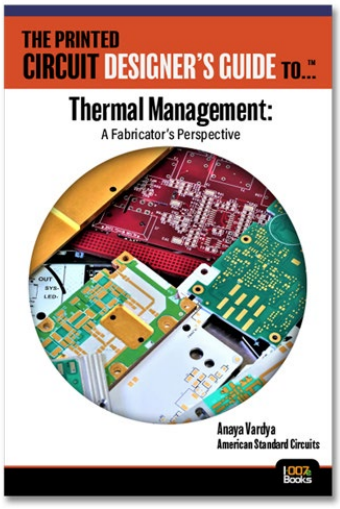
See you next month or sooner! DESIGN007

Kelly Dack, CIT, CID+, is the communication officer for the Printed Circuit Engineering Association (PCEA). To read past columns or contact Dack, click here.

Book Excerpt

'The Printed Circuit Designer's Guide to... Thermal Management: A Fabricator's Perspective,' Chapter 2: IMPCBs or MCPCBs

Insulated metal PCBs (IMPCB) or metal-clad PCBs (MCPCB) are a thermal management design that utilizes a layer of solid metal to dissipate the heat generated by the various components on the PCBs. When metal is attached to a PCB, the bonding material can either be thermally conductive but electrically isolative (IMPCBs or MCPCBs), or in the case of RF/microwave circuits, the bonding material may be both electrically and thermally conductive. The reason that RF designers usually have the bonding material thermally and electrically conductive is that they are using this not only as a heat sink but also as part of the ground layer. The design considerations are quite different for these different applications.



This chapter will focus on the IMPCB design considerations, and Chapter 4 will focus on RF thermal management. We will focus on things designers should be discussing with their PCB supplier to ensure manufacturability and a successful product launch. Since the choices, options, and decisions can be extremely complicated, it is critical to engage early and collaborate with the PCB fabricator about the specific design to ensure the most cost-effective solution.

Some of the more common applications of IMPCBs include:

- Power Conversion: Thermal-clad offers a variety of thermal performances, is compatible with mechanical fasteners, and is highly reliable
- LEDs: Using thermal-clad PCBs ensures the lowest possible operating temperatures and maximum brightness, color, and life
- Photovoltaic Energy: Renewable energy to power telecommunications, military camps, residential and commercial structures, and battery charging stations
- Motor Drives: Thermal-clad dielectric choices provide the electrical isolation needed to meet operating parameters and safety agency test requirements
- Solid-State Relays: Thermalclad offers a very thermally efficient and mechanically robust substrate
- Automotive: The automotive industry uses thermal-clad boards, as they need long term reliability under high operating temperatures coupled with their requirement of effective space utilization

Click here to download this free book.

Meeting the Challenge With Design Reuse

Feature Article by Stephen V. Chavez, CID+
PCEA

As project schedules get shorter and budgets get squeezed, project managers and small business owners must constantly look at ways to maximize limited funding and resources. But reusable PCB design IP allows us to investigate ways to potentially shorten design cycle time.

Typically, engineering teams are looking for ways to design PCBs faster, better, and cheaper, all with fewer resources. Within those engineering teams, today's circuit engineers must meet three competing perspectives for success (Figure 1): layout solvability (DFS), performance (DFP), and manufacturing (DFM) requirements with the targeted end-result of maximum placement and routing density, optimum performance, and efficient defect-free manufacturing. I refer to this as the Designer's Triangle.

A Variety of Challenges

Some of the biggest recurring problems in today's PCB designs are challenges regarding DFM, constraints, board layout planning, and routing; in general, schematics capture, and documentation for both fabrication and

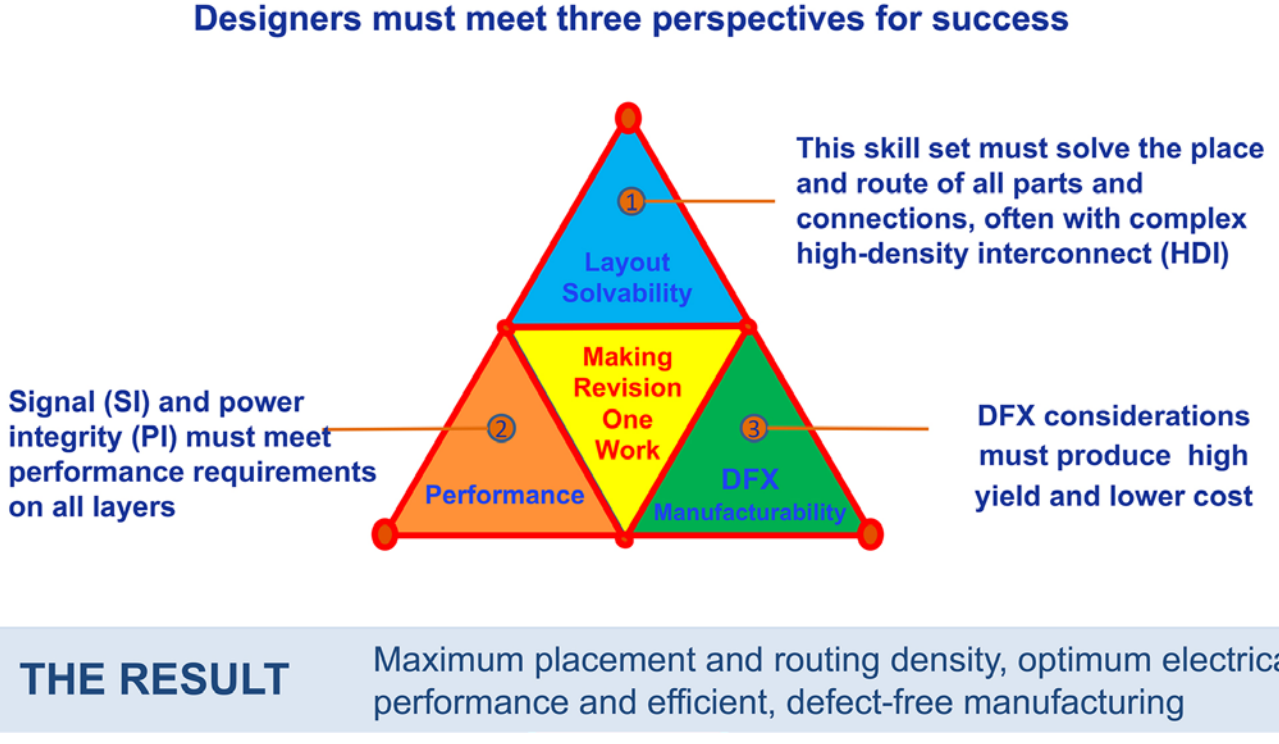


Figure 1: The three competing perspectives for success in printed circuit engineering.

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assembly. No matter what EDA tool you are using, the general process is the same:

- Define requirements
- Create libraries if they don't already exist
- Capture schematics to include constraints
- Integrate into PCB layout for parts placement and signal routing to include appropriate MCAD-ECAD handshakes
- Run SI/EMC/PI simulations (making layout adjustments as required)
- Generate final manufacturing outputs
- Release the final data into your respective product life management system

After this process is followed, send the released manufacturing data outputs to your suppliers to get the PCB fabricated and assembled. This is basically the same approach for design after design and has been for many years now.

However, we often step back and ask, "How can we design faster and better while cutting cost?" It's tempting to start with your EDA tool, but is greater tool automation enough to make a significant impact here? I believe it can be, to a certain extent.

But in PCB design, the moment of truth comes when you get that initial CCA into the lab and start testing its functionality, especially if it's an initial prototype. Will it work as designed and meet all the requirements? It potentially becomes Pandora's Box at that stage in the overall design process. No matter how well you design that PCB layout, if the actual electrical circuit simply doesn't work or it does not meet the end requirements, then it's back to the drawing board and another re-spin. This is a reoccurring issue.

Another common issue—especially in large companies—occurs when engineers are not aware that others have already been through the design phase of a particular circuit, so they repeat the design process over and over. For each redundant circuit created, a new verification cycle is required. Also, different choices for components are made in each redundant circuit, reducing volume purchasing leverage. Many printed circuit engineers keep reinventing the wheel, laying out and routing that same circuit many times from one PCB design to another. So, is there an alternate approach out there?

Precluding Problems With Design Reuse

Yes, there is. Take advantage of reusable PCB design IP by creating reuse blocks within your EDA library. In Figure 2, we see an example of a reuse block created from an existing vali-

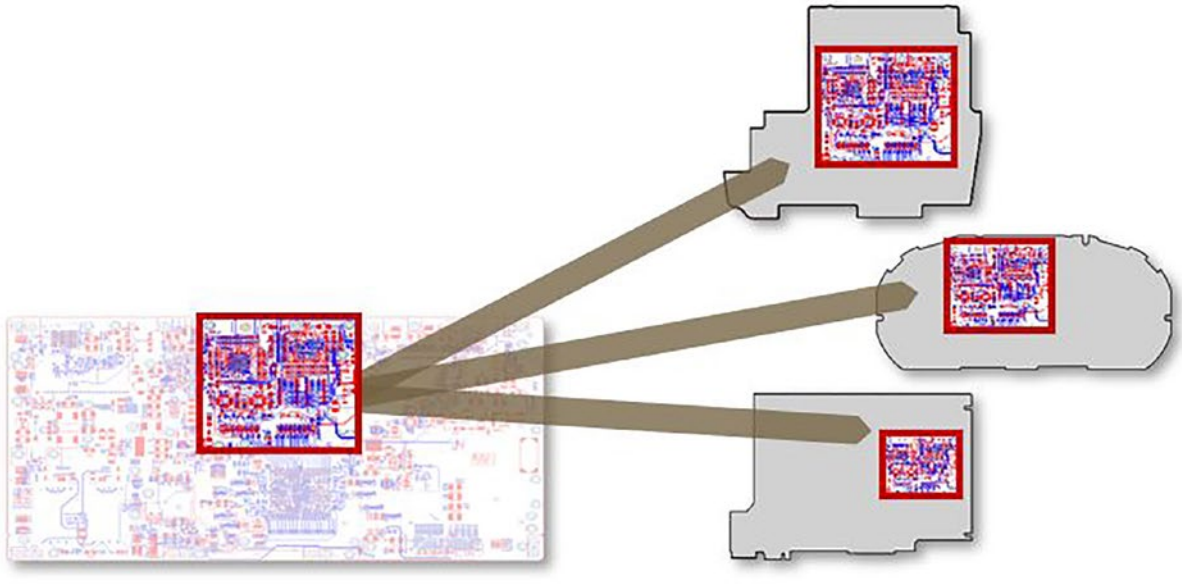

Figure 2: Example of a reuse block created from an existing known, validated, and certified CCA design.

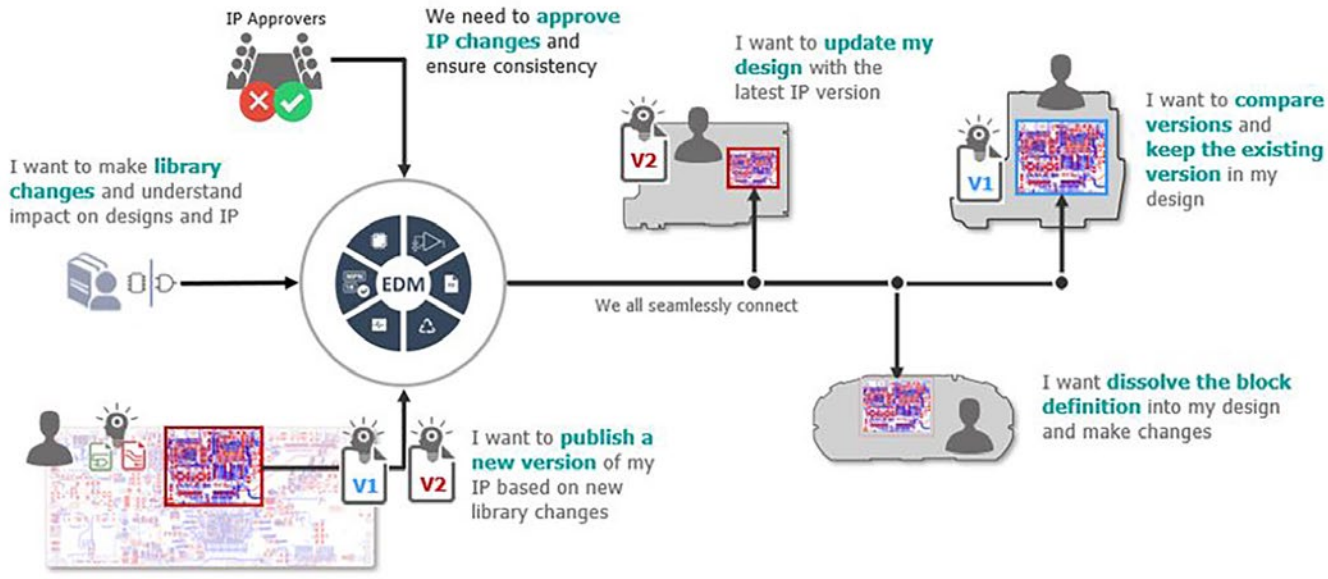

Figure 3: Example of managed block use cases using Xpedition and EDM.

dated, certified, and known CCA design. Its respective circuitry and layout have been captured and managed. This is not a "copy circuit" function; it's way more than that!

This known circuitry and layout is then reused in three separate PCB designs, saving the respective printed circuit engineer time from having to re-layout that same specific circuity. It also saves engineering time—both in the upfront engineering, which creates circuitry, and in the backend during the CCA bring-up testing phase. Your potential for success is much higher since the individual blocks are already known to work and are already validated. This is where you see the most significant cost savings, not to mention the potential of eliminating the need for a PCB re-spin.

Some of today's EDA tools can create and utilize reusable PCB design IP by using reuse blocks. These blocks can be managed within your library for total revision control and export content control as well. In Figure 3, we see an example of a managed block use case.

Here is an example, using this approach, of how I recently addressed my original question (How can we design faster and better while cutting cost?) on a recent hardware design reuse project.

I once created roughly 20 reuse blocks of known validated circuits to include their respective layouts. The reuse blocks consisted of a completed schematic and its associated completed design layout. The reuse blocks ranged from a simple circuit design of 10 to 50 components, to a complex multiple sheet schematic consisting of roughly 500 or more components. These blocks were managed efficiently and effectively within the EDM library.

In general, using a reuse block in a design is treated no differently than the way you would use a typical resistor symbol and its associated land pattern in the same design. The reuse blocks are connected from block to block and other circuitry by their respective ports, in the same manner as you would connect resistors, caps, and other ICs in your design.

From these initial 20 reuse blocks, the final design ended with about 120 reuse blocks by replicating respective reuse blocks within the main design as required to meet the final requirements of the CCA. By using this reuse approach, we cut about three to four weeks out of the upfront engineering and layout design cycle time as well eliminated about two weeks of backend lab testing time during the CCA bring-up and testing phase of the project. In

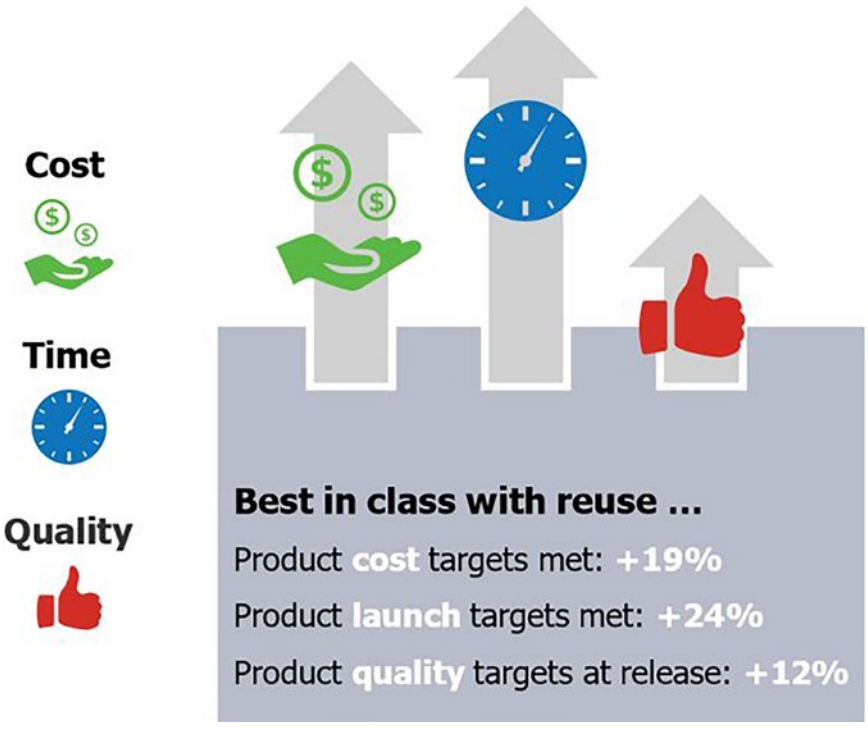

Figure 4: The Aberdeen study showing percentages of product launches meeting targets when design reuse is utilized. (Source: Aberdeen)

the end, the CCA worked the first time. There were no surprises or simple engineering mistakes, as the CCA worked as anticipated since all the blocks consisted of already known and validated circuitry. The icing on the cake was that these re-use blocks are now available not just for this project, but all engineering teams within the company could take advantage of it in their respective designs. So, the potential savings to the company had even more of a long-term effect.

Studies have shown that design reuse is an effective way to solve these classic problems. The Aberdeen study cited in Figure 4 showed increases in the percentage of product launches meeting their cost, schedule, and quality targets when reuse was applied.

IP reuse has been standard procedure in IC development for decades because complexity and engineering costs demanded it. So, it's not as if this is a new concept to the industry. With circuit board complexity and speeds rapidly rising, the time has come to adopt similar practices in the PCB design realm. Most new products are variations of existing products, so it only makes sense to reuse proven circuitry from those products whenever possible. Leveraging known good circuits in new PCB designs accelerates new product development and eliminates redundant effort. For example, once a power supply circuit is built and verified, why recreate it for every design that has the same power supply requirement? Leveraging certified circuits ensures they are high-quality, comply with company standards, and use preferred components. In turn, this reduces verification time and avoids potential supply chain issues.

For designs containing sensitive or restricted circuitry, formal management of reusable IP allows for proper tracking of critical information such as the owner, operating characteristics, and any export control requirements. All these benefits combine to reduce design time and product cost while improving quality. With up to 50% reduced design cycle time, the potential for reduced respins, and an increase in reliability and quality of designs, I highly recommend looking into design reuse as an option to design faster, better, and cutting cost in your company—provided that your respective EDA tool can handle true design reuse and data management of reuse blocks, as well as a potential shift in your internal engineering culture toward the use of reuse blocks. **DESIGN007**

Stephen V. Chavez is chairman of PCEA, the Printed Circuit Engineering Association.

MilAero007 Highlights

NASA Begins Final Assembly of Spacecraft Destined for Asteroid Psyche ▸

Set to launch next year, the agency's Psyche spacecraft will explore a metal-rich asteroid in the main asteroid belt between Mars and Jupiter.

IPC Study: Europe's Economic Recovery, Long-Term Future Depend on Attention to Electronics Manufacturing Industry ▸

A new IPC study, "Digital Directions, Greener Connections," finds the electronics manufacturing industry has largely withstood the negative effects of the COVID pandemic and is poised to help drive Europe's economic recovery and resilience, especially if anticipated government decisions take a supportive approach.

Defense Speak Interpreted: Industrial Base Evaluation ▸

So, what is an "industrial base" to the Defense Department? And wouldn't we expect a "battle plan" from Defense, not an "industrial strategy"? We want to review the Defense Industrial Strategy in the January 2021 Report to Congress from the Acquisition and Sustainment section of the Department of Defense.

Arlon EMD Introduces 84HP Prepreg to Compliment the 85HP Laminate System ▸

Arlon Electronic Materials introduces 84HP high-performance 250^{0}C Tg temperature polyimide resin prepreg. Arlon developed 84HP as a prepreg bonding companion to Arlon's 85HP filled pure polyimide resin laminate system. 84HP is designed for use in filling etched areas in polyimide multilayers that contain thick copper metal cores.

Her Voice: I'm Not Betty Crocker ▸

It takes both reason and intuition to outfit a manufacturing facility, a point I was able to demonstrate as we prepared and moved into our new building several years ago.

IPC Issues Call for Participation for IPC APEX EXPO 2022 ▸

IPC invites engineers, researchers, academics, technical experts and industry leaders to submit abstracts for IPC APEX EXPO 2022 to be held at the San Diego Convention Center.

Elbit Systems of America Completes Acquisition of Sparton Corporation ▸

Elbit Systems of America, LLC has completed the acquisition of Sparton Corporation from an affiliate of Cerberus Capital Management, L.P. for $380 million, subject to customary price adjustments, resulting in a significant expansion of Elbit Systems of America in the United States.

BAE Systems Australia Invests in Hypersonic Weapons Capabilities ▸

BAE Systems Australia announced that it will increase its investment in Australia to support the rapid development of a sovereign high-speed weapons capability.

Lockheed Martin Awarded $1 Billion Contract for Precision Fires All-Weather Rocket ▸

Lockheed Martin received a $1.12 billion contract from the U.S. Army for Lot 16 production of Guided Multiple Launch Rocket System (GMLRS) rockets and associated equipment.

Pin-Out Challenge: Rethink the Solution

PCB Talk

by Tara Dunn, AVERATEK

Semi-additive PCB fabrication is getting a lot of attention as fabricators install new processes that enable them to provide much finer features than traditional subtractive etch processes. This is opening new opportunities and tools for PCB designers to solve today's complex electronics challenges. These packaging and interconnect solutions can reduce size and weight by 90% over traditional processing techniques in the U.S. and bring significant signal integrity benefits. As with any new technology, there are many questions: How to apply this new capability to the design, what are the signal integrity considerations, and who has the capability to supply these fine features?

This column kicks off a series of interviews with veteran PCB designer who share their thoughts, opinions, and questions as they navigate this new frontier. I recently sat down with Cherie Litson, MIT CID/CID+, president of Litson1 Consulting and an instructor at Everett Community College, to understand her perspective on this new fabrication capability.

Tara Dunn: Cherie, you are a well-known designer and instructor in the industry, but for those who have not had the opportunity to meet you, could you please start with a quick introduction?

Cherie Litson: My background is broad and deep: it has been an amazing opportunity to work with so many companies, notably Microsoft—where I helped create their design database for the Surface and, earlier, the first wireless mouse. The first hand-held ultrasound from SonoSite was another passion project. Passing on what I have learned from others led me to become a Master Instructor for the IPC Designer Certification program. I learn more every time I teach. As a member of the Averatek Community of Interest, I encourage everyone in the industry to share their experiences with this new technology so we can all learn and optimize the benefits of new developments.

Figure 1: Cherie Litson is an instructor at Everett Community College.

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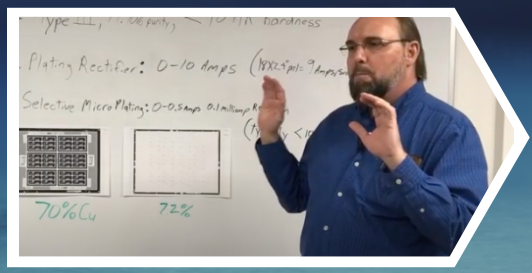

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Figure 2: Cherie is an avid golfer whose teams have gone to national competitions in the past five years.

Golf is my other passion: I have been involved in the LPGA Amateur Association (previously EWGA) since 2001. While learning how golf and the professional world mix, I have been able to take my golfing teams from local to national competitions for the past five years. I could go on about golf, but let's tee up this discussion!

Dunn: Impressive! My golf skills stop with my highly developed golf cart driving expertise; actually hitting that ball in a straight line is something I am still working on. You mention Averatek's Community of Interest; this is new. Can you tell me about that?

Litson: Averatek, a Silicon Valley innovation company, manufactures key chemistries and licenses the processes for their use. Two processes, in particular, are having an effect on the PCB design industry: LMI™, the catalytic ink used in the A-SAP™ process, and Mina™, a surface treatment that enables soldering to aluminum. These products are now commercially available through licensed fabricators, so it is important for designers to learn about them. The Community of Interest is starting to bring together a wide range of people from all sectors of the industry who are interested in learning more about semi-additive PCB processes. Nothing formal yet, but we're hoping to set up a website or blog to pool our knowledge on these types of products.

Dunn: What aspect of these new PCB fabrication capabilities is most valuable to you?

Litson: I am excited by the ability to route traces at 1 mil or even below, as that opens possibilities for designers to produce increased density at lower cost. The A-SAP process provides the designer an opportunity to significantly reduce layer count, simplifying complex designs.

These geometries can potentially eliminate pin-out challenges while maintaining reliable signal integrity. I can see the advantages of using a taller yet narrower trace for signal integrity; this is the winning factor for me. This process results in traces with vertical rather than trapezoidal sidewalls, realizing benefits in both size and RF advantages, eliminating the etch compensation requirements.

Designers working on next-generation products will be excited about the ability to form a 15-µm trace and space with the semi-additive processes. Many designs are being driven to require line and spaces at 50 µm due to smaller pin spacing on components and smaller package products. The fabrication of these traces is something that has not been available in the U.S. until now.

Dunn: Cherie, I know you are an avid learner; when you are researching new technology, which reliability tests mean the most to you?

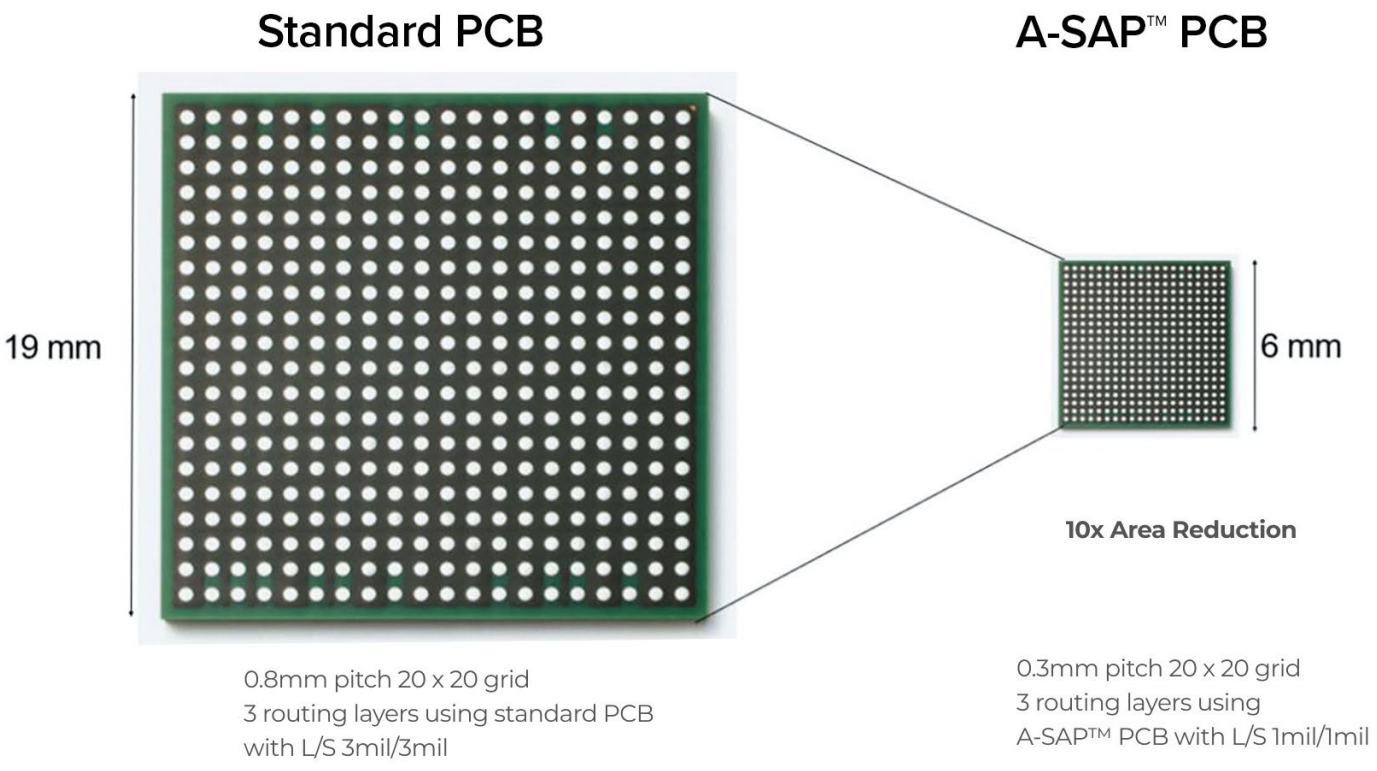


Figure 3: Many designs are being driven to require line and spaces at 50 µm due to smaller pin spacing on components and smaller package products.

Litson: As I consider how to best apply this technology, material compatibility is an important aspect. It is important to know that a new process is going to be compatible with nearly all materials. Next, I'm looking into the electrical aspects of these new geometries.
I also look at proven reliability parameters: the A-SAP process passed peel strength, IST coupon testing, and signal integrity analysis across a variety of materials.

Dunn: Working with something new can be exciting and just a little intimidating. Navigating the learning curve, do you see any challenges for designing with this new technology in mind?

Litson: In my opinion, designers should remember their basic electronics—it influences everything we do. We must understand the physics to make certain we know what will be affected. With these new parameters, we will need to go back and take another look at our calculations, which are based on the resistance of copper which is based on the area. Then bring into the equations the resistance of the dielectric materials, layer structures, etc. I am curious to see how the geometry of the conductors shifts the electrical results.

Because each product is different, there are few set-in-stone design rules for semi-additive processed layer-only guidelines. The most important guideline: this process requires close collaboration between design and fabrication. For additional guidance, a collection of case studies would be great, maybe online as a dynamic design guide. Just brainstorming!

Dunn: An online dynamic design guide is a great idea. Taking a step back from design, why do you feel that this new technology is important to the industry?

Litson: I think this is important to the industry for several reasons. One is implementation of this process—it is designed to integrate

Cherie teaching a class during the pandemic.

with existing PCB fabrication equipment, so it does not require the costly capital investment usually associated with new technologies, allowing even the smaller and mid-size shops to offer this advanced technology to their customers.

While this process certainly gives us the benefit of 25 µm line/space and below, the additive process also has RF benefits at larger feature sizes, such as improving impedance control. I think we are just scratching the surface of how to get the most benefit from this capability. I am already seeing the simplification of complex designs, improving yields, and reducing costs. I am excited to see where this technology takes us.

Dunn: Cherie, as we wrap up, what advice would you give to PCB designers who are just hearing about the opportunity to work with fabricators that can now offer these fine feature sizes?

Litson: Start today! Do some research, share your concerns, share your experiences, try it out. I can see many benefits to utilizing this process at the 75 µm, 50 µm, and 25 µm trace sizes and smaller.

Dunn: Thank you so much for talking with me today. To learn more, what is the best way to reach you?

Litson: The best way to reach me is at Litson1@aol.com. Thank you. **DESIGN007**

Tara Dunn is the vice president of marketing and business development for Averatek. To read past columns or contact Dunn, click here.

A Roundup of Stackup Coverage

In almost every conversation with PCB designers and design engineers about challenges they face—not to mention our reader surveys—stackup design is a recurring theme. The stackup, sometimes described as the "backbone of the PCB," continues to perplex even veteran designers, often due to a lack of communication between OEMs and fabricators.

So, this month, we're including links to some of our recent coverage of PCB design stackups. If you missed these pieces before, here's another bite of the apple!

TTM's Approach to Stackup Design: Train the Customer


In this interview with the I-Connect007 Editorial Team, TTM's Julie Ellis and Richard Dang drill down into stackup design. They detail some of the common stackup challenges that their customers face when designing for both prototype and volume levels and offer advice to designers or engineers who are struggling with stackup issues.

Stackup Planning: Three Decades of Innovation

This column by iCD's Barry Olney is a gift that keeps on giving: He includes a dozen links to his past Design007 columns that focus on stackup design, with an emphasis on signal integrity. Barry also discusses the current best practice for high-speed stackup design, as well as tips on utilizing field solvers and incorporating multiple technologies in a stackup. It's all here.

The Magnitude of Stackup Considerations

When Michael Creeden of Insulectro was asked to write this feature on stackup creation, he paused at the magnitude of the subject. He noted that stackups are similar to the framework used to pour concrete—you need to get the framework right because the framework has such a big impact on the final outcome.

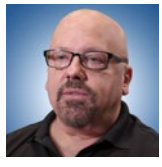
Seven Tips for Your Next Stackup Design

University of Colorado-Boulder instructor Eric Bogatin's feature on stackup design was written from his viewpoint as the Signal Integrity Evangelist, and he shines a light on factors that may not always be apparent to the typical PCB designer. We know that our readers love lists, and this seven-step primer for designing stackups with SI in mind will not disappoint.

Layer Stackup, Short and Sweet

As Cherie Litson of Litson1 Consulting notes in her article, there are so many ways to do a layer stackup for your PCB, but there are almost too many options available today. Cherie helps clear away some of the confusion about stackup options, drilling down to what works, what doesn't work, and why. Bonus: Cherie even includes a formula for calculating the number of signal layers for a design.

OEMs Must Own the Stackup

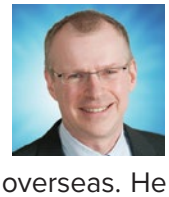


Who owns the stackup design process? Is it the OEM's design team, which is familiar with all the electrical requirements of the PCB, or the fabricator, who knows far more about the manufacturing process? In this interview, Bill Hargin of Z-zero, a stackup optimization software tool company, explains why he believes many of today's stackup miscues stem from OEMs who refuse to take ownership of the stackup. Don't miss this article.

Stackups: Properly Conveying Your Info to the Fabricator

Most designers would agree that communication with the fabricator can preclude many of the problems they face. In this column, Mark Thompson of Monsoon Solutions discusses how to create the perfect board stackup, specify what you truly want to convey to the fabricator, and eliminate conflicting information about stackups.

Martyn Gaudion on Stackup Design Considerations



The I-Connect007 team met with Martyn Gaudion of Polar Instruments to discuss the ins and outs of stackup design, and why designers seem to be getting stackups wrong, especially if a board is going into volume production overseas. He also focuses on the many trade-offs involved in even the simplest stackup design today.

Conformal Coating vs. Encapsulation Resin

Sensible Design

by Phil Kinner, ELECTROLUBE

Without a doubt, the biggest question we get asked regularly at Electrolube is, "When is it suitable to use a conformal coating or an encapsulated resin?" There are several considerations that will determine the answer; however, it depends largely on how the circuit will be housed within the assembly as well as the type of environment in which it will operate. For instance, if the PCB housing design is intended to deliver the primary environmental protection, we would recommend using a conformal coating as it will act as the second line of defence in the event of any housing seal failure.

Alternatively, where there is no separate housing or capacity to provide primary environmental protection, then an encapsulation resin is likely to be the better choice. Clearly, there will be applications where the choice of technology is obvious, for example, where duty in a harsh environment demands the highest level of protection. In this case, a potting and encapsulation resin will provide the necessary long-term protection—so long as the correct resin has been selected, tested, and approved for the prevailing environmental conditions.

Where ease and speed of processing are important, conformal coatings will always be the preferred choice, particularly as the thin cured film of a modern, well-formulated coating can provide a high level of protection in any

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case. Most of these coatings are single-part systems that are easy to apply and quick to cure with little temperature rise. On the downside, single-part coatings are solvent based to modify their viscosity for application purposes, which can have environmental repercussions.

Conformal coatings can be applied manually using a paint brush, a spray gun, or simply by dipping the circuit board into a bath containing the coating material. Where large numbers of circuits must be treated in a fast-moving production line, coatings are more likely to be applied by closely controlled robotic selective-coating systems for maximum consistency. Conformal coatings are applied in their liquid state as thin films which cure to provide a dry film thickness of between 25 and 100 microns, adding minimal weight increase to the assembly. These coatings are usually clear and allow rework, so coated components are visible and easy to replace. The level of chemical resistance and thermal protection that conformal coatings provide is generally good for short exposures.

The level of chemical resistance and thermal protection that conformal coatings provide is generally good for short exposures.

Encapsulation resins and potting compounds can be applied in thicknesses from 0.5 mm, but are generally applied much thicker than this, which can lead to a significant weight gain for the assembly. Weight gain aside, this increased thickness does mean that the PCB is far better protected against chemical attack, particularly in cases of prolonged immersion. Depending upon the formulation, a resin can also provide superior protection against physical shock since its bulk will help to dissipate the forces across the PCB, rather than allowing them to be concentrated. A bonus for protecting your intellectual property and design advantages, a layer of dark-coloured resin can obscure the circuit layout and components from prying eyes. One thing to remember, though, is that attempting to remove the resin will damage the PCB, severely limiting opportunities for component replacements.

Compounds and resins are generally two-part systems, in which a resin is mixed with a hardener in a precise ratio to form a cross-linked polymer when cured. It's also possible to add mineral substances (fillers) to resins to improve their performance under certain operating conditions. Like conformal coatings, most resins will cure at room temperature, and while this can be a relatively slow process in the case of potting resins, cure time can be reduced by applying heat.

It might interest you to learn that, in certain applications, where a two-part resin formulation may have been the first choice for circuit protection, a two-part conformal coating may turn out to be the better approach, thanks to its superior mechanical properties, as compared with one-part coatings. For example, Electrolube developed the 2K range of solvent-free coating materials, based on similar two-part chemistry to resins, but designed to be applied by selective coating equipment in the 200–400-micron range, combining many of the advantages of both technologies and minimising many of the drawbacks of each. Moreover, switching from a resin to a conformal coating will eliminate the weight penalties of the former, which may be critical to some applications. Two-part conformal coatings can be applied relatively thickly without risk of cracking, giving a sharp edge coverage that performs somewhere between where a conventional conformal coating fails, and potting is required. A two-part conformal coating's environmental protection capability is also rather impressive.

For example, in environmental chamber trials simulating highly condensing conditions, while a urethane resin potted assembly gave the highest overall values in terms of circuit protection—and showed the least change during condensing events—the very large difference in thickness between it and a two-part conformal coating didn't show a large increase in performance. Indeed, the two-part coating achieved much the same results as the potting compound at one-tenth the thickness.

Despite these advances in conformal coating chemistries, potting and encapsulation resins will always offer the highest level of protection for PCBs, whether used to protect against mechanical shock and vibration, thermal cycling, chemical attack, or the presence of high voltages where maximum dielectric strength is needed to avoid damaging discharges and leakage currents. The trade-offs are added weight, loss of rework capability, longer processing times, and high cure temperatures.

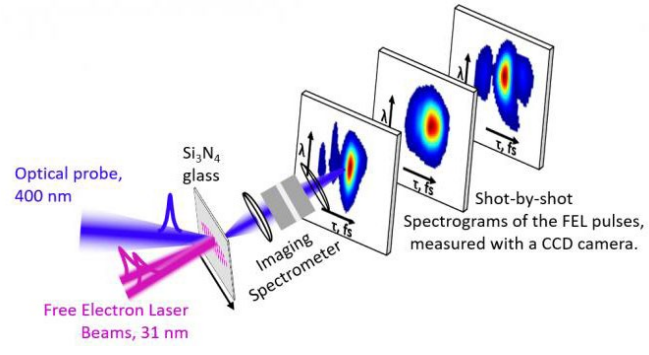
If you do experience problems choosing between these methods of circuit protection, remember, there are experts out there to help. And it is always worthwhile taking the trouble to test alternative methods of protection, preferably at the prototype stage, before you make your final choice; the experts are ready to help you with this task as well. **DESIGN007**

Phil Kinner is the global business and technical director of conformal coatings at Electrolube. To read past columns or contact Kinner, click here. Download your free copy of Electrolube's book, *The Printed Circuit Assembler's Guide to... Conformal Coatings for Harsh Environments,* and watch the micro webinar series "Coatings Uncoated!"

New Method Measures Super-Fast, Free Electron Laser Pulses

New research shows how to measure the super-short bursts of high-frequency light emitted from free electron lasers (FELs). By using the light-induced ionization itself to create a femtosecond optical shutter, the technique encodes the electric field of the FEL pulse in a visible light pulse so that it can be measured with a standard, slow, visible-light camera.

"This work has the potential to lead to a new online diagnostic for FELs, where the exact pulse shape of each light pulse can be determined. That information can help both the end-user and the accelerator scientists," said Pamela Bowlan, Los Alamos National Laboratory's lead researcher on the project. The paper was published April 12, 2021 in Optica. "This work also paves the way for measuring x-ray pulses or femtosecond time-resolved x-ray images."



Free electron lasers, which are driven by kilometer-long linear accelerators, emit bursts of short-wavelength light lasting one quadrillionth of a second. As a result, they can act as strobe lights for viewing the fastest events in nature—atomic or molecular motion—and therefore promise to revolutionize our understanding of almost any kind of matter.

Squeezing all of the energy of a continuous laser into short pulses means that femtosecond laser pulses are extremely bright and have the ability to modify a material's absorption or refraction, creating effectively instantaneous "optical shutters."

The researchers showed that ionization itself can be used as a "femtosecond optical shutter" for measuring extreme ultraviolet laser pulses at 31 nanometers.

(Source: Los Alamos National Laboratory)

FLEX007
A SPECIAL DESIGN007 MAGAZINE SECTION

Designing Via-in-Pad for Higher-Density Flexible Circuits

Talking Flex

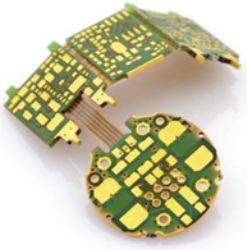
by John Talbot, TRAMONTO CIRCUITS

For flex circuit designs with high layer counts utilizing high density outer layers, the extra area utilized for separate pads and SMT components severely limits the available space for trace fan out. By designing via-in-pad in flex and rigid-flex circuits, it can significantly increase density, utilizing vias as mounting pads. The copper- or silver-filled flat vias allow for soldering components directly on via holes.

Utilizing via-in-pad will release extra surface area for routing of traces. However, like any new technology, there are a few points to be aware of when using this type of construction with flex. When manufacturers fill rigid PCB vias for SMT pads, they are typically filled with a conductive epoxy, copper plated, and then planarized flat. The final sanding leaves a very smooth pad surface allowing the assembler to process the circuit board normally through the pick-and-place cycle.

The via-in-pad technology has progressed so that via fill is very common on rigid PCBs. The

Focused on Flex



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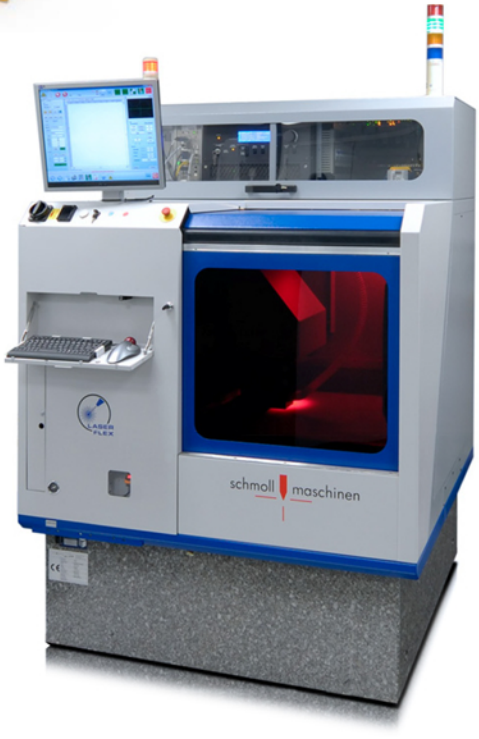

Typical applications:

- Polymer cover foil
- Covered polymer laminates
- Thin, rigid-flex materials
- Inner layers and prepregs
- Separation or decap from tracks
- Structuring cavities
- Micro-via and through-hole drilling

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same equipment utilized on rigid PCBs to perform fill and planarization will crumple a flex panel. A flex panel will not be held stiff enough in the screen fill machine nor will it survive the screening fill process, which presses hard on the surface to drive the thick ink into the shallow hollow of the microvia. Also, the flexible panel will bend and crinkle in the tough sanding planarization machine.

Rigid PCB vias are conductive ink filled after drilling and electroless plating, but before imaging and etching. After an oven cycle to cure the conductive ink, a sanding process is used to flatten the surface and remove any of the conductive fill material from the surface. The resulting surface is quite smooth and ready for dry film. The rigid panel has dry film applied, imaged, developed, and electroplated with copper plating and tin. The dry film is removed, the base copper etched, and then tin stripped. The resulting via surface hole is copper filled and is now reasonably flat copper with a slight dimple, if any.

The via fill operation for flex is quite different. It utilizes a horizontal, flat screen-printing process to fill the vias with conductive ink. Inevitably, some fill material, usually a small bump, is left on the surface of the panel where it is not wanted. This over-screening residue needs to be removed. The residue will be plated over during cap plating, resulting in a possible short when final etch is performed. It is very difficult to remove this unwanted residue on a flex PCB panel. They are too thin and crumple easily when run through a planar sanding machine, which is typically used to remove the hardened fill residue and a small amount of surface copper on a rigid PCB. Due to these difficulties, this method is seldom used on flex microvias or laser vias.

A new and improved process for a flat via-in-pad on multilayer flex is to fill the vias with a special type of copper plating. On thin flex layers that are laser-drilled, the new copper fill plating chemistry is designed to fill the laser via from the bottom up, creating a reasonably flat top on the via. Though some small dimpling can usually be seen, it presents no problem for assemblers. This plating technology is used on a wide range of flex and rigid-flex circuits.

Top flex circuit manufacturers have specially designed copper plating lines which preferentially plate inside the via holes, effectively filling them without plating any significant amount of copper on the panel surface. Excess electroplated copper on the surface is not desired as it would be a less ductile copper where, typically, RA copper for the traces is required for flexibility. Also, any extra copper plating on the trace surface will make it very difficult to etch very small features on outer layers that are typically used on high density designs utilizing via-in-pad technology.

Because the vias are selectively fill-plated with only copper, and resin fill is not utilized, the surface is smooth enough to forgo a subsequent sanding operation. The entire sanding and conductive screening process with the uneven surface topography of the flex circuit is therefore not a problem. The only negative to the copper plating fill process is that the cop-

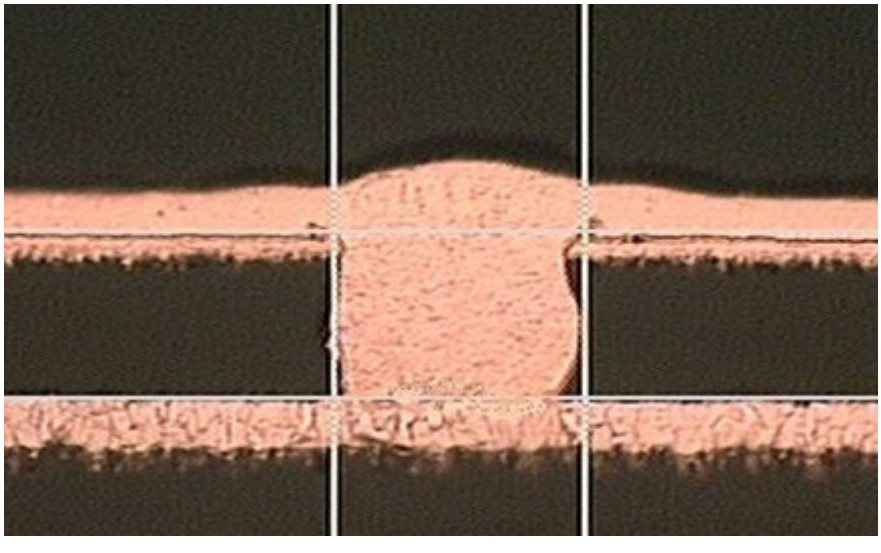
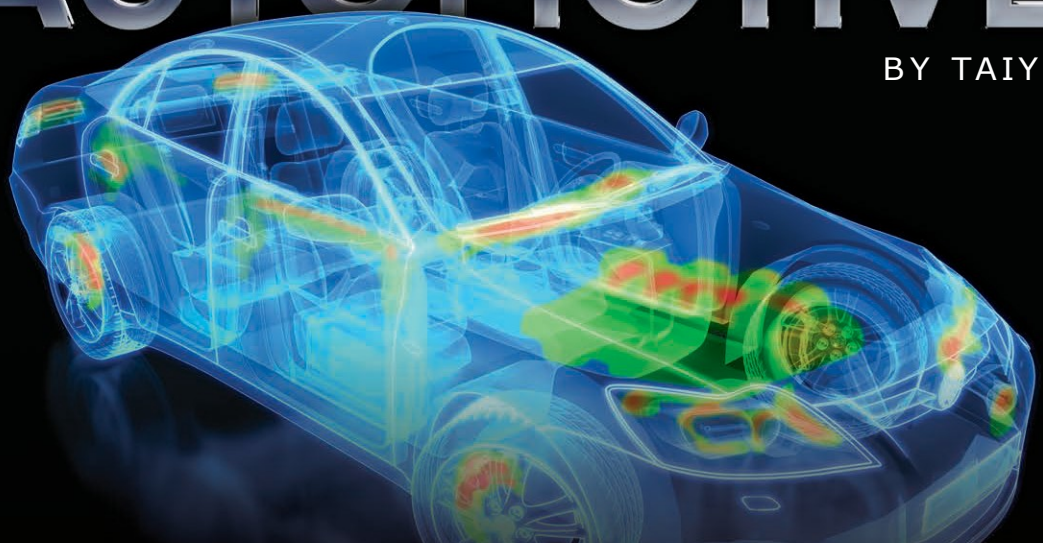


Figure 1: Copper-plated filled via showing the small dimples typically created from copper fill plating.

DRIVING TO THE FOREFRONT OF INNOVATION

AUTOMOTIVE

BY TAIYO



During PCB assembly, cracking is far more prevalent in white solder mask than standard green. So we created PSR-4000 CR01MW to eliminate long term cracking and peeling and meet the harsh environment requirements of the automotive LED market. With an extremely high photo-sensitivity and reflectance than standard glossy white solder mask, this matte finish can be used via screen print or spray applications.

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per-filled vias are sometimes not completely filled flat or have a small outward dimple. The dents and small dimples are not a problem for the assembler. The use of filled copper vias in flex can greatly increases routing area by freeing up via pads and spaces.

Small dimples on very small pads can cause some assembly headaches since the dimple occupies a large portion of the pad surface. The small bump is usually not an issue, but on very small pads such as 01005 chips and small BGAs, the dimple can pose challenges for the assembler. Sometimes the component assembler must modify their tools and processes to deal with the small depressions by adding slightly more solder paste to pads that have a dimple.

Everything I have covered to this point assumes multilayer flex. Rigid-flex can also utilize via-in-pad, and depending upon the application and material stack, the fill method can vary by design. For instance, if the rigid cap layers on a rigid-flex are relatively thick (~0.010" +), they need to be filled with conductive resin and planarized like a rigid PCB. Thinner outer cap layers (0.003" or less) may use the copper plating fill option. For everything between 0.003" and 0.010", it is probably wise to get your flex supplier's input on the best option for your application. **FLEX007**

John Talbot is president of Tramonto Circuits. To read past columns or contact Talbot, click here.

Plastic Logic's Colour Display Revolutionizes Smart Wearables

Plastic Logic, a leader in the design and manufacture of flexible, glass-free electrophoretic displays (EPDs), has announced a new flexible 5.4in colour display that is set to revolutionise smart wearable devices.

Smart wearables, such as jewelry, have become increasingly popular among consumers over the last decade. The problem is most wearable displays are black and white – Plastic Logic is changing all that with its new full-colour display technology.

"Wearable device designers can now source innovative flexible colour display technology to incorporate into applications including smart jewelry, smart clothing and even smart health-tracking devices," said Tim Burne, CEO, Plastic Logic. "Colour really enhances the functionality and look and feel of any smart wearable—in fact, it makes smart wearables even smarter."

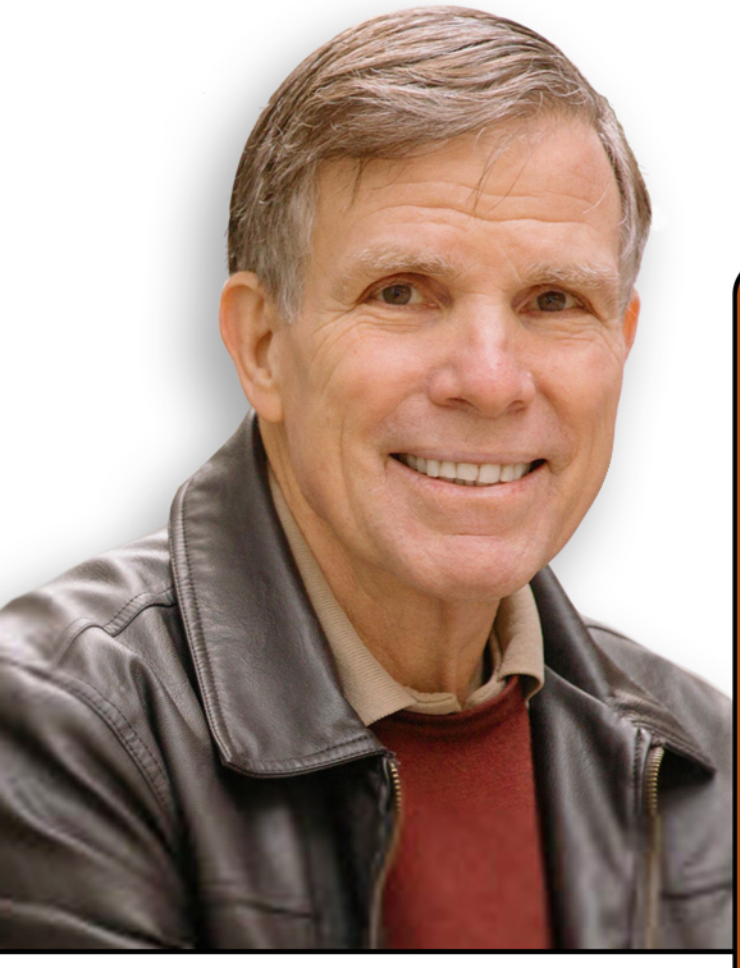
As well as flexibility, which is key to wearables' design, Plastic Logic's displays are extremely robust as well as ultrathin, lightweight and flexible, making them ideally suited for integration into wearables that need to withstand the wear-and-tear of daily usage.

"When it comes to wearable products, we've proved that you don't have to trade visual appeal for functionality," added Tim Burne. "We have already worked with several smart jewelry manufacturers, developing wearable display solutions for their innovative products. There are many more wearable applications that this technology is perfect for."

Plastic Logic's displays are available as engineering samples as well as in volume and can be ordered on request.

(Source: Plastic Logic)

I-007e WORKSHOP



Online Training Workshop Series:

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with Joe Fjelstad

This free on-demand workshop series is a comprehensive look into the structures, applications, materials, and manufacturing processes of flexible printed circuits.

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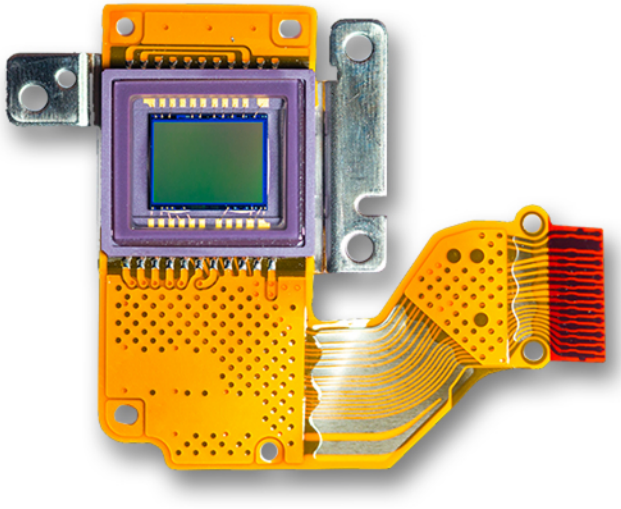

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Flex007 Highlights

Insulectro Picks Paul Welter for Director of Sales for Dupont Chemistry Line ▸

Insulectro, distributor of materials for use in manufacture of printed circuit board and printed electronics, has announced it has promoted industry veteran Paul Welter as director of sales for DuPont Chemistry.

With Flex, Sometimes You Gotta Break the Rules ▸

Sometimes in life, we need to break the rules. For example, in junior high I had a curfew but to have my first kiss, I had to break curfew. I got grounded, but it was worth it! My last article was about reasons to follow IPC design and inspection rules. This time, we are discussing instances where, due to complex requirements, customers are not always able to follow the rules. I will also discuss some design options that will hopefully keep you from "getting grounded."

Averatek Announces A-SAP License Agreement with FTG ▸

Averatek Corporation has announced FTG as an A-SAP licensee. A-SAP is an advanced PCB manufacturing technology that enables feature sizes of 25 microns and below, effectively providing PCB designers with new opportunities to address the challenges of next-generation electronics.

After Decades of E-Textiles Work, a Rising Star Award ▸

After decades of work in my field, I was awarded the Rising Star award during IPC APEX EXPO 2021. I would like to thank my research team, all the colleagues from the D-75A-EU E-Textiles Wearables Standard Task Group in Europe, Chris Jorgensen from IPC, and Sigrid Rotzler, the Task Group vice-chair. Last but not least, I would like to express my thanks to IPC CEO John Mitchell for this award.

Eltek Reports Full Year and Fourth Quarter 2020 Financial Results ▸

Eltek Ltd., a global manufacturer and supplier of technologically advanced solutions in the field of printed circuit boards, announced its financial results for the full year and fourth quarter ended December 31, 2020.

APCT Increases Technology with Rigid Flex Optical Registration from DIS ▸

APCT Inc has added Rigid Flex Optical Registration™ (RFS), developed by DIS Inc of Islandia, N.Y., to enhance their PCB registration capabilities. The RFS machine is built specifically to process difficult flex, rigid, and rigid-flex jobs. Using DIS, Inc proprietary Optical Registration™ technology in conjunction with SmartWeld, the RFS has the ability to align inner-layers and pre-preg without the use of expensive pin-tooling.

Trackwise Appoints Steve Hudson as COO ▸

Trackwise is delighted to announce the appointment of Steve Hudson as Chief Operating Officer. He will support CEO Philip Johnston in executing the company's strategy and vision as Trackwise expands to serve customers in its key verticals: automotive, aerospace, and medical.

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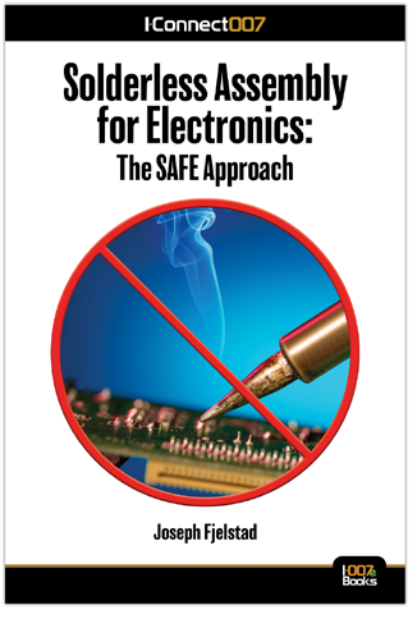
Process Flow for Occam QFN Test Vehicle

Flexible Thinking

by Joe Fjelstad, VERDANT ELECTRONICS

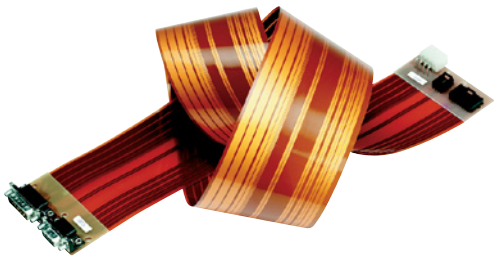
If you have followed my quixotic pursuit to convince the electronics industry of the many benefits of fabricating electronic assemblies without solder over the last 13-plus years, you are likely (or hopefully) familiar with the structures and methods I have advocated to build what I call Occam process assemblies. The solutions I have offered in my writings (there is more than one way to build such assemblies) can significantly reduce the number of process steps required to manufacture an electronic module or assembly (perhaps by as much as one-third) and in the process make electronic assemblies more reliable and less costly by fundamentally focusing on the elimination of solder and the soldering process.



Those who have been in the electronics manufacturing industry for any length of time likely know well that solder and the soldering process are the root cause of most defects and failures in electronics. According to one recent survey, approximately 80% of problems experienced in assembly are related to soldering, including not just faulty soldering but also damage to the PCB structure (delamination) and damaged plated vias.

My effort to teach the Occam process to the electronics industry culminated in a free book titled, *Solderless Assembly For Electronics—The SAFE Approach*. For those who have not yet downloaded and flipped through the pages of this short book, the Occam Process is fundamentally a reverse order approach to manufacturing electronics assemblies; that is, rather than building a circuit board and soldering components to its surfaces, the suggestion is that the industry design and build "component boards" and then build up the circuits on the assembly. Originally, I called it a Reverse Interconnection Process with "RIP" as its acronym, but quickly realized that such an acronym would not instill confidence in prospective users (wink).

In my book, I have listed many reasons why it makes arguable sense to adopt the "SAFE" approach, but for the purpose of this column the focus will be on one benefit that is becoming increasingly important: thermal management of electronic components. Why? Because heat has always been an enemy of electronic assemblies. Every heat exposure above a certain threshold reduces the long-term reliability of an electronic module by a small amount, those exposures have a cumulative effect, and they add up. Moreover, one of the biggest thermal shocks inflicted on an electron-



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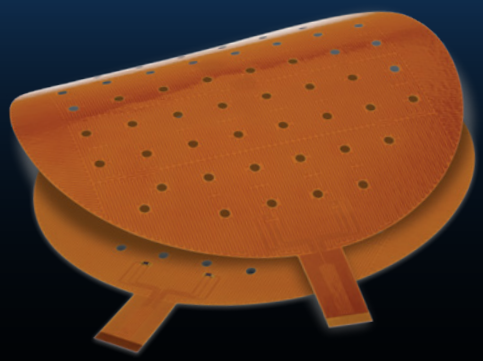

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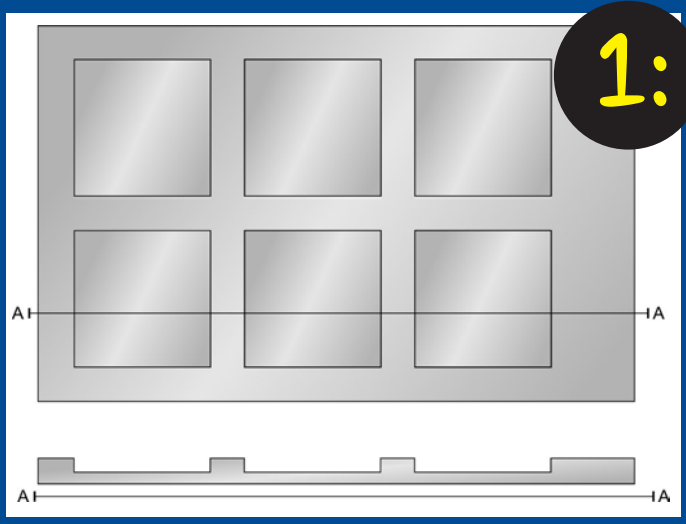
ics assembly during its life occurs during the soldering process, which might happen two, three, or more times during assembly. This can be followed by rework which further degrades the electronics, so approaches that eliminate high temperature exposure (including pursuit of low temperature solders) are "low hanging fruit" from a targeting standpoint.

However, the thermal problem doesn't end there. Heat of operation is another ongoing problem faced by the industry, and QFNs, as attractive as they are, are one of the more vulnerable component types. Over the last several years, QFNs are being increasingly called upon to address electronic module design due to their minimalist size and performance benefit, but making full solder connection to the thermal pad on the bottom of QFNs has been one of the more vexing problems facing assemblers. Thus for the balance of this article, QFNs will be used as exemplar components for this brief discussion and description of a method for building an electronic module that is, in and of itself, a thermal spreader. The series of story board graphics and their accompanying descriptions that together accompany this discussion are provided as a word picture to allow the reader to quickly grasp these concepts.

Illustration of the 12-Step Occam Process

1: Prepare aluminum carrier with cavities to accept packages and tested components. Note: Aluminum can be electrophoretically coated with epoxy or anodized. The base can also be molded or machined of insulating material or copper-clad laminate, if desired, and can be prepared to provide power and ground layers with additional circuitry, if desired, for the design.



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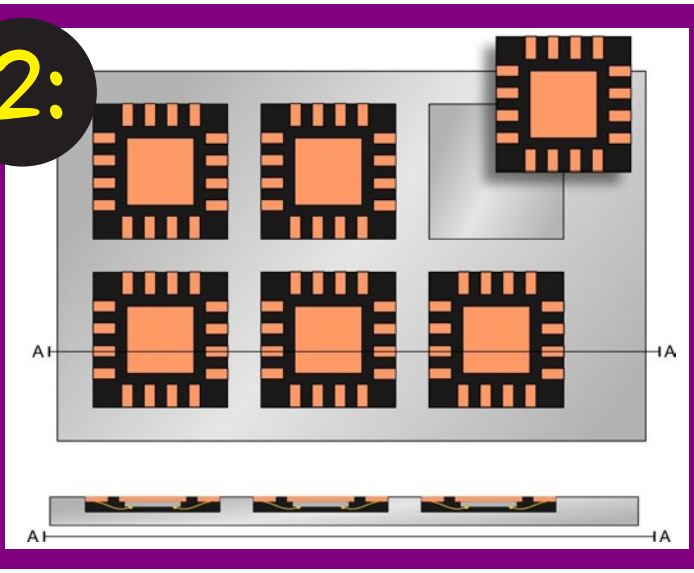

Place and bond components in cavities with copper terminations up. Note: Vent holes can be provided in aluminum base to help planarize components.

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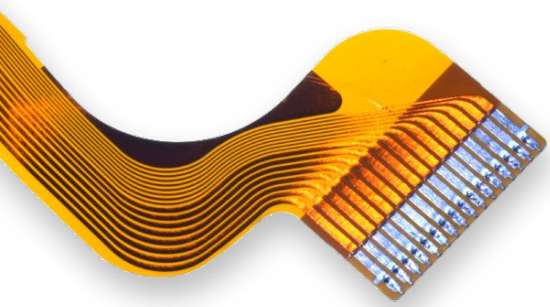

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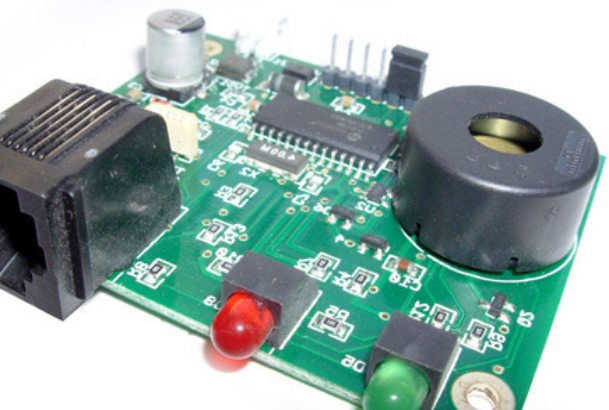

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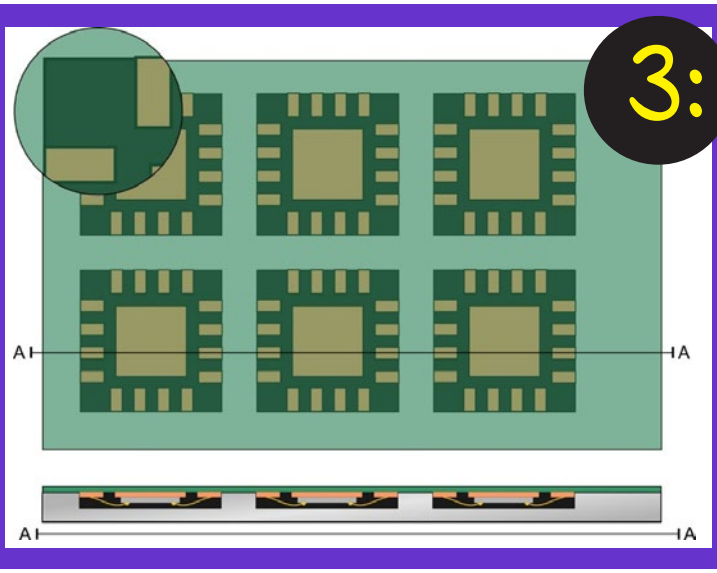
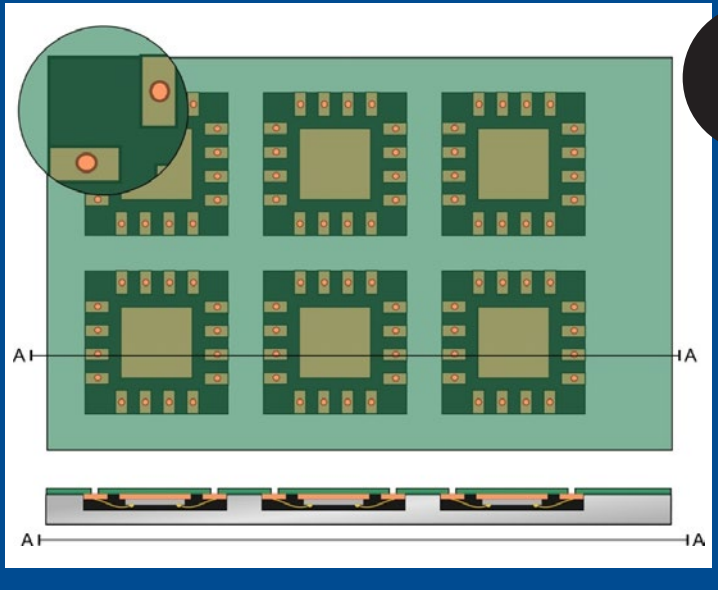
Coat components and carrier with insulating polymer. Note: Polymer can be photoimagable solder mask or polyimide coverlay film.

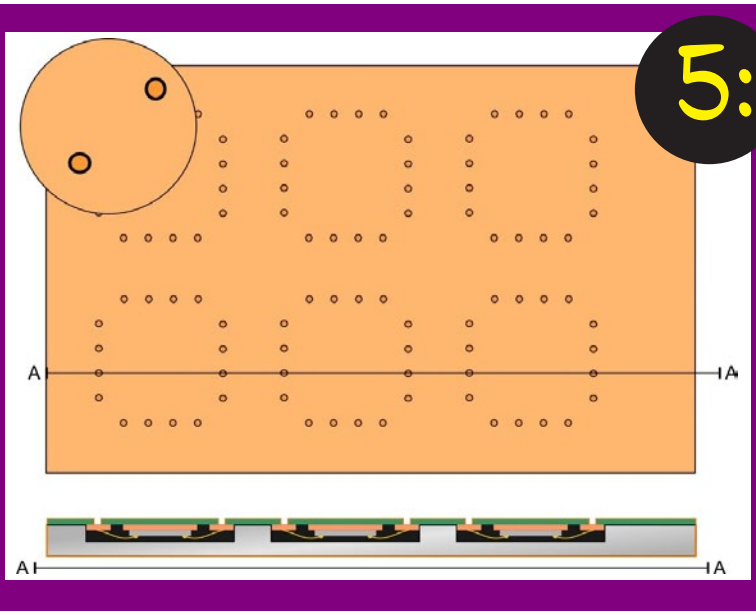




4:

Laser drill or photoform vias down to terminations on packaged components. Note: Holes can be made as small as practical to provide additional routing space.

Coat assembly with copper (e.g. electroless copper or sputtering). Note: Both sides and edges of base can be copper coated.



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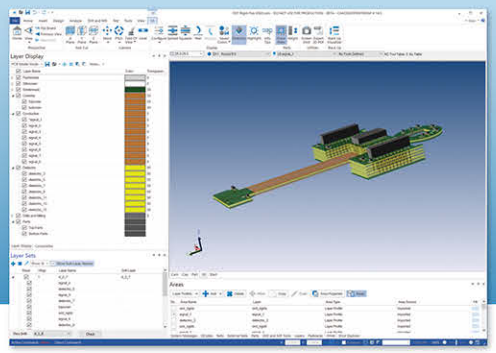

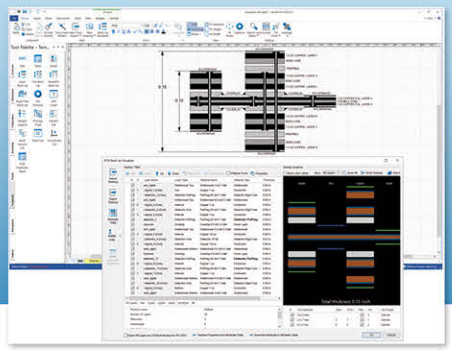

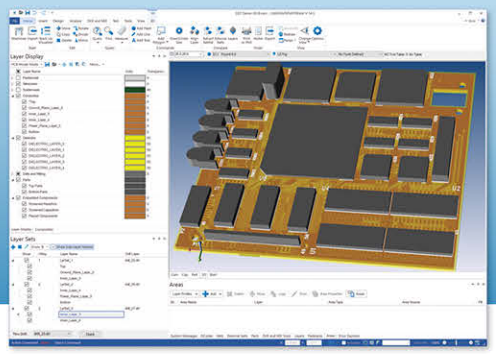

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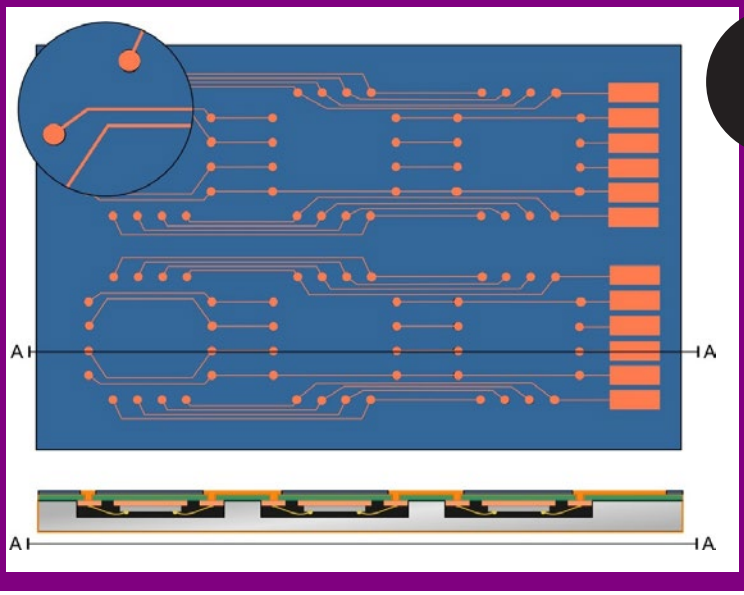
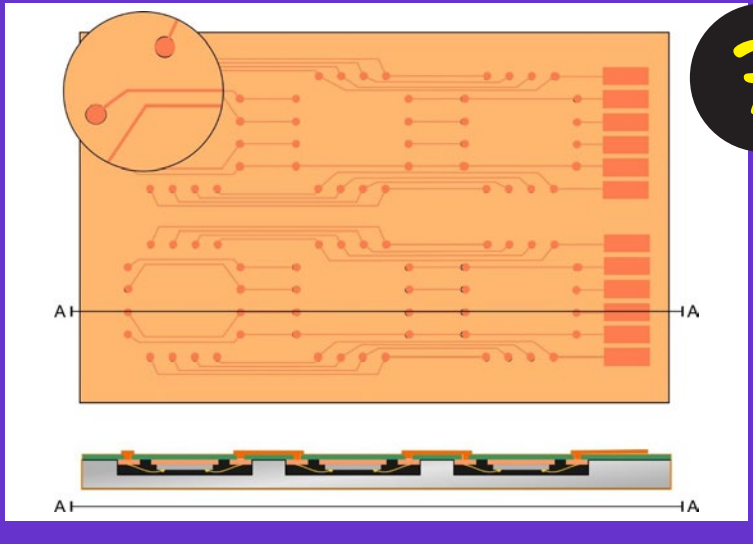


6:

Apply, expose, and develop pattern and plate circuit pattern with copper. Note: Holes and traces are plated up in recessed areas with exposed copper.

Strip plating resist to expose thin copper base and copper circuit pattern.



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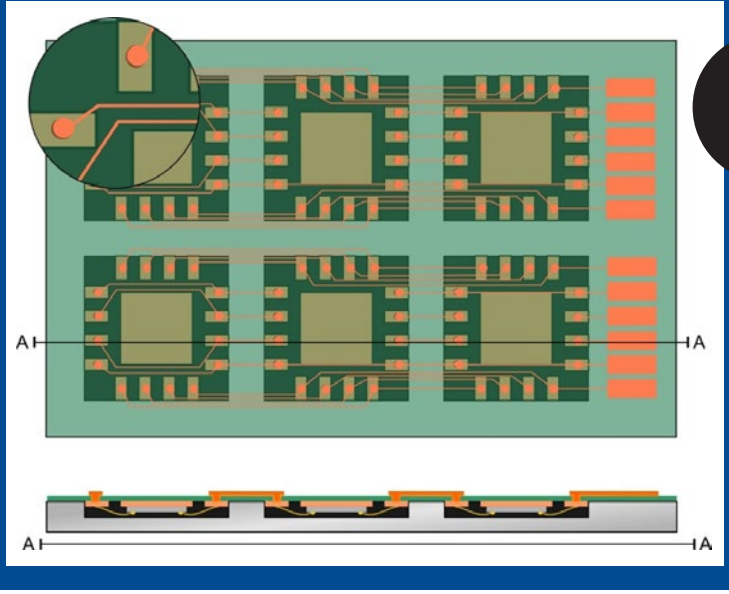

8:

Differentially etch thin background copper to create circuits. Note: Circuits are coated with polymer and the assembly can be provided with additional build-up layers.

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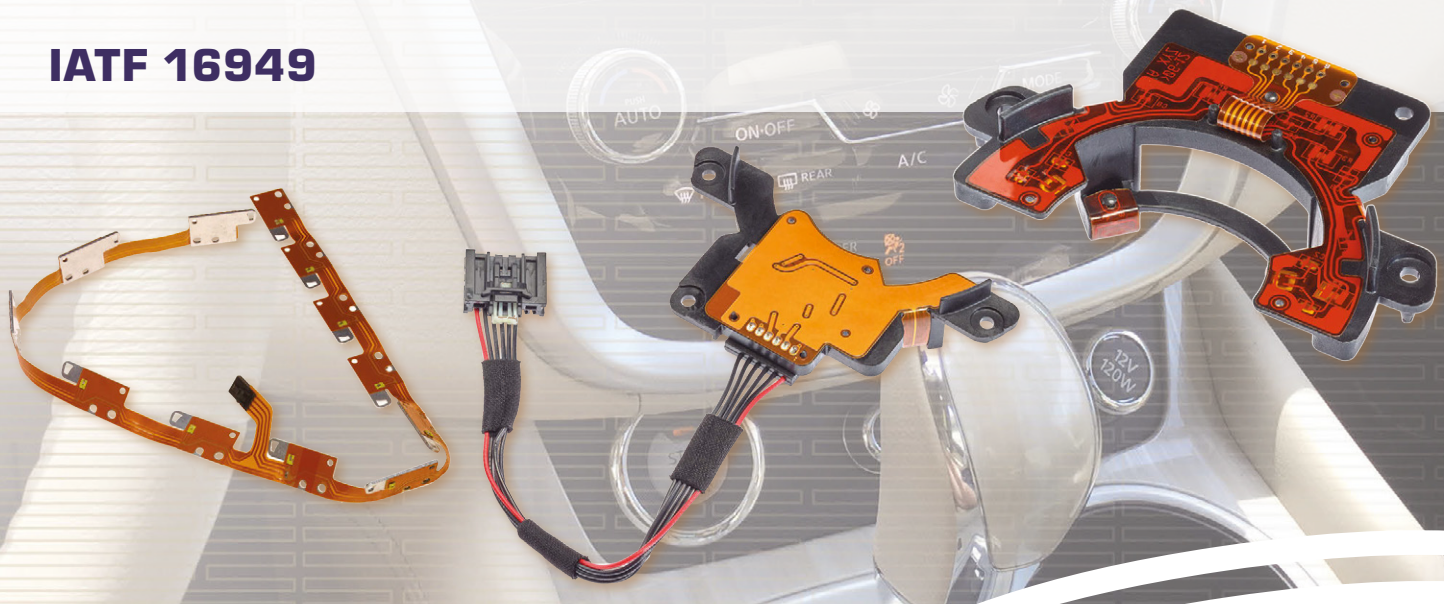

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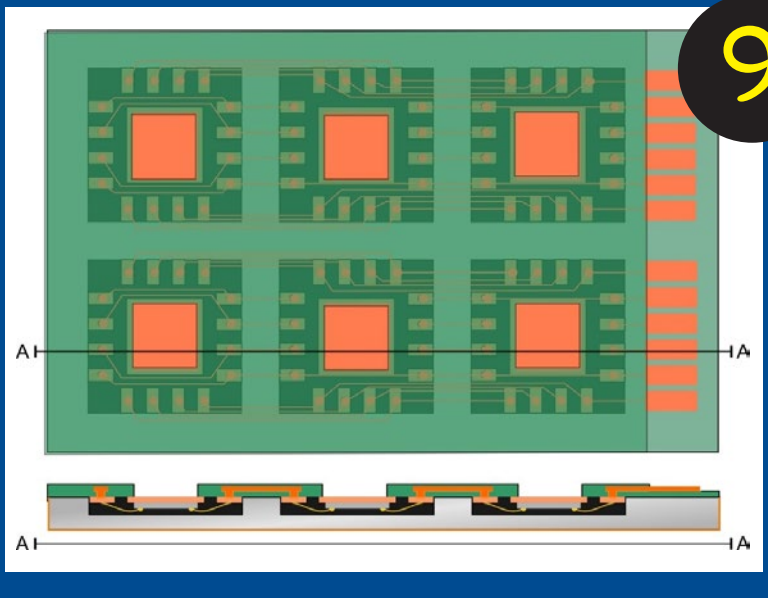
9:

Expose thermal pad using laser or controlled depth routing. Note: Exposure of thermal pad is optional. If left coated it could provide additional routing space.



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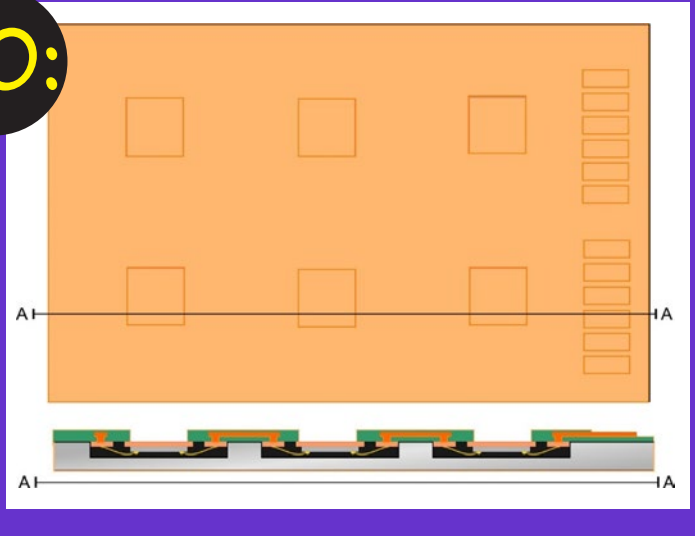
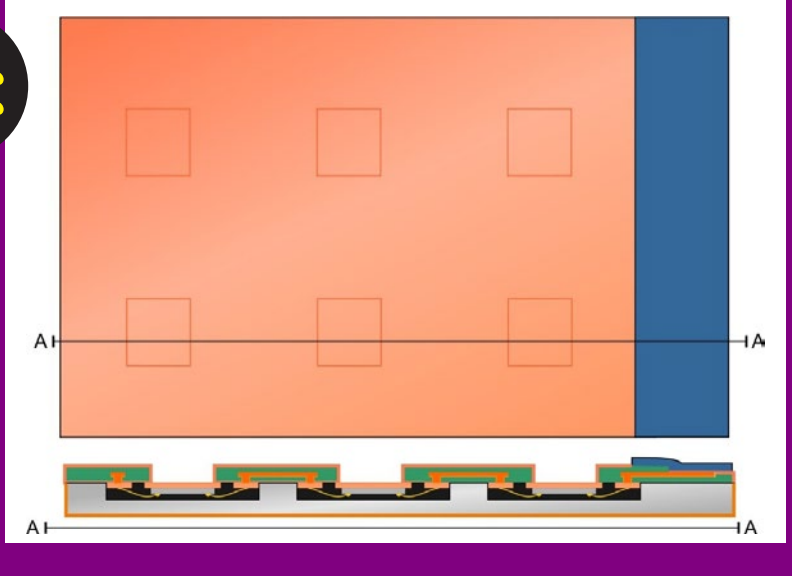
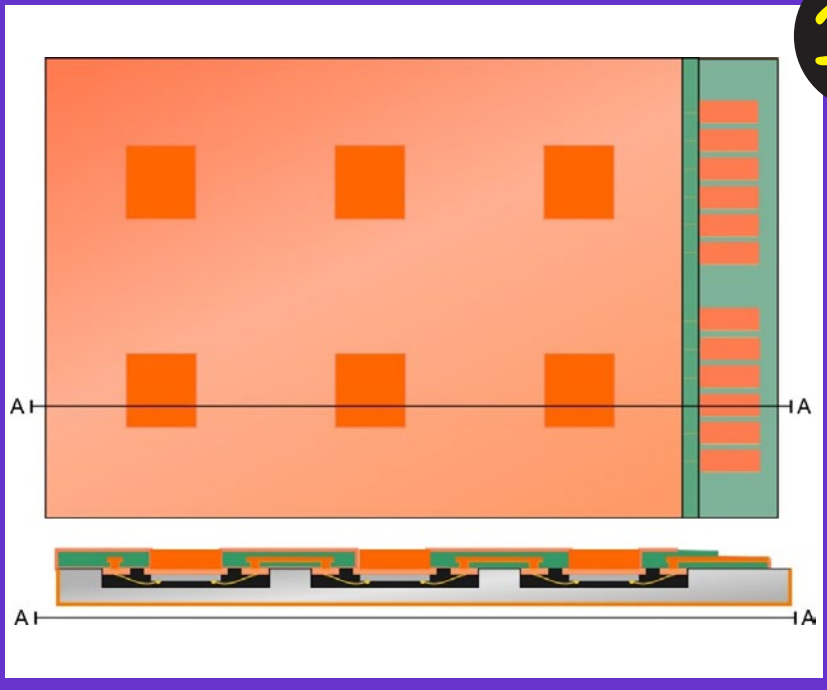


Coat assembly with electroless copper. Note: All surfaces are plated creating a metal encasement for the electronics.

11:

Tape off contacts and electroplate copper over assembly. Note: The tape prevents undesirable extra copper from being plated on contacts.





12: Remove tape, flash etch electroless copper, fill cavities with optional sinterable conductive paste. Note: Metal paste brings thermal pad to surface level for better access to thermal spreader if desired. Assembly with metal jacket is ESD and EMI immune and largely hermetic. Contacts can be gold plated.

Discussion

What has been presented is a novel way to address the increasingly vexing problem that the industry has been battling for decades: effective heat removal from an electronic module. As one of my trusted advisors, thermal management guru Bernie Siegal, shared with me when I first showed him the idea a dozen years ago, "This approach allows the thermal guys to solve the thermal problems on the front-end design rather than at the end."

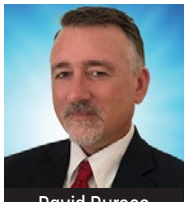
Those who have skill in the manufacture of printed circuits should be able to appreciate the steps shown, and I trust they can also see how it can be done and accomplished using existing materials equipment and processes. No attempt is being made to identify all the prospective materials, both permanent and process consumable, that might be employed. There are simply too many to list, especially when the need to endure the soldering process is removed from the list of requirements and assembly must endure during manufacturing.

Presently there is an effort underway to build out demonstration Occam assemblies to once and for all remove doubt from the minds of those who have adamantly asserted that the concept will not work. As an optimist, I am inclined to share the words of a kindred iconoclast from early in the last century, Henry Ford, who opined: "Whether you think you can, or you think you can't—you're right."

I look forward to sharing the results of the forthcoming efforts with readers when they are available. **FLEX007**

Joe Fjelstad is founder and CEO of Verdant Electronics and an international authority and innovator in the field of electronic interconnection and packaging technologies with more than 185 patents issued or pending. To read past columns or contact Fjelstad, click here. Download your free copy of Fjelstad's book *Flexible Circuit Technology, 4th Edition,* and watch his in-depth workshop series "Flexible Circuit Technology."

1 Fresh PCB Concepts: Does the Assembly Process Damage a PCB? (Part 1—Soldering) ▸


David Duross

Every time a printed circuit board is exposed to soldering temperatures it is damaged. This is the case not only for lead-free soldering applications but also for eutectic soldering consisting of tin-lead.

2 Design Circuit: IPC-2231A—Insights from the IPC 1-14 DFX Subcommittee ▸

In mid-2019, IPC released IPC-2231, DFX Guidelines, a comprehensive guide for establishing best practice methodology in developing a formal DFX (design for excellence) process for laying out printed boards and assemblies.

3 Rising Star Award Winner: Radu Diaconescu ▸

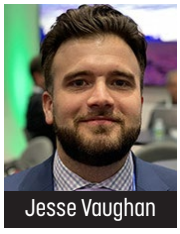

Radu Diaconescu

Last year's IPC APEX EXPO seems to have taken place in a different world. Back then, were a lot of things that we had no clue that we didn't know. The concept of "knowing what you don't know" or figuring out the areas where one lacks knowledge is probably as important as acquiring the knowledge itself.

4 Siemens Introduces PCBflow ▸

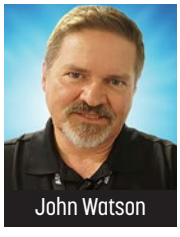
Siemens introduced PCBflow, an innovative cloud-based software solution which bridges the gap between the electronics design and manufacturing ecosystems.

5 Emerging Engineer: Jesse Vaughan ▸


Jesse Vaughan

Jesse Vaughan, a member of the IPC Emerging Engineer program, discusses some of the takeaways from this year's virtual IPC APEX EXPO.

6 Elementary, Mr. Watson: Keeping Counterfeit Components Out of Your Library ▸


John Watson

To know whether anything is wrong, you must first know in detail what is correct to follow the standard or pattern. This principle could not be truer when handling our components in the library.

7 Connect the Dots: The Power Behind the (PCB) Throne—Power Supply Design Tips ▸


Matt Stevenson

Delivering the required power to each component on a PCB can be a complex challenge. Designers have to manage converting AC to DC while also delivering the correct voltage and current to each component. A well-designed PCB results when the designer takes power supply seriously—paying close attention to the effects that power delivery can have on surrounding components.

8 Polar Instruments Driven by Customer Demand ▸


Geoffrey Hazelett

Andy Shaughnessy recently spoke with Geoffrey Hazelett, vice president of sales for Polar Instruments, about the virtual IPC APEX EXPO and the eventual return of live trade shows and conferences. They also discussed some of the company's newest releases, many of which came about through customer demand.

9 Bridging the Simulation Tool Divide ▸


Todd Wetserhoff

Todd Westerhoff of Siemens EDA recently spoke with the I-Connect007 editorial team about the divide between users of high-powered enterprise simulation tools and those who need a more practical tool for everyday use, and how Siemens is working to bridge the gap.

10 EMA Design Automation Expands Operations in the United Kingdom ▸

EMA Design Automation, a full-service provider and innovator of Electronic Design Automation (EDA) systems solutions, announced it is expanding its operations in the United Kingdom with the addition of Parallel Systems to its sales channel.

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For just $750, your 200-word, full-column ad will appear in the "career opportunities" section of all three of our monthly magazines, reaching circuit board designers, fabricators, assemblers, OEMs, and suppliers.

In addition, your ad will be featured in at least one of our newsletters, and your posting will appear on our jobConnect007.com board, which is also promoted in every newsletter.

Potential candidates can click on your ad and submit a resume directly to the email address you provide or be directed to the URL of your choice. If you wish to continue beyond the first month, the price is the same per month.

No contract required. We even include your logo in the ad, which is great branding!

To get your ad into the next issue, contact:
Barb Hockaday at barb@iconnect007.com or +1 916.365.1727 (-8 GMT PST)

I-Connect007
GOOD FOR THE INDUSTRY

smt007 pcb007 pcb design007

Career Opportunities

U.S. CIRCUIT

Plating Supervisor

Escondido, Calif.-based PCB fabricator U.S. Circuit is now hiring for the position of plating supervisor. Candidate must have a minimum of five years' experience working in a wet process environment. Must have good communication skills, bilingual is a plus. Must have working knowledge of a plating lab and hands-on experience running an electrolytic plating line. Responsibilities include, but are not limited to, scheduling work, enforcing safety rules, scheduling/maintaining equipment and maintenance of records.

Competitive benefits package. Pay will be commensurate with experience.

Mail to:
mfariba@uscircuit.com

apply now

INDIUM CORPORATION®

Packaging Engineer

Job description: The Packaging Engineer designs and deploys product packaging to ensure product integrity under varying shipping conditions. This individual is responsible for testing, analyzing, and selecting materials for packaging based on durability, function, ease of use and cost effectiveness. The Packaging Engineer helps ensure that packaging complies with all regulatory requirements.

Requirements: Bachelor's degree in engineering, packaging science and at least one year of related work experience. An equivalent combination of education and related work experience may be considered. Demonstrable skills with computer-aided design (CAD) software and other relevant programs.

Indium Corporation is a premier materials refiner, smelter, manufacturer, and supplier to the global electronics, semiconductor, thin-film, and thermal management markets. Products include solders and fluxes; brazes; thermal interface materials; sputtering targets; indium, gallium, germanium, and tin metals and inorganic compounds; and NanoFoil®. Founded in 1934, the company has global technical support and factories located in China, India, Malaysia, Singapore, South Korea, the United Kingdom, and the USA. Indium Corporation is an Equal Opportunity/Affirmative Action and Minority/Female/Disability/Protected Veteran Employer. We provide a drug-free work environment and a full benefits package.

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Career Opportunities

SIEMENS

Siemens EDA
Sr. Applications Engineer

Support consultative sales efforts at world's leading semiconductor and electronic equipment manufacturers. You will be responsible for securing EM Analysis & Simulation technical wins with the industry-leading HyperLynx Analysis product family as part of the Xpedition Enterprise design flow.

Will deliver technical presentations, conduct product demonstrations and benchmarks, and participate in the development of account sales strategies leading to market share gains.

- PCB design competency required
- BEE, MSEE preferred
- Prior experience with Signal Integrity, Power Integrity, EM & SPICE circuit analysis tools
- Experience with HyperLynx, Ansys, Keysight and/or Sigrity
- A minimum of 5 years' hands-on experience with EM Analysis & Simulation, printed circuit board design, engineering technology or similar field
- Moderate domestic travel required
- Possess passion to learn and perform at the cutting edge of technology
- Desire to broaden exposure to the business aspects of the technical design world
- Possess a demonstrated ability to build strong rapport and credibility with customer organizations while maintaining an internal network of contacts
- Enjoy contributing to the success of a phenomenal team

***Qualified applicants will not require employer-sponsored work authorization now or in the future for employment in the United States. Qualified Applicants must be legally authorized for employment in the United States.*

apply now

APL

JOHNS HOPKINS

CAM / Process Engineer

The JHU/APL PCB Fabrication team is seeking a Computer Aided Manufacturing Engineer to support front-end data processing of APL manufactured hardware. You will directly contribute to hardware fabrication in support of National Security, Military Readiness, Space Exploration, National Health, and Research related to fundamental scientific advancement. This position includes a variable mix of core CAM work scope with additional opportunities for hands-on support such as bare board electrical testing, laser drilling, and mechanical CNC drilling and routing.

Responsibilities:

1. Computer Aided Manufacturing for rigid PCB, rigid-flex, and flexible circuits
   a) Perform design checks, panel layout, coupon generation, file generation, stackups
   b) Support manufacturability reviews with internal APL engineers (customers)
   c) Generate work travelers
   d) Communicate status to supervisors and internal customers
2. Support transition of software tools (Genesis 2000 to InCAM Pro)
   a) Edit design rules checks and generate automation scripts
   b) Develop new ideas to further the technical progress of our product
   c) Develop CAM area through continuous improvement initiatives
3. Interface and inform APL Engineers on PCB design for manufacturing guidelines
4. Operate bare board electrical tester
5. Backup operator for CNC drilling, routing, laser drilling (on-site training)

For more details and to apply:
www.jhuapl.edu/careers and search for CAM.

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Career Opportunities

ventec INTERNATIONAL GROUP 騰輝電子

Customer Service Representative, UK

We are looking to expand our UK Customer Service/ Internal Sales team. As Customer Service Representative you will provide great sales and customer service support and respond to the needs of clients from industries including Aerospace, Defence, Automotive and Pharmaceutical. Duties include:

- Maintain & develop relationships with new and existing customers
- Make rapid, accurate cost calculations and provide quotations
- Accurately input customer orders through bespoke MRP System
- Liaise with colleagues at Chinese HQ and other Overseas Business Units to manage domestic and international requirements
- Assist sales team with reporting, sales analysis and other items at their request

Skills and abilities required for the role:

The ideal candidate is a proactive self-starter with a strong customer service background. Friendly, approachable, and confident, you should have a good phone mannerism and be computer literate.

- Previous experience in a Customer Service background, ideally management or supervisor role
- Experience with MRP Systems
- Good working knowledge of Microsoft Office Tools such as Outlook, Excel etc.

What's on Offer:

- Excellent salary & benefits commensurate with experience

This is a fantastic opportunity to become part of a successful brand and leading team with excellent benefits.

Please forward your resume to HR@ventec-europe.com

apply now

mp Micropack

Micropack Private Limited
Sales Representatives

Micropack is a leading Indian PCB manufacturer with a state-of-the-art facility in Bangalore. Our focus on quality and reliability is demonstrated by the fact that we are certified to Nadcap, MIL 31032 & AS9100, apart from many customer approvals.

Catering to both quick-turn and medium volume requirements, our product range covers:

- Double-sided & multilayer PCBs, up to 30 layers
- Rigid-flex PCBs
- High-copper PCBs
- Hybrid PCBs with FR4+ Hydrocarbon Ceramic Substrates
- Heatsink Multilayer PCBs—Metal core and thermal plate PCBs

We are looking beyond our borders for sales representatives to expand our customer reach in the United States, Europe & South America.

Candidates must have previous PCB sales experience and should understand the technical aspects of printed circuit board manufacturability.

Contact us for more information.
mp3@micropack.in

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Career Opportunities

Indium Corporation: Field Sales Representative

Field Sales Representative serves as lead sales contact and customer advocate to maintain existing sales and to drive new qualifications and sales of products and services through effective account management and coordination of efforts throughout Indium Corporation's Metals, Compounds, Solar and Reclaim (MCSR) organization. This position is ideal for a sales- and customer-focused individual with an engineering degree.

- Develop, cultivate, and follow-up with prospective and existing customers to generate orders
- Develop an in-depth expertise of product offerings
- Work to gain insight into customer activities for future R&D developments
- Respond to customer requests for product data, specifications, and service information
- Identify customer requirements, priorities, and opportunities
- Build strong, trusting relationships with key decision-makers and influencers at target accounts
- Gather competitive insight, including pricing, delivery, and performance information
- Visit customer facilities to observe manufacturing processes and exchange information
- Promote industry recognition of Indium Corporation, its products, and its services
- Be a key member of overall team, including worldwide sales organization, product management, operations, engineering, R&D, etc.
- Submit required paperwork in timely manner
- Work within established budget, while increasing market share
- Perform other duties and projects as assigned

Click below for more details on job responsibilities and requirements.

apply now

Circuit Engineering

Planning Engineer

Experience

- Minimum of 5 years' working within printed circuit board manufacturing industry

Responsibilities

- Review Gerber data and talk with the customer when necessary
- Create production traveler based on Gerber data to release the order
- Improve process capability, yields and cost while maintaining safety and improving quality standards
- Work with customers in developing cost-effective production processes

Quality Engineer/Manager

Experience

- Minimum of 2 years' working within printed circuit board industry
- Possess working knowledge of the IPC requirements and submitting PPAP reports
- Should have knowledge of working with the A16949 certification

Responsibilities

- Perform defect reduction analysis and activities
- Participate in the evaluation of processes, new equipment, facility improvements and procedures

Sales Associate/Customer Service

- Should have a minimum of 2 years' experience
- Salary plus commission

All positions will be on location at Circuit Engineering, 1390 Lunt Ave., Elk Grove Village, Illinois, not remote!

Contact: Felix Simon: (847) 867-7942

apply now

Career Opportunities

We're Hiring!
Atlanta Georgia Facility

ADVANCED CIRCUITRY INTERNATIONAL is a world class supplier of RF/microwave and antenna PCBs. We have four state-of-the-art facilities on three continents to serve our customers. From rapid prototype development to large scale production ramp-ups, we supply many notable OEMs and EMS companies around the world.

As we are anticipating rapid growth for 2021 and beyond, we are recruiting for the following positions:

- Manufacturing manager
- Process engineering
- Sales and business development
- Maintenance management

Qualifications:

- 5-10 years' experience working in the PCB industry
- The ability and drive to learn about our unique product offering
- Excellent written and oral communication skills
- Strong, honest work ethic
- Degree in engineering, operations management, or related field preferred but not required

What We Offer:

- Excellent salary and benefits commensurate with experience

If you want to be part of the upcoming ***5G*** revolution and the growth in RF/microwave and antenna PCB manufacturing, consider a career at **ACI**. Were located in the Northern Atlanta suburbs, where you will enjoy a moderate climate, affordable housing, low taxes, quality school systems and numerous recreational opportunities. Please send your resume in confidence to: Career@aciatlanta.com

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American Standard Circuits
Creative Innovations In Flex, Digital & Microwave Circuits

CAD/CAM Engineer

Summary of Functions

The CAD/CAM engineer is responsible for reviewing customer supplied data and drawings, performing design rule checks and creating manufacturing data, programs, and tools required for the manufacture of PCB.

Essential Duties and Responsibilities

- Import customer data into various CAM systems.
- Perform design rule checks and edit data to comply with manufacturing guidelines.
- Create array configurations, route, and test programs, penalization and output data for production use.
- Work with process engineers to evaluate and provide strategy for advanced processing as needed.
- Itemize and correspond to design issues with customers.
- Other duties as assigned.

Organizational Relationship

Reports to the engineering manager. Coordinates activities with all departments, especially manufacturing.

Qualifications

- A college degree or 5 years' experience is required. Good communication skills and the ability to work well with people is essential.
- Printed circuit board manufacturing knowledge.
- Experience using CAM tooling software, Orbotech GenFlex®.

Physical Demands

Ability to communicate verbally with management and coworkers is crucial. Regular use of the telephone and e-mail for communication is essential. Sitting for extended periods is common. Hearing and vision within normal ranges is helpful for normal conversations, to receive ordinary information and to prepare documents.

apply now

Career Opportunities

Senior Account Manager
Midwest Region

Summit Interconnect, a leading North American manufacturer of advanced technology printed circuit boards across all end-user markets, is seeking an experienced, dynamic leader to drive new business in the Midwest Region of the U.S.

Headquartered in Anaheim, Calif., with additional locations in California and Toronto, Can., Summit's manufacturing features facility-specific expertise in rigid, flex, rigid-flex, RF/MW, and HDI PCBs.

The ideal candidate is highly motivated and should possess in-depth market knowledge, deep contacts across multiple markets and extensive experience in PCB sales with a demonstrated aptitude in proposing engineered solutions to complex requirements.

Reporting to the VP of Sales, the Midwest Senior Account Manager will be the primary hunter in the region and responsible for monitoring customer, market and competitor activity to build appropriate sales strategies for the region, create a strategic plan to grow existing and new business in the region, and be responsible for interfacing across all levels of the organization.

Preference is for the applicant to reside in region and be located within one-day travel to key accounts in the metropolitan business areas. However, the proven professional able to demonstrate reach into the region will be considered regardless of physical location.

Compensation will be a combination of salary and commission, with a comprehensive, competitive benefits package.

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Our Summit Anaheim, CA, division currently has multiple open positions for planning engineers.

The planner is responsible for creating and verifying manufacturing documentation, including work instructions and shop floor travelers. Review lay-ups, details, and designs according to engineering and customer specifications through the use of computer and applications software. May specify required manufacturing machinery and test equipment based on manufacturing and/or customer requirements. Guides manufacturing process development for all products.

Responsibilities:

1. Accurately plan jobs and create shop floor travelers.
2. Create documentation packages.
3. Use company software for planning and issuing jobs.
4. Contact customers to resolve open issues.
5. Create TDR calculations.
6. Assist in the training of new planning engineers.
7. Review prints and purchase orders.
8. Create stackups and order materials per print/spec.
9. Plan jobs manufacturing process.
10. Institute new manufacturing processes and or changes.

Education/Experience:

1. High school diploma or equivalent
2. Minimum five (5) years' experience in the printed circuit board industry with three (3) years as a planning engineer.
3. Must be able to cooperate and communicate effectively with customers, management, and supervisory staff.
4. Must be proficient in rigid, flex, rigid/flex, and sequential lam designs.

apply now

Career Opportunities

Now Hiring

Director of Process Engineering

A successful and growing printed circuit board manufacturer in Orange County, CA, has an opening for a director of process engineering.

Job Summary:

The director of process engineering leads all engineering activities to produce quality products and meet cost objectives. Responsible for the overall management, direction, and coordination of the engineering processes within the plant.

Duties and Responsibilities:

- Ensures that process engineering meets the business needs of the company as they relate to capabilities, processes, technologies, and capacity.
- Stays current with related manufacturing trends. Develops and enforces a culture of strong engineering discipline, including robust process definition, testing prior to production implementation, change management processes, clear manufacturing instructions, statistical process monitoring and control, proactive error proofing, etc.
- Provides guidance to process engineers in the development of process control plans and the application of advanced quality tools.
- Ensures metrics are in place to monitor performance against the goals and takes appropriate corrective actions as required. Ensures that structured problem-solving techniques are used and that adequate validation is performed for any issues being address or changes being made. Develops and validates new processes prior to incorporating them into the manufacturing operations.
- Strong communication skills to establish priorities, work schedules, allocate resources, complete required information to customers, support quality system, enforce company policies and procedures, and utilize resources to provide the greatest efficiency to meet production objectives.

Education and Experience:

- Master's degree in chemical engineering or engineering is preferred.
- 10+ years process engineering experience in an electronics manufacturing environment, including 5 years in the PCB or similar manufacturing environment.
- 7+ years of process engineering management experience, including 5 years of experience with direct responsibility for meeting production throughput and quality goals.

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Now Hiring

Process Engineering Manager

A successful and growing printed circuit board manufacturer in Orange County, CA, has an opening for a process engineering manager.

Job Summary:

The process engineering manager coordinates all engineering activities to produce quality products and meet cost objectives. Responsible for the overall management, direction, and coordination of the engineering team and leading this team to meet product requirements in support of the production plan.

Duties and Responsibilities:

- Ensures that process engineering meets the business needs of the company as they relate to capabilities, processes, technologies, and capacity.
- Stays current with related manufacturing trends. Develops and enforces a culture of strong engineering discipline, including robust process definition, testing prior to production implementation, change management processes, clear manufacturing instructions, statistical process monitoring and control, proactive error proofing, etc.
- Ensures metrics are in place to monitor performance against the goals and takes appropriate corrective actions as required. Ensures that structured problem-solving techniques are used and that adequate validation is performed for any issues being address or changes being made. Develops and validates new processes prior to incorporating into the manufacturing operations

Education and Experience:

- Bachelor's degree in chemical engineering or engineering is preferred.
- 7+ years process engineering experience in an electronics manufacturing environment, including 3 years in the PCB or similar manufacturing environment.
- 5+ years of process engineering management experience, including 3 years of experience with direct responsibility for meeting production throughput and quality goals.

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Career Opportunities

LENTHOR ENGINEERING
MAKING THINGS FLEXIBLE IN A RIGID WORLD®

Sales Account Manager

Sales Account Management at Lenthor Engineering is a direct sales position responsible for creating and growing a base of customers that purchase flexible and rigid flexible printed circuits. The account manager is in charge of finding customers, qualifying the customer to Lenthor Engineering and promoting Lenthor Engineering's capabilities to the customer. Leads are sometimes referred to the account manager from marketing resources including trade shows, advertising, industry referrals and website hits. Experience with military printed circuit boards (PCBs) is a definite plus.

Responsibilities

- Marketing research to identify target customers
- Identifying the person(s) responsible for purchasing flexible circuits
- Exploring the customer's needs that fit our capabilities in terms of:
  - Market and product
  - Circuit types used
  - Competitive influences
  - Philosophies and finance
  - Quoting and closing orders
  - Providing ongoing service to the customer
  - Develop long-term customer strategies to increase business

Qualifications

- 5-10 years of proven work experience
- Excellent technical skills

Salary negotiable and dependent on experience. Full range of benefits.

Lenthor Engineering, Inc. is a leader in flex and rigid-flex PWB design, fabrication and assembly with over 30 years of experience meeting and exceeding our customers' expectations.

Contact Oscar Akbar at: hr@lenthor.com

apply now

LENTHOR ENGINEERING
MAKING THINGS FLEXIBLE IN A RIGID WORLD®

Senior Process Engineer

Job Description

Responsible for developing and optimizing Lenthor's manufacturing processes from start up to implementation, reducing cost, improving sustainability and continuous improvement.

Position Duties

- Senior process engineer's role is to monitor process performance through tracking and enhance through continuous improvement initiatives. Process engineer implements continuous improvement programs to drive up yields.
- Participate in the evaluation of processes, new equipment, facility improvements and procedures.
- Improve process capability, yields, costs and production volume while maintaining safety and improving quality standards.
- Work with customers in developing cost-effective production processes.
- Engage suppliers in quality improvements and process control issues as required.
- Generate process control plan for manufacturing processes, and identify opportunities for capability or process improvement.
- Participate in FMEA activities as required.
- Create detailed plans for IQ, OQ, PQ and maintain validated status as required.
- Participate in existing change control mechanisms such as ECOs and PCRs.
- Perform defect reduction analysis and activities.

Qualifications

- BS degree in engineering
- 5-10 years of proven work experience
- Excellent technical skills

Salary negotiable and dependent on experience. Full range of benefits.

Lenthor Engineering, Inc. is the leader in Flex and Rigid-Flex PWB design, fabrication and assembly with over 30 years of experience meeting and exceeding our customers' expectations.

Contact Oscar Akbar at: hr@lenthor.com

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Career Opportunities

Manncorp

SMT Operator
Hatboro, PA

Manncorp, a leader in the electronics assembly industry, is looking for a **surface-mount technology (SMT) operator** to join their growing team in Hatboro, PA!

The **SMT operator** will be part of a collaborative team and operate the latest Manncorp equipment in our brand-new demonstration center.

Duties and Responsibilities:

- Set up and operate automated SMT assembly equipment
- Prepare component kits for manufacturing
- Perform visual inspection of SMT assembly
- Participate in directing the expansion and further development of our SMT capabilities
- Some mechanical assembly of lighting fixtures
- Assist Manncorp sales with customer demos

Requirements and Qualifications:

- Prior experience with SMT equipment or equivalent technical degree preferred; will consider recent graduates or those new to the industry
- Windows computer knowledge required
- Strong mechanical and electrical troubleshooting skills
- Experience programming machinery or demonstrated willingness to learn
- Positive self-starter attitude with a good work ethic
- Ability to work with minimal supervision
- Ability to lift up to 50 lbs. repetitively

We Offer:

- Competitive pay
- Medical and dental insurance
- Retirement fund matching
- Continued training as the industry develops

apply now

Manncorp

SMT Field Technician
Hatboro, PA

Manncorp, a leader in the electronics assembly industry, is looking for an additional SMT Field Technician to join our existing East Coast team and install and support our wide array of SMT equipment.

Duties and Responsibilities:

- Manage on-site equipment installation and customer training
- Provide post-installation service and support, including troubleshooting and diagnosing technical problems by phone, email, or on-site visit
- Assist with demonstrations of equipment to potential customers
- Build and maintain positive relationships with customers
- Participate in the ongoing development and improvement of both our machines and the customer experience we offer

Requirements and Qualifications:

- Prior experience with SMT equipment, or equivalent technical degree
- Proven strong mechanical and electrical troubleshooting skills
- Proficiency in reading and verifying electrical, pneumatic, and mechanical schematics/drawings
- Travel and overnight stays
- Ability to arrange and schedule service trips

We Offer:

- Health and dental insurance
- Retirement fund matching
- Continuing training as the industry develops

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Career Opportunities

EAGLE electronics Inc.

MANUFACTURERS OF QUALITY PRINTED CIRCUIT BOARDS

Pre-CAM Engineer

Illinois-based PCB fabricator Eagle Electronics is seeking a pre-CAM engineer specific to the printed circuit board manufacturing industry. The pre-CAM Engineer will facilitate creation of the job shop travelers used in the manufacturing process. Candidate will have a minimum of two years of pre-CAM experience and have a minimum education level of an associate degree. This is a first-shift position at our Schaumburg, Illinois, facility. This is not a remote or offsite position.

If interested, please submit your resume to HR@eagle-elec.com indicating 'Pre-CAM Engineer' in the subject line.

apply now

Process Engineer

We are also seeking a process engineer with experience specific to the printed circuit board manufacturing industry. The process engineer will be assigned to specific processes within the manufacturing plant and be given ownership of those processes. The expectation is to make improvements, track and quantify process data, and add new capabilities where applicable. The right candidate will have a minimum of two years of process engineering experience, and a minimum education of bachelor's degree in an engineering field (chemical engineering preferred but not required). This is a first shift position at our Schaumburg, Illinois, facility. This is not a remote or offsite position.

If interested, please submit your resume to HR@eagle-elec.com indicating 'Process Engineer' in the subject line.

apply now

BLACKFOX

Premier Training & Certification

IPC Instructor

Longmont, CO; Phoenix, AZ; U.S.-based remote

Independent contractor, possible full-time employment

Job Description

This position is responsible for delivering effective electronics manufacturing training, including IPC Certification, to students from the electronics manufacturing industry. IPC instructors primarily train and certify operators, inspectors, engineers, and other trainers to one of six IPC Certification Programs: IPC-A-600, IPC-A-610, IPC/WHMA-A-620, IPC J-STD-001, IPC 7711/7721, and IPC-6012.

IPC instructors will conduct training at one of our public training centers or will travel directly to the customer's facility. A candidate's close proximity to Longmont, CO, or Phoenix, AZ, is a plus. Several IPC Certification Courses can be taught remotely and require no travel.

Qualifications

Candidates must have a minimum of five years of electronics manufacturing experience. This experience can include printed circuit board fabrication, circuit board assembly, and/or wire and cable harness assembly. Soldering experience of through-hole and/or surface-mount components is highly preferred.

Candidate must have IPC training experience, either currently or in the past. A current and valid certified IPC trainer certificate holder is highly preferred.

Applicants must have the ability to work with little to no supervision and make appropriate and professional decisions.

Send resumes to Sharon Montana-Beard at sharonm@blackfox.com.

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Career Opportunities

eptac

TRAIN. WORK SMARTER. SUCCEED.

Become a Certified IPC Master Instructor

Opportunities are available in Canada, New England, California, and Chicago. If you love teaching people, choosing the classes and times you want to work, and basically being your own boss, this may be the career for you. EPTAC Corporation is the leading provider of electronics training and IPC certification and we are looking for instructors that have a passion for working with people to develop their skills and knowledge. If you have a background in electronics manufacturing and enthusiasm for education, drop us a line or send us your resume. We would love to chat with you. Ability to travel required. IPC-7711/7721 or IPC-A-620 CIT certification a big plus.

Qualifications and skills

- A love of teaching and enthusiasm to help others learn
- Background in electronics manufacturing
- Soldering and/or electronics/cable assembly experience
- IPC certification a plus, but will certify the right candidate

Benefits

- Ability to operate from home. No required in-office schedule
- Flexible schedule. Control your own schedule
- IRA retirement matching contributions after one year of service
- Training and certifications provided and maintained by EPTAC

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MivaTek Global

MivaTek Global: We Are Growing!

MivaTek Global is adding sales, technical support and application engineers.

Join a team that brings new imaging technologies to circuit fabrication and microelectronics. Applicants should have direct experience in direct imaging applications, complex machine repair and/or customer support for the printed circuit board or microelectronic markets.

Positions typically require regional and/or air travel. Full time and/or contractor positions are available.

Contact HR@MivaTek.Global for additional information.

apply now

Career Opportunities

APCT, Printed Circuit Board Solutions: Opportunities Await

APCT, a leading manufacturer of printed circuit boards, has experienced rapid growth over the past year and has multiple opportunities for highly skilled individuals looking to join a progressive and growing company. APCT is always eager to speak with professionals who understand the value of hard work, quality craftsmanship, and being part of a culture that not only serves the customer but one another.

APCT currently has opportunities in Santa Clara, CA; Orange County, CA; Anaheim, CA; Wallingford, CT; and Austin, TX. Positions available range from manufacturing to quality control, sales, and finance.

We invite you to read about APCT at APCT.com and encourage you to understand our core values of passion, commitment, and trust. If you can embrace these principles and what they entail, then you may be a great match to join our team! Peruse the opportunities by clicking the link below.

Thank you, and we look forward to hearing from you soon.

apply now

Sales Representatives (Specific Territories)

Escondido-based printed circuit fabricator U.S. Circuit is looking to hire sales representatives in the following territories:

- Florida
- Denver
- Washington
- Los Angeles

Experience:

- Candidates must have previous PCB sales experience.

Compensation:

- 7% commission

Contact Mike Fariba for more information.

mfariba@uscircuit.com

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Back by popular (on) demand!

Even though this year's show was a little different,
our coverage is still like nothing the industry has ever seen!

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I-007e EDUCATIONAL RESOURCE CENTER

Learn from the Experts in Our On-demand Video Series

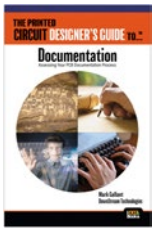
NOW AVAILABLE:
***Implementing "Digital Twin" Best Practices From Design Through Manufacturing with Expert Jay Gorajia*, a 12-part micro webinar series.**

I-007eBooks The Printed Circuit Designer's Guide to...

Thermal Management: A Fabricator's Perspective

by Anaya Vardya, American Standard Circuits

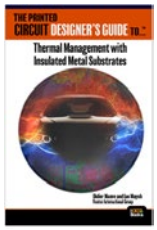
Beat the heat in your designs through thermal management design processes. This book serves as a desk reference on the most current techniques and methods from a PCB fabricator's perspective.



Documentation

by Mark Gallant, Downstream Technologies

When the PCB layout is finished, the designer is still not quite done. The designer's intent must still be communicated to the fabricator through accurate PCB documentation.



Thermal Management with Insulated Metal Substrates

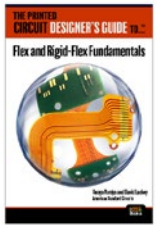
by Didier Mauve and Ian Mayoh, Ventec International Group

Considering thermal issues in the earliest stages of the design process is critical. This book highlights the need to dissipate heat from electronic devices.

Fundamentals of RF/Microwave PCBs

by John Bushie and Anaya Vardya, American Standard Circuits

Today's designers are challenged more than ever with the task of finding the optimal balance between cost and performance when designing radio frequency/microwave PCBs. This micro eBook provides information needed to understand the unique challenges of RF PCBs.



Flex and Rigid-Flex Fundamentals

by Anaya Vardya and David Lackey, American Standard Circuits

Flexible circuits are rapidly becoming a preferred interconnection technology for electronic products. By their intrinsic nature, FPCBs require a good deal more understanding and planning than their rigid PCB counterparts to be assured of first-pass success.

Our library is open 24/7/365. Visit us at: I-007eBooks.com

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