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JANUARY 2021

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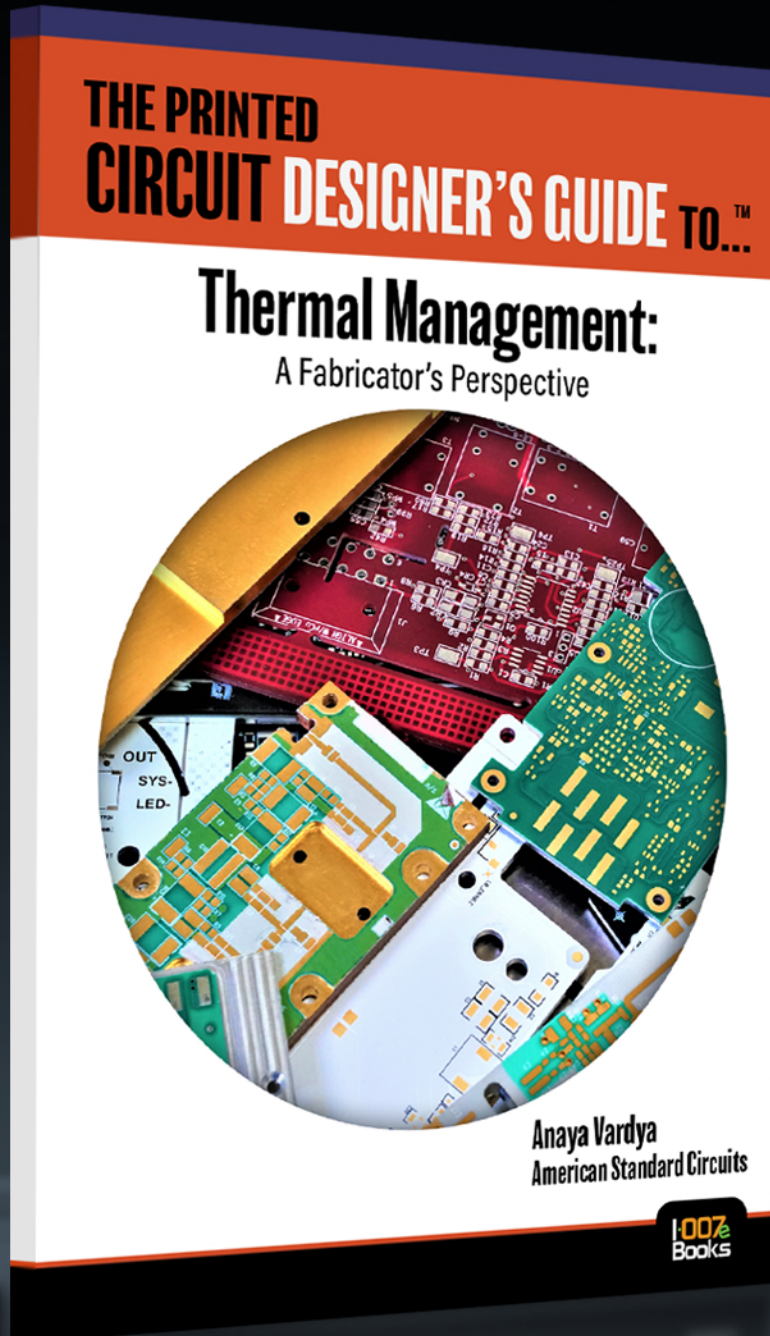
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MAGAZINE

Stackup Design

Designers routinely say that PCB stackup design is one of their more pressing challenges. With proper communication between the fabricator and OEM, coupled with today's CAD tools' stackup functions, stackup design shouldn't be such a problem. But there's still very little agreement about best practices. This month, we peel back the layers and ask, "Who owns the design stackup?"

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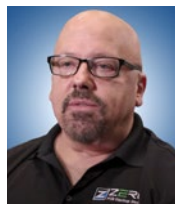


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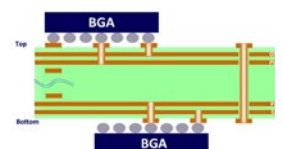
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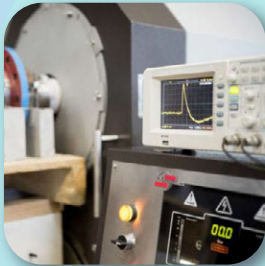


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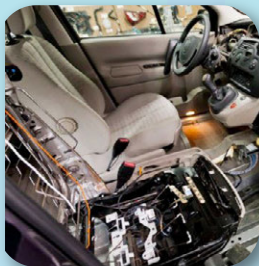
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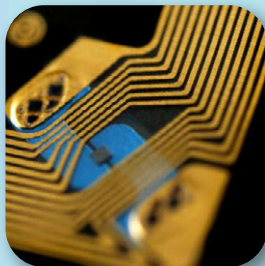
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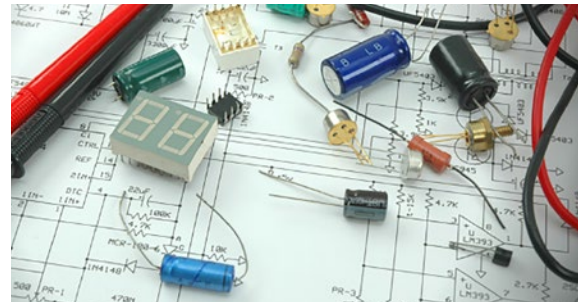
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This Month in Flex

Designing stackups for flexible and rigid-flex circuits presents a slew of unique challenges that rigid designers usually don't have to worry about. But, as we illustrate in this issue, there's nothing too mysterious about flex stackup design. It all comes down to following the process.

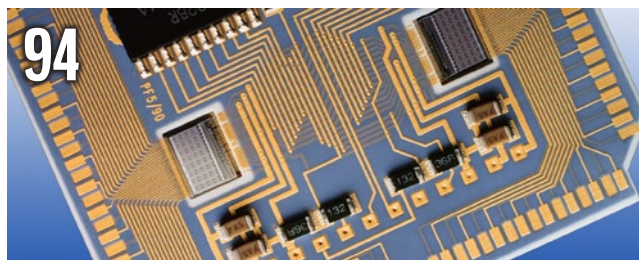
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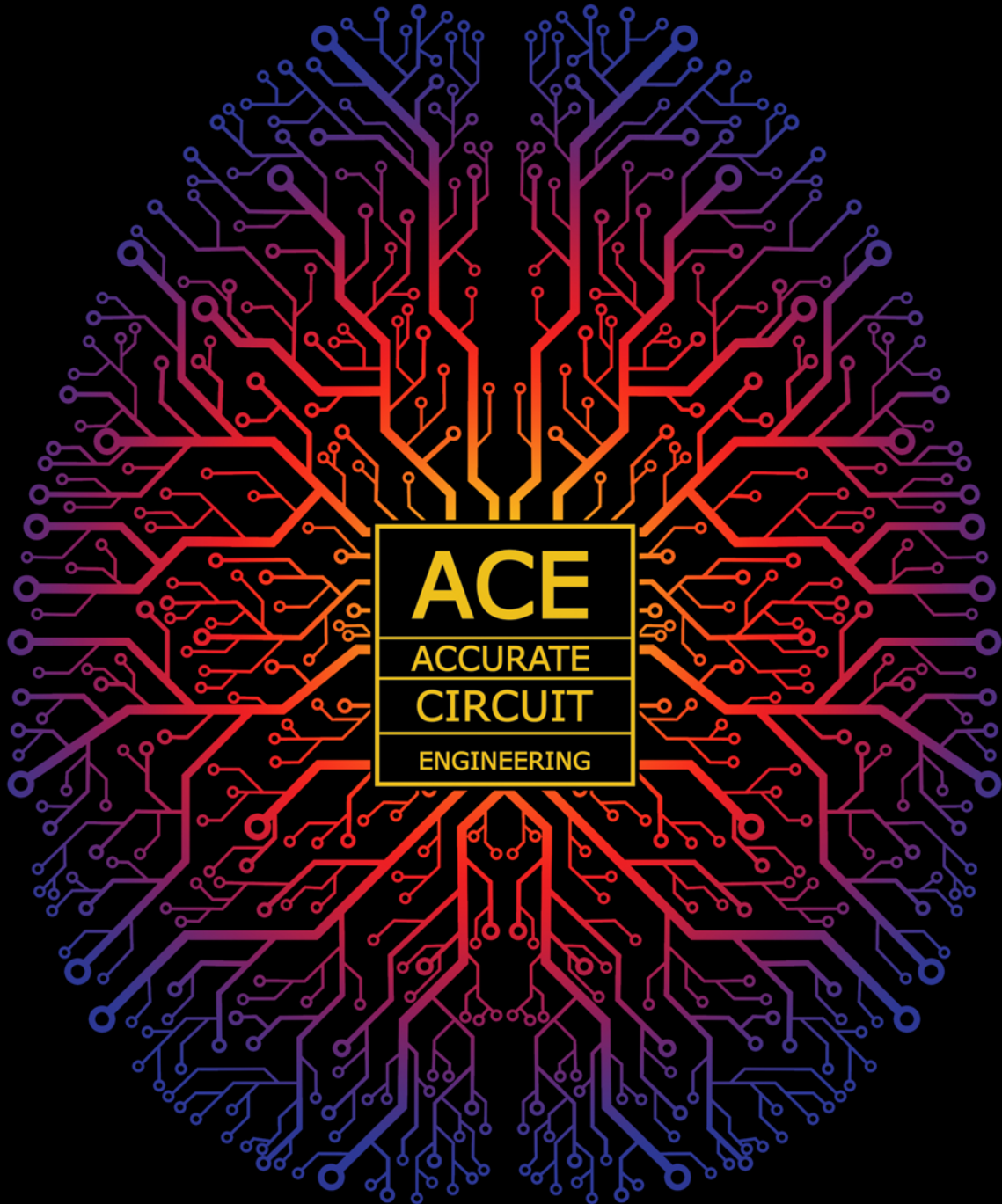
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How Does **Your Stackup** Stack Up?

The Shaughnessy Report
by Andy Shaughnessy, I-CONNECT007

The idea for the January issue topic came about in a familiar way: Several survey respondents named stackup design as one of their biggest continuing challenges.

Here are just a few of the comments we received about stackup problems:

- Choosing too many layers for the stackup
- Last-minute stackup changes
- EDA tool's stackup functions not intuitive
- Not understanding stackup limitations

Stackup design may be the single most important piece of the puzzle in PCB design. Over the years, I've heard designers say, "If you get the stackup right, the design is almost done." Get the stackup right and you're on your way.

With proper communication between the fabricator and OEM, coupled with today's CAD tools' stackup functions, stackup design shouldn't be such a problem. But here's the thing: There's very little agreement about stackup design best practices.

There are hundreds of tradeoffs that must be made, and each decision can cause havoc somewhere else in the stackup. Something as seemingly simple as changing copper deposi-

tion to avoid bowing and twisting can cause trouble with controlled impedance requirements.

If you're using a North American fabricator for your prototypes and an offshore fabricator for volume, you already know that some offshore fabricators can't match your prototype company's "sweet spot" for via and trace sizes. This month, you'll read a few horror stories about stackups that weren't optimized for their fabricator's processes.



Much like opinions, everyone has a different method for doing stackup. Even though conventional wisdom says that your stackup should be finished at the beginning of the design cycle, not all designers follow this dictum. Some designers work with their fabricator to create the best stackup, while others expect the fabricator to design the stackup for them. Many designers just assume that the CAM department is going to make a lot of changes to their stackup, and if they don't hear about these changes, no news is good news, right?

In the end, it all comes down to the simple question of who owns the layer stackup: the OEM, or the fabricator? Many OEMs choose to

let the fabricator do all the stackup heavy lifting, assuming that since the fabricator is going to be manufacturing the board, it's wise to let the fabricator set up your stackup. But does the fabricator have access to all the necessary information?

This month, we peel back the layers of the PCB stackup. We begin with an interview with TTM's Julie Ellis and Richard Dang, who explain the tradeoffs that go into even the simplest design, and why designers and design engineers need fabricators' help to get stackups right. Next, Bill Hargin of Z-zero presents an opposing theory: Only OEMs have all the information needed to create a good stackup, and PCB designers and engineers need to own their design and stop relying on fabricators to do their stackups.

Insulectro's Mike Creeden shares a laminate supplier's view of proper stackup design. Eric Bogatin provides seven tips to remember for your next stackup design, and Cherie Litson offers a handy formula for estimating your PCB's layer count. Try it out.

Our columnists really do some heavy lifting on the topic of stackups this month. Tim Haag breaks down the various challenges that

designers face in creating a stackup. Barry Olney provides an overview of his 30 years in stackup planning, with links to many of his earlier columns on the topic. And Mark Thompson explains why proper stackup design really comes down to communicating your design intent to your fabricator. Martyn Gaudion of Polar Instruments explains why a seemingly simple concept such as layer stackup can be so complex, and what role software tools can play in stackup design. And Tara Dunn helps break down many of the myths surrounding flexible circuit stackup design.

It's 2021 now, and I'm glad to see 2020 in the rear-view mirror. We have a couple of COVID-19 vaccines now, and it's looking like we may be nearing the end of this. The world has come together to fight this thing; there's nothing we can't do if we work together.

I hope to see you in person this year. Have a great 2021! **DESIGN007**



Andy Shaughnessy is managing editor of *Design007 Magazine*. He has been covering PCB design for 20 years. He can be reached by clicking [here](#).

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STACKUP ADVICE

TTM's Approach to Stackup Design: Train the Customer

Feature Interview by the I-Connect007 Editorial Team

In this interview with the I-Connect007 Editorial Team, TTM's Julie Ellis and Richard Dang drill down into stackup design, detailing some of the common stackup challenges that their customers face when designing for both prototype and volume levels, and offering advice to designers or engineers who are struggling with stackup issues. They also discuss why having too many different prepregs in a stackup can be asking for trouble, and how proper stackup design can optimize both the fabrication and assembly processes.

Andy Shaughnessy: Julie, why don't you start by explaining why proper stackup design is so critical.

Julie Ellis: A stackup not only has to meet all of the customer requirements and industry standards, such as IPC-6012, but it also should be designed for best cost for fabrication using the least number of processes and available material that we can buy in time to meet the delivery, and be planned for special requirements,

such as laser microvias or thick copper for high current. For products destined for volume manufacturing, stackups and minimum design guidelines should be verified with the final fabrication site capabilities in mind. We also take into account long-term reliability issues when we create our stackups for very high voltage devices ($> 500V$) that are being driven by the electric vehicle and energy markets.

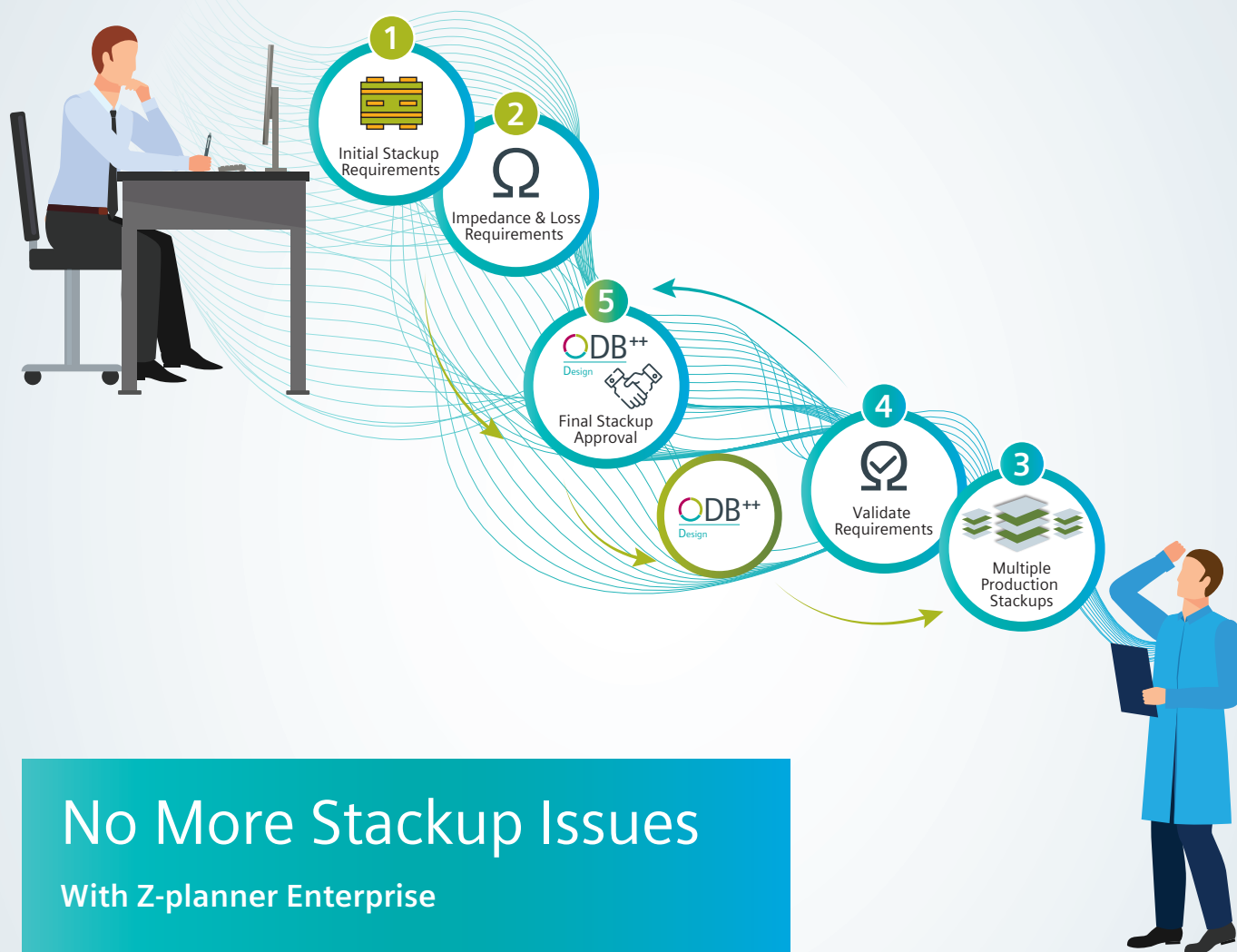
So, there's a lot that goes into a stackup, and it's not only 2D in the vertical cross-section view (Z-axis), where we're trying to figure out the copper layers and the dielectric thicknesses. We need to achieve designs that accommodate registration process limitations in lamination, drilling, plating, and etching, which drive the minimum design guidelines. Depending on the design and the components that the customer is using, we determine the minimum trace, space, pad and via geometries on the horizontal X-Y plane. But it can be kind of difficult for customers to accept minimum



Julie Ellis



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design rules that are slightly larger than they planned when they don't understand all the trade-offs and tolerances that we have to consider in our fabrication processes.

Shaughnessy: It's where the rubber meets the road.

Ellis: It's totally where the rubber meets the road. It's better to plan carefully before you start putting the rubber to the road.

Shaughnessy: That's one of the things that we hear: Some designers are doing stackups as they go.

Ellis: Yes, and if they don't have all the fabricator's input, which they would not necessarily know from their experience and point of view, they can accidentally start a design with extreme features and end up with a finished product that can be manufactured in small prototype quantities, but not in production volumes.

Shaughnessy: I've heard some designers say that if they can get the stackup right, that's 80% of the design, basically.

Ellis: It could be, especially if their fabricator also provides all the minimum design guidelines, before they start routing their circuits.

Shaughnessy: Give us a quick overview of how you work with a customer who has a potential problem with the stackup.

Ellis: With my regular customers, if they have a new product and it's got special requirements, they call me before they even start routing their boards. For rigid designs, we begin by discussing project requirements to determine the subgroup, which establishes which fab sites should be considered, by the complexity of the stackup.

Then we review the specific design attributes shown below, including BGA pitches and geometries, to provide enough information to build the initial stackup:

- Stackup
- Material
- Overall thickness (tol +/-10%)
- Number of lamination cycles (adds cost)
- Layers
 - Number
 - Cu thickness of each layer

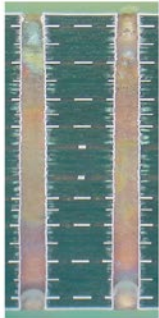

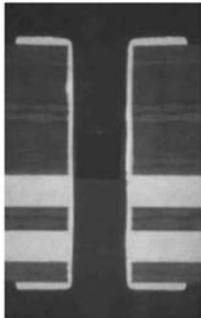

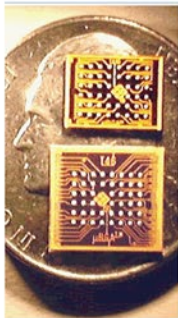
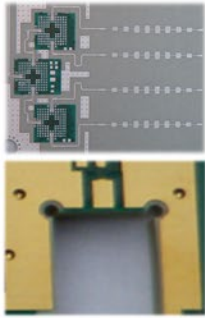
					
Single Lamination Mechanical Drills	Multiple Lam Mechanical Drills	Heavy Copper	Standard HDI > 0.4mm BGA	Micro HDI ≤ 0.4mm BGA	RF and Microwave
<ul style="list-style-type: none"> • Conventional Through-Hole • >0.65mm BGA • Min .008" drill • 4mil line/space • 10:1 aspect ratio 	<ul style="list-style-type: none"> • Blind vias • Buried vias • Through Hole • Min .008" drill • 10:1 Aspect Ratio • Lamination cycles = press+drill+plate • Significant cost 	<ul style="list-style-type: none"> • > 2oz. Cu foil • Up to 12 oz. Inner Layers • High Voltage/Amps • Single or multiple lam • Increased lines/spaces for etch capability • Special-order material • Increases cost & lead time 	<ul style="list-style-type: none"> • 4mil laser uvias • 10mil pads • Offset uvias • 3mil min lines • 1 or more lams • Offset uvias • Stacked uvias 	<ul style="list-style-type: none"> • 3-4mil laser uvias • 8.8mil pads • 2.3mil lines/spaces • Stacked uvias • Multiple lam cycles • CONTACT TTM 	<ul style="list-style-type: none"> • Advanced materials • Cavities • Horizontal Launch • Filters , antennas • Controlled etch • Hybrid stack-ups • Multiple lam cycles • CONTACT TTM

Figure 1: Rigid PCB conventional and HDI subgroups. Pick the simplest subgroup that your design can conform to.

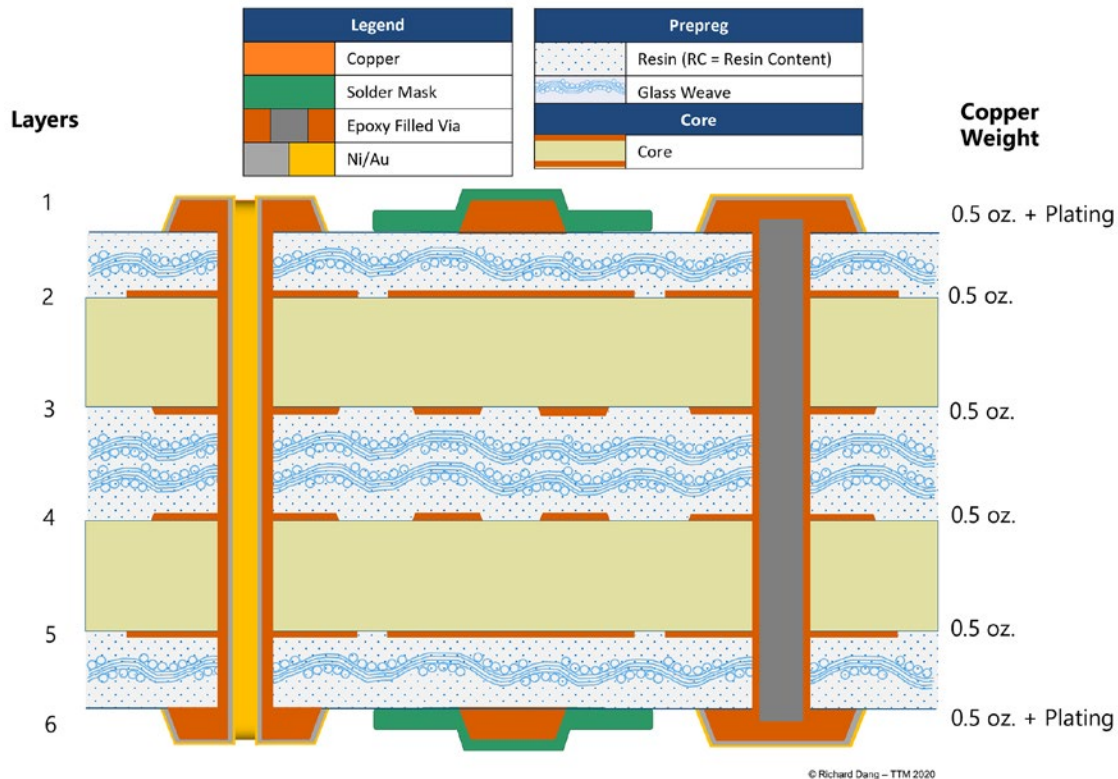
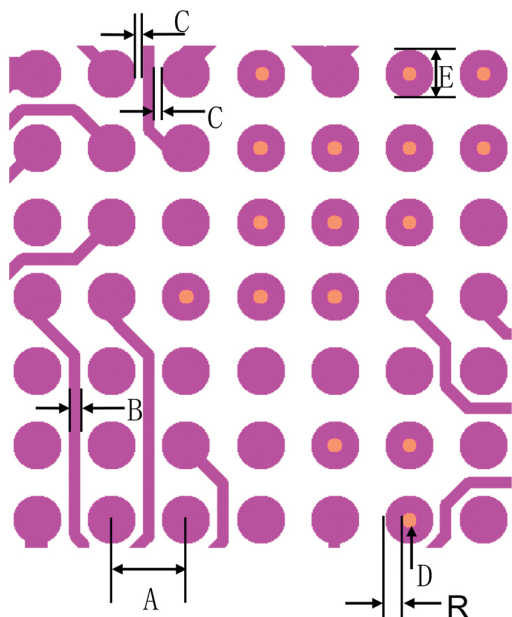


Figure 2: Single lam stackup with filled vias.

- Signal, plane (PWR/GND), or mixed copper density assignment for each layer
- Controlled impedance requirements (with reference layers) per layer
- Minimum pitch of BGA or other special components that will require fan-out and the drill structures
- Drill structures, including start/stop layers for μ vias
 - Minimum drill/pads/antipads for all layers
 - Verification of VIPPO (non-conductive epoxy via fill in pad, Cu plated over)
 - Confirm laser microvias, offset or stacked (buried stacked microvias should be solid Cu-filled). Skip blind vias.
 - Backdrills (confirming starting and do-not-cut layers, drill/antipad diameter)
- Minimum lines/spaces requested
 - Internal layers, etch only
 - Plated layers, whether internal or external
- Any special dimensional requirements affecting etching, routing, drilling, and lamination

For example, when we're trying to route a 0.5 mm pitch BGA, which we know automatically means it's a laser microvia board, we'll get on WebEx so they can share the BGA pad configuration. With knowledge of how many rows of balls or pads there are on the device, my customer can figure out how many layers they need, and then we try to optimize the fan-out to route all those rows of pads in the lowest number of lamination cycles as possible (Figure 3).

Once my prelim stackup is approved by the customer, I have the factories (quick-turn prototype and volume site, if necessary) provide their site stackups and confirm the design rules, the minimum lines and spaces on each layer, the minimum drill and pad diameters, and the controlled impedance lines and spaces. We provide all that information so the customer has the design rules to put into their CAD program before they start.



Item	Mark	DFM Suggestion(mm)	
BGA pitch	A	0.5	0.4
μVia pad	E	0.25 (10-11mil)	0.20 (9mil)
Line width	B	0.075	0.075
Space	C	0.0875	0.0625
μVia diameter	D	0.10	0.075
μVia ring	R	0.075	0.0625
Copper thickness	/	H oz.	H oz.

Figure 3: 0.5 mm and 0.4 mm BGA pitch with one line, for inner layer.

Shaughnessy: You're sort of like an intermediary between the designer and the circuit board shop, in a way?

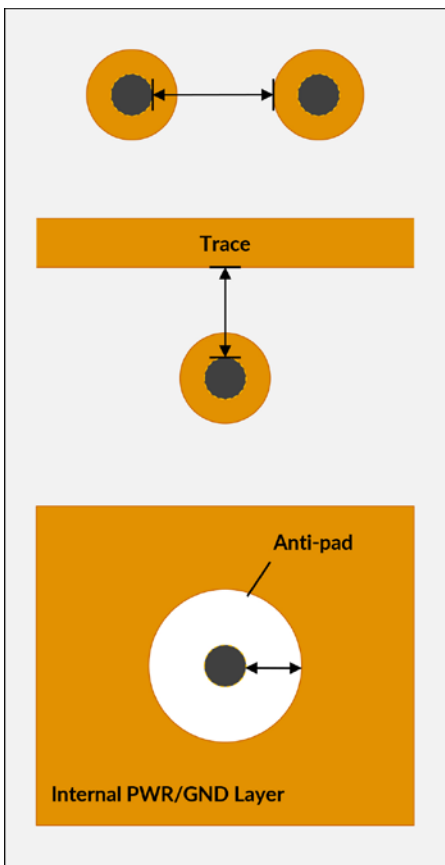
Ellis: Yes, I'm the person who will translate information going both directions. I share fabrication knowledge with customers for their projects, so they can confidently make informed design decisions that align with fabrication capabilities.

The key manufacturability considerations and standard design guidelines (which can be improved upon engineering review) that all design engineers would benefit from understanding are listed below. We have to take all of these into account if we are creating stackups in the vertical plane (microsection view) that accommodate the component and drill connection requirements in the horizontal plane (TOP or BOT view):

- 1) Aspect ratio: The ratio of thickness being drilled to the drill diameter to assure compliant Cu plating thickness inside the hole walls
 - a. Plated through-hole (PTH), mechanical drill: $\leq 10:1$ – thickness drilled should not be more than 10X the drill diameter

- b. Blind microvia, laser drill: $\leq 0.75:1$ —the drill diameter is 33% larger than the thickness drilled
- 2) Pad diameter, tangency, no break-out (accommodates misregistration of drill and Cu etching):
 - a. Mechanical drill, through-hole: = drill diameter + 10 mil
 - b. Laser drill, blind hole: = drill diameter + 5 mil (note the space-saving potential here, but these are shallow, blind vias that can't go all the way through the board)
- 3) Etched lines: Increase in width as Cu thickness increases, refer to fabricator tables
- 4) Etched spaces: Increase in width as Cu thickness increases, best if larger than adjacent lines by 0.5–1mil in dense circuitry due to artwork compensation that increases the lines to achieve the designed line after etching
- 5) Etched line widths are slightly different for plated versus unplated layers, because plated layers include starting Cu foil + surface plating that occurs when plating the hole walls

- 6) Non-conductive epoxy-filled vias with Cu cap plates: add 0.5 mil to outer layer space—difficult for ≤ 0.5 mm pitch BGAs
- 7) Controlled impedance lines:
 - a. Increase/decrease with dielectric thickness
 - b. Become very small for small microvia dielectrics, so watch factory minimum line etch capabilities when < 3.5 mil. But watch aspect ratio on the microvia when increasing the dielectric to increase the linewidths
 - c. Decrease with increased ohms
- 8) Minimum drill hole wall to different net Cu (drill-to-Cu) = 8 mil, (Figure 4) the sum of the following:
 - a. Imaging: front-to-back = ± 0.002 " (50 μm)
 - b. Lamination: layer-to-layer registration = ± 0.003 " (75 μm)
 - c. Drill: drill tolerance = ± 0.003 " (75 μm)



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Figure 4: Drill-to-Cu minimum of 8 mils.

Let's face it: when well-informed customers are creating designs in accordance with standard guidelines from the fabricators, they're going to have high yields and be easier to run through our shops. And with higher yields, they're going to be more cost-competitive, and they will be less prone to failures. It makes all of our jobs easier, which is why we invest in "training" our customers.

Shaughnessy: But things go badly sometimes, and you have some great horror stories that you share with your class.

Ellis: One of the designs I'd been asked to review for quote was from a super-nice independent designer, and it was a medical application. He had used the component manufacturers' reference designs off the two 0.5 mm (19.6 mil) pitch BGAs in the schematic. Both designs specified 5-mil vias and 9-mil pads through all six layers, a blatant violation of pad diameter for a mechanically drilled PTH. Luckily, Asia suppliers had already no-bid the job, so I didn't have to be the one to drop the "your design can't be fabricated in any volume" bomb.

This one was actually designed as a through-hole design when it really should have been a laser microvia board with a different stackup. Luckily, we were able to fix the design by adding one lamination cycle for microvias on L1-L2 and L2-L3 to the stackup and re-routing some circuitry to achieve what we needed to make it manufacturable.

Unfortunately, one of the things that I sometimes worry about is when the semiconductor manufacturers supply reference designs they have only used with their local, quick-turn fabricators. Since they haven't designed those for volume production, their customers can get into a bit of a wicket when they try to transfer those often-tested and approved designs.

Happy Holden: Yes. Don't talk to us about app notes (laughs). We went through that discussion with the June 2020 issue of *Design007 Magazine*.

Ellis: Absolutely, Happy. Some of the most difficult designs that I see are reference designs from semiconductor customers. We just had another one recently from one of my automotive customers. They used one of their offshore divisions to design a respin of a board that the original designer and I had spent a lot of time on together. It had two high-pin-count 0.65 millimeter-pitch BGAs. They designed them as through-holes, which violates 8-mil drill-to-copper. When it came across my desk, it was being manufactured locally at TTM in San Jose, with a 6-mil drill that we don't normally use in China, and my gut just caved, because I'm thinking, "Did I actually lead them into a design like that?"

When I brought it up, the design engineer said, "No, Julie, we inherited this one, where the 0.65-mm BGAs were added; we know we need to redesign it." So now we're working on the redesign for volume production that is also high reliability for automotive. In this case, a 0.65-mm pitch BGA using an 8-mil drill hole violates guidelines for 8 mil minimum drill-to-copper. We need to be careful of high-volume designs in China. We will be able to meet the 8 mils through very clever re-routing and off-setting via pads.

Shaughnessy: How do you go about navigating this, if you're having your prototype built here, and then they want to build it offshore for volume? I mean, it seems like a delicate kind of dance.

Ellis: Oh, it's so scary. There's nothing worse than having to call a designer and say, "Hey, I'm having problems with this finished design, with this stackup, because we can't fabricate it in Asia." But how would a design engineer who has expertise in electronics design know all of this? They can't know everything that I know. I've been doing this for 30 years, which is why they should contact us at the start of their project.

Shaughnessy: What are some of the other more common mistakes that you keep seeing?

Ellis: A big one is always VIPPO, via-in-pad plated over, when we have non-conductive epoxy-filled holes in a through-hole board with semiconductor or passive components-pads that have vias in them. For the assembler to effectively solder those and not have all the solder flow through the holes, we need to fill those with non-conductive epoxy and then Cu plate them, so the pad, even though it has a hole in it, just looks like a rectangular pad that the assembler can solder to without solder going down through the hole.

The via-in-pad plated-over process takes extra process steps, so it's significantly more expensive and it also adds plating to the outer layers of the circuit board; when we add the non-conductive epoxy fill, we need at least 0.5 mil more spacing between the fine lines. We also need to recalculate controlled impedance line widths, which become slightly smaller as the Cu thickness increases. Circuit board design engineers don't always think of the ramifications of via-in-pad and how that's going to affect etching or assembly.

Richard Dang: Aspect ratio for microvias is another one. I've seen designers come to us with a stackup on their fab drawing, they're specifying dielectrics, and then they put a microvia in there and they're specifying the microvia size. We see that sometimes designers might not understand that there's an aspect ratio of $\leq 0.75:1$ that we have to comply with in order to successfully plate that via.

Any time there are microvias, it limits the dielectric thickness between those layers, which will result in small-modelled line widths for your impedances. Your trace and space are also limited by the distance between your microvia pads.

A final issue with microvia layers is that different factories have different plating capabilities, so the resulting plated layers may differ in nominal Cu thickness by 0.2–0.3mil when



Richard Dang

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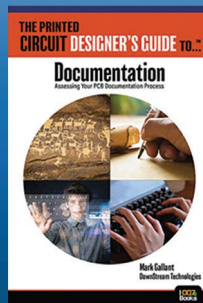
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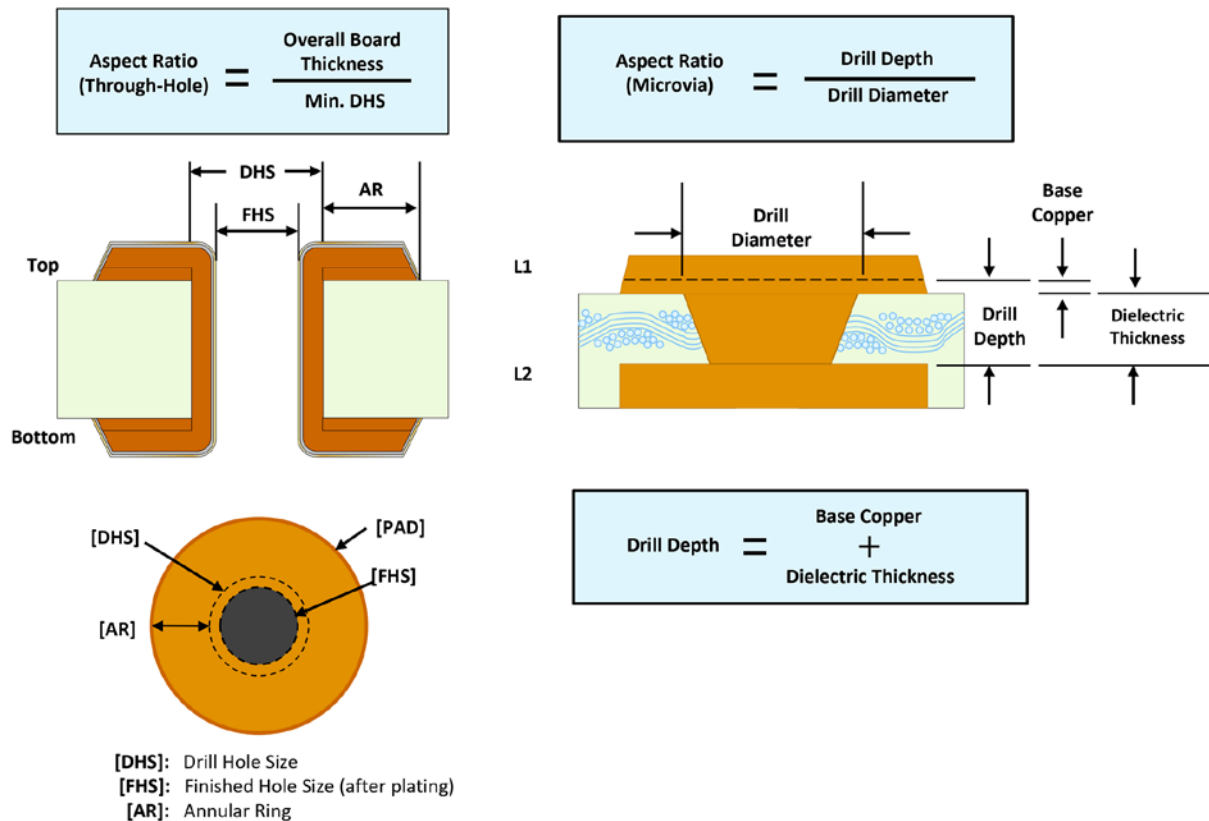


Figure 5: Aspect ratio measurements for typical through-hole vias and microvias.

transferring between sites, and we request customer approval for this (Figure 5).

Ellis: Figure 6 shows what Richard is talking about. With laser microvias, stackups get really complicated, quickly.

This one has a L1–12 through-hole. It's got another mechanical through-hole creating a buried via in the middle of the stackup in the first L4–L8 sublamination, and then it also has all these microvias, L1–4 offset ($\geq 0.5\text{mm}$ BGAs) and L9–12 stacked ($\leq 0.5\text{mm}$ BGAs). Basically, the way we build this board is through the four lamination cycles starting with the L4–L8 sublam which entails laminating the layers, drilling, plating, and etching. The next sublam repeats the processes, adding layers above and below the first sublam, laminating, drilling, plating, and etching, and then adding more layers above and below again, and so on. Every lamination cycle adds multiple processes, resulting in additional costs. So a good designer works to reduce lamination cycles.

These are the kind of examples that we see, where customers have a requirement, they've planned for what they think works, but then process and geometry really don't work when we put all the different features together, and we request they adjust their design.

Shaughnessy: Right. It seems like they would want to have some communication for something like this.

Ellis: Yes, to plan ahead. Another common one that I'm actually working on right now is that we have a board that was designed per IPC-class 2, but somebody slapped an IPC Class 3 fab note on it and then expects us to achieve it. But we can't, because Class 3 has larger design rules—namely, larger annular rings that take up space in a fixed design and thicker copper plating on the hole walls and surface that affects outer layer etching—than Class 2. It's more a fabrication than a stackup issue, but that is a common problem that we've seen.

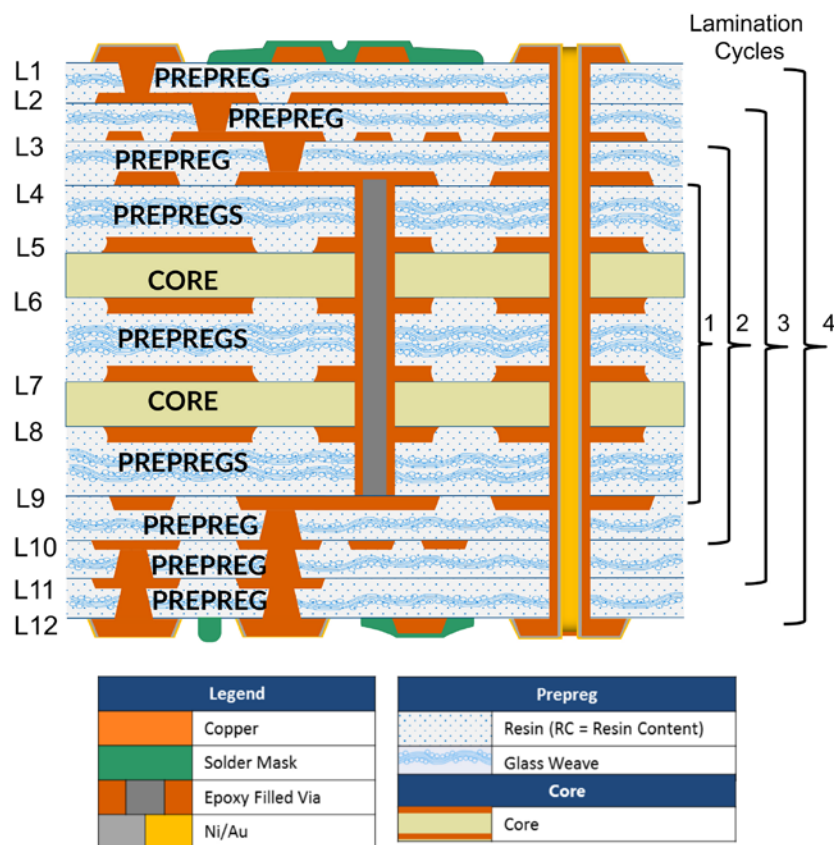


Figure 6: A four-lamination cycle HDI stackup.

Another common problem we see is on heavier copper stackups. In Figure 7 we can see the heavier copper gets taller, and we need to space out these signals, which are basically lines running in parallel to each other, in order to etch them. With thicker copper, we need wider lines and spaces. Often, when customers have problems with their designs, it's with an established design. They're trying to adapt it by increasing the copper thicknesses on the layers, and the lines and spaces were already at the maximum that they could be that fit in the circuitry, but then we can't etch them.

An issue that makes stackups so difficult is the predictability. When we put down these cores, and we melt the prepregs between them under high temperature and pressure, they might start out at a certain thickness, but how thick are they going to mush together after lamination? For heavier Cu stackups, we have to add plies of high resin content prepregs to ensure there's enough resin to flow into the etched spaces between the copper patterns on the core layers during lamination and have enough resin (but-

tercoat) between the glass and Cu to prevent failures and voiding (Figure 7).

Holden: It can be different for each fabricator, even though they're using the same materials, because of process variations.

Ellis: Exactly. In fact, it's one of the biggest complaints that Richard and I hear for transfer stack-ups. TTM has a trademark called Seamless Global Transfer, which is one of our core competencies that we advertise. We can match stackups between our sites as closely as possible, so that we know that we do have the long-term prototype-to-volume production migration path planned and approved before we even start the first prototypes.

But frustrated customers sometimes ask, "Well, you're TTM.

Why aren't all your stackups exactly the same?" We respond that they are not exactly

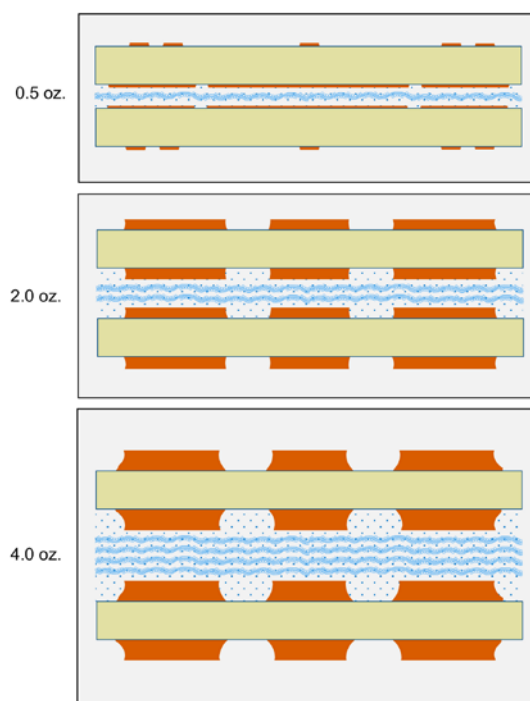


Figure 7: Copper thicknesses and plies of prepregs.

the same because even some of our major laminate manufacturers manufacture some of the material here for North America, and they manufacture material in China for Asia. The process equipment we use is going to affect that material a little bit differently, and have different tolerances. We have to optimize our simulators based on the output of the actual products from our fabrication sites.

I've dubbed the term "fabrication equivalent stackups." Some of my customers understand that we're providing two stackups, and even though they are slightly different, like the prepreg thicknesses here, for the three plies of prepreg it might be 9.2 in China, where it's 9.08 here (for San Jose), for example. Fabrication equivalent stackups are going to meet all the IPC and customer requirements. Even though there are minor variances, those variances are all within the fabrication and process tolerances, and they're all within the customer specification tolerances.

Holden: When you do that, you've just eliminated one respin, since making that mistake, between local low-volume quick-turn and high-volume Asia, will result in enough differences to require a further change.

Ellis: Richard, do you want to bring up the subject of best practices that you mentioned this morning, with regard to the prepregs?

Dang: Yes. One of the things we consider when we're making a stackup is that we want to keep the prepregs as similar as possible across the stackups. We have a process called lay-up before we go to a lamination, and the operator has to basically get all the materials in line and lay it up according to the stackup. If your design is using four or five different prepregs, once you take the prepreg out of their bag, you

can't tell what it is. You really can't tell a 1080 from a 106 sometimes, just by looking at it. We try not to do too many, like adding 106 and 1080 in the same prepreg opening. If we can do it in two plies (sheets) of 1080 (68% resin content), that's what we'll try to do, and we'll try to do it across the entire stackup. That helps us eliminate potential operator error, especially in mass production, when they're working on hundreds of panels.

Another best practice is to consider the glass weave used for different applications, such as low layer count, high-voltage, or high-speed applications. For 1.6 mm (.063") thick four-layer boards, we use thicker glass prepregs to achieve the dielectric thicknesses without using too many sheets, or plies, between layers of copper. However, when it comes to high voltage applications, years of testing has proven that thicker glass styles (i.e., 7628) don't hold up as well against conductive anodic filament

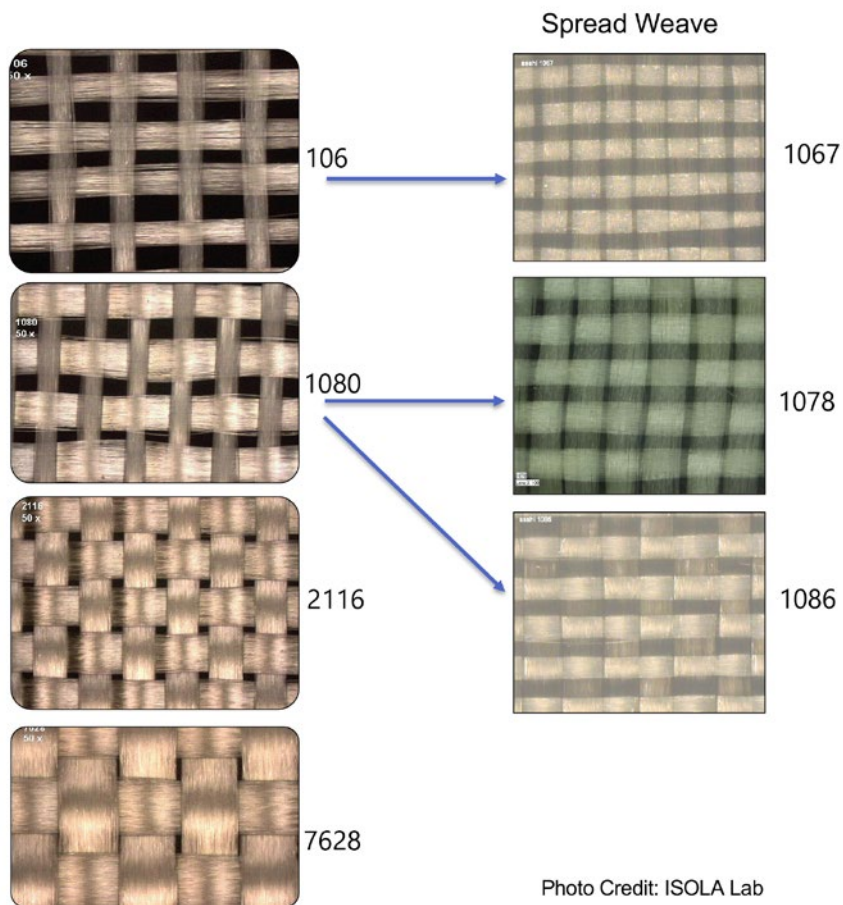


Photo Credit: ISOLA Lab

Figure 8: Typical glass weave constructions.

(CAF) failures as the finer glasses. So we often use 1080 and 2116.

The Dk of glass is higher than the Dk of the resin, and there are thick knuckles where the fiberglass thread bundles cross each other in the weave. High speed signals traveling across the weave see the Dk alternating between knuckles and resin between the threads, so the knuckles act as speed bumps. When applicable, we select spread weave glass prepregs to minimize this effect (Figure 8).

One of the things that happens is that, if we have two of these prepreg weaves stacked on top of each other, as the resin melts, these will start what we call nesting, where they slip over so the knuckles are adjacent to each other. They press in closer to each other, reducing the finished thickness. That's just one of the interesting features about predictability for the dielectric thicknesses; we have to pay attention to those things that the simulators take into account based on actual measurements.

Of course, it's not always possible, depending on how difficult a design is, but we do our best to try to maintain best practices to reduce manufacturing processes, which increases

yield for our customers, and they can get their boards in a shorter lead time (Figure 9).

Ellis: To Richard's point, customers will give us our competitors' stackups that were prototyped here in North America, and then we need to move them to Asia. We'll see things like three different prepregs in this one dielectric opening, because somebody in North America, for quick-turn prototypes, is just using whatever material they have on hand to meet customer requirements. But we try to plan just the next step better, so that we're planning using common materials that we know will also transfer to Asia without having to add additional part numbers to a stackup.

Dang: Because we do so many boards over in China, there are some classes of material that we actually have more laminates available and qualified for over there than we have here. Something that might be available in China may not be stocked by local distributors, so we often have to request alternate, equivalent materials to support quick-turn prototypes here in North America. We do a lot of pre-analysis on things like that before recommending a stackup.

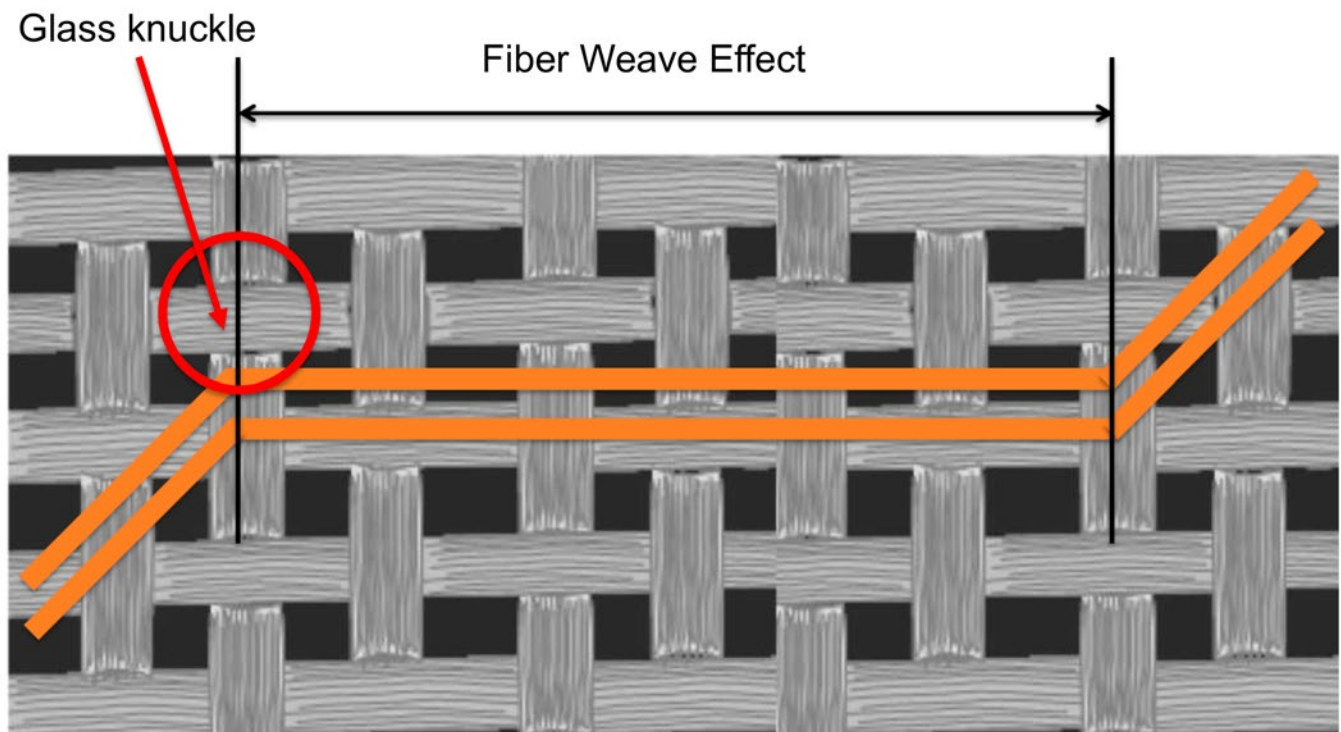


Figure 9: Glass "knuckle" shown in fiber weave effect close-up.

Holden: With a block or a table, what are the reference layers for the particular signal there, if they've chosen to make it a layer that's not adjacent, which is much of the time?

Ellis: Oh, that's a good point.

Holden: A lot of times, they do. They've got to tell us it's not the adjacent layer.

Dang: And whether the trace is coated or uncoated by solder mask.

Ellis: That's a really good one, Happy, because a lot of times, we just hear, "We want 50, 100 or 120 ohms on all layers," and once we get into fine dielectrics, 120 ohms is really hard to hit because the lines can be so small that they may be impossible to etch.

Holden: Nowadays, you have to tell people not just the solder mask, but are you going to put anything on top of solder mask, like thermal grease or conformal coating, because if you've got micro strips, the fields will go up into those materials. You can't assume that it's air.

Ellis: That's interesting. Our simulators only cover for coated microstrip, which would be solder mask. I don't think we have simulators that include conformal coat.

Dang: We don't.

Shaughnessy: Julie, how much of what you do involves making life easier for the assembly guys?

Ellis: Since I have an assembly background, I always include that, too, because another issue is the dimensions of the bare individual printed circuit board versus how it's going to convey down a surface mount assembly line. It usually needs a minimum 5 mm, or 0.2", of clearance with no components on both of the long sides of the part. No assembler is going to want to be hand loading 2" x 2" small parts or putting it into a fixture to run it down the

volume production assembly line. So with my customers, a lot of times if it's a smaller part, we try to plan the multiple-up array with rails that is optimized on our fabrication panel and delivered to the assembler.

The other thing with my regular customers is they also know the standard panel size is normally 18" x 24", and we need an average of 0.7" to 1" all the way around for our tooling. So just on average, we're looking at a 16" x 22" fabrication panel. Sometimes a really big power board will come in, but they've got a little bit of room to play with dimensions, so we will squeeze down to the last 0.01". We may adjust one side, shorten one side and adjust the other dimension, to achieve two-up, instead of only one, on a fabrication panel, where we've squeezed every inch that we can. For volume production, especially for big boards, material optimization is the lowest hanging fruit that can save the most money by planning ahead.

The best circuit board designers select components that aren't so small they drive advanced fabrication requirements, take into account design rules for both the fabricator and assembler, work with both on the array with rails to achieve best material utilization with the least amount of assembly loading time, and provide accessible test points for the final assembly.

Shaughnessy: Do you have any advice for a designer or engineer having issues with stackup?

Ellis: Find a trusted fabricator and work with them, initially, to develop the stackup with the design rules for any project that will set the circuit board design precedence for a complicated, high-reliability, or production volume level of product. If it's a really simple four-layer stackup that doesn't have any controlled impedances or special requirements like high aspect ratio, then engineers can pretty much use their own software to create it. But if there are any higher requirements, or controlled impedances, please work with your fabricator.

Richard and I plan for a reduction in line-width of approximately 0.3 mil for a controlled impedance line transferring from TTM North America and TTM Chinese sites. If we're starting with a 3.0-mil line and the line shrinks by 0.3-mils when it transfers, it can put the design out of the planned site's etching capability.

Also, educate yourself and pick your experts wisely. It's easy to fall for a bad expert and get steered down the wrong path if you don't know anything yourself.

Holden: The only thing sad about this conversation is that in 1980, we had exactly the same issues, and exactly the same problems and

feedback. What's discouraging is it's 40 years later and we're still addressing things that are fundamental.

Ellis: You're right, Happy, because one size doesn't fit all, and just look at how complicated technology has become in that time.

Shaughnessy: Thanks for sharing all of this with us, Julie.

Ellis: No problem. It's always great talking to you all.

Holden: Thank you, Julie. DESIGN007

LG Display Launches First 48-inch Bendable Cinematic Sound OLED Display

LG Display, a leading innovator of display technologies, has announced that it will showcase the first 48-inch Bendable Cinematic Sound OLED (CSO) optimized for gaming at CES 2021.

The 48-inch Bendable CSO display utilizes OLED's advantages as its paper-thin screen bends and unfolds with a curvature radius of up to 1,000R, meaning that it can be made to bend up to a radius of 1,000mm without affecting the function of the display. It can therefore be turned into a flat screen while watching TV and used as a curved screen while gaming. The curved display offers a uniform viewing distance from the middle of the screen to its edge, maximizing the visual immersion that is popular among gamers.

In addition, the company's CSO technology enables OLED displays to vibrate and make their own sound without the use of any speakers, offering a vivid sense of reality as if the on-screen characters were talking directly to the viewer. The 48-inch Bendable CSO display's ultra-slim film exciter, which is the part that vibrates the display, has been reduced to a thickness of just 0.6mm from 9mm and therefore allows viewers to enjoy

a thinner screen as well as highly impressive sound.

OLED technology has recently been gaining attention in the gaming TV market for its superiority, as each pixel emits its own light, offering an infinite contrast ratio. This creates another level of vivid picture quality, along with the seamless experience delivered by a response time of 0.1 milliseconds, a refresh rate of 120Hz per second, and a wide variable refresh rate range from 40Hz to 120Hz.

Moreover, for gamers who view screens for an extended period of time, LG Display's OLED displays are particularly suitable because they are known for their eye comfort.

(Source: LG Display)



Conquering **Layers of Challenges** in PCB Stackups

Tim's Takeaways

Feature Column by Tim Haag, FIRST PAGE SAGE

There is an expression, “You can’t have your cake and eat it too,” which is another way of saying that for those things in life that are either one way or the other, you can’t have both. That’s really a shame in my opinion. Oh, not about wanting something both ways. I think that we all know from past experiences that trying to accomplish something by going about it in what is obviously the wrong way never ends up the way we really want or expect it to. For instance: trying to get into shape without exercising; wanting to improve yourself without being willing to learn; or trying to fly a remote-control airplane without extending the antenna on the control box. (Even though it’s been many years, I’m still kind of bitter about that last one.)

I think it’s a shame, literally—not being able to have a cake and eat it too. Can you imagine? There are very few things on a plate that I like

better than a slice of good, rich, moist, multi-layer chocolate cake. Your mouth is starting to water now, too, isn’t it? Just imagine having all of that chocolate goodness in a cake like that right in front of you, and then not being able to eat it. That would be sheer torture, and I think that is one of the reasons why I’m not the biggest fan of cooking shows. I can’t stand to watch them create something incredibly delicious and not be able to grab a fork and plunge in. But as we all know, there is a price to be paid for over-indulgence, whether it is in multiple layers of chocolate cake, or even multiple layers in a circuit board.

When I first started laying out printed circuit boards many years ago, I was working for a computer systems manufacturer whose PCB designs were all multilayer boards. While there were a great many things that I learned there, it also fostered one bad habit: I became



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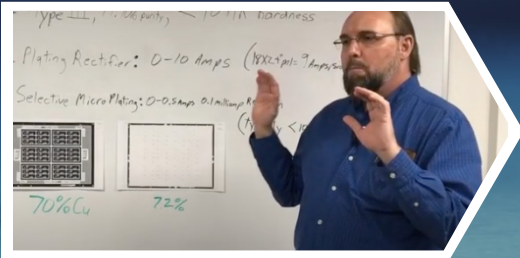
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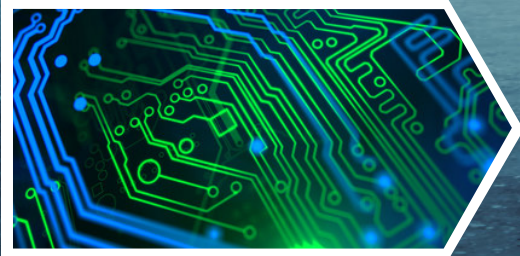
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accustomed to relying on being able to use multiple layers for routing instead of planning a more efficient layout.

“Can’t get this bus routed in? No problem; we’ll just throw in another couple of layers for you to work with.”

It probably wasn’t quite that easy, as memories like that tend to be a bit untrustworthy. It is true, though, that they were very generous with the amount of board layers that you had to work with, and critical board configuration decisions like layer stackups were created for me by others. This proved to be quite an inconvenience later in my career when my next employers didn’t give me the same flexibility in board layers that I was used to in order to work myself out of a jam. Instead, not only was I expected to work with what I had, but I was also supposed to reduce the layer count to improve on it whenever possible. This meant dealing with a whole new set of design rules and considerations related to board layer stackups that I had never had to work with before.

As we all know, it takes a herculean balancing act to create a circuit board that will deliver the maximum amount of performance for the least amount of manufacturing expense. Trying to sort out all the different pieces of the circuit board puzzle to achieve this balancing act can end up being a real brain teaser for new designers. Just for starters, you need to consider the following as you configure the board layer stackup that you will be working with:

- Signal integrity
- Power integrity
- Placability
- Routability
- Manufacturability
- Profitability

There are enough “itys” in that list to sink a ship, and we haven’t gotten to testability or designer confusability yet.

Thankfully, I worked with some great people who helped me to relearn some of the basics of PCB layout. They taught me how to work correctly with circuit board layer stackups, and why there was a whole lot more to multi-layer boards than just providing more room to

route on. It took some time, but after a while I came to a better understanding of the relationship between the different board materials and thicknesses, and how they should all be configured to design the board correctly.

I was very fortunate to have co-workers who helped me understand and refine the art of printed circuit board layout. I wonder, though, who will help today’s new designers work through problems like these. Company cultures are changing, experienced designers are retiring, and more is being expected of PCB layout personnel with less time to make it happen. How are today’s puppies going to learn some of these more advanced skills, such as how to correctly configure their board layer stackup? Here are some of my ideas on how this can happen:

- **Circuit board manufacturers:** I have talked to different manufacturers, and one of the more common themes I have heard is that they want to engage with their customers more before the board is designed. They typically have years and years of experience building circuit boards under their belts, and they understand the challenges that designers face better than most. They also are very aware of the capabilities and limitations of their own manufacturing processes, and the PCB materials being used. They want to help designers come up with the best layer stackup configurations possible because their customer’s success will ultimately translate to their own success. New designers can gain a wealth of information simply by working with their manufacturers.

- **Professional resources:** There is more technical training available out there than you probably realize. It not only covers PCB layer stackups, but many other aspects of PCB design. You can easily find a variety of seminars and classes from various organizations and groups within the design industry. There are design conferences that feature instructional sessions from some of the brightest minds in our industry, along with product demos and information on new design methods and technologies. In addition, you can also find a plethora of online

videos, white papers, and design-related publications that can help.

• **New technology:** One of the more exciting things happening in our industry is the creation of new tools intended to help PCB design and manufacturing work better together. One of those tools is the IPC-2581 data exchange format. Many manufacturers now can take your board information directly from your CAD system and create a layer configuration that will best fit its needs. Then, using the same data format, they send that layer configuration right back to your CAD system for inclusion in your design.

You: One of the best resources to pass along some of these advanced PCB design skills can often be found by looking in a mirror. Yes, I mean you. If you've been laying out circuit boards for any length of time, chances are good that you already have a lot of knowledge that can be extremely valuable to those who are laying out their first designs. Don't be afraid to reach out a helping hand to those who still have a lot to learn.

Along with the variety of online resources, I want to mention this edition of *Design007 Mag-*

azine you are currently reading. As you already know, this month's issue is focused on PCB layer stackups, and it is chock full of information and data from those who know what they are talking about. If you know someone looking for a little help with determining the most optimum PCB layer stackup for their design, be sure to point them this way.

The good news is that with all of the help available from manufacturers, professional resources, new technologies, co-workers and peers, you have the ability to create the perfect layer stackup for your PCB design. The more I think about it, the more I realize that I was wrong about my first statement. I guess that this is one way that you can have your cake and eat it too. Pardon me while I grab a fork.

In the meantime, keep on designing, everyone. **DESIGN007**



First Page Sage: Tim Haag writes technical, thought-leadership content for First Page Sage on his longtime career as a PCB designer and EDA technologist. To read past columns or contact Haag, [click here](#).

Engineering Technology Team's Printed Circuit Board Design Improves Electric Guitars

Traditional electric guitars have a "pickup," a magnetic transducer made with miles of copper wire coiled around magnets via a tedious, time-consuming process.

Purdue Polytechnic's Davin Huston, Mark French, and Kathryn Smith (a former graduate student) have created a flexible, printed circuit board that imitates the conventional copper wire configurations inside electric guitars.



With a conventional electric guitar pickup, string vibrations cause the electromagnetic field to oscillate, induce a voltage in the coil, and generate an electric signal. The team's circuit board works the same way.

Davin Huston, assistant professor of practice in engineering technology, said, "Our circuit boards can be printed in large quantities and fit inside just about any electric guitar, which simplifies the manufacturing process but keeps the sound quality and reliability."

"With typical pickups, the coils often produce undesired feedback and need to be potted with wax or a polymer," said French. "Our circuit board provides an alternative that is easier to produce with manufactured consistency."

(Purdue Polytechnic Institute)

DESIGNING FOR



The Magnitude of Stackup Considerations

Feature by Michael R Creeden, CID+, MIT INSULECTRO

When I was asked to write about stackup creation, I paused at the magnitude of this subject. It is similar to the framework used to pour concrete cement—you need to get the framework right because the framework has such a big impact on the final outcome. Such is the case with shaping the success or failure of our circuits. In writing the newest training manual due out early this year, I observed that the longest chapter in the textbook was dedicated to this subject.

Therefore, I believe it is truly one of the most important and far-reaching subjects in our industry. It was at the heart of my decision to accept an offer to work for Insulectro because it allows me to make a difference in our industry on this subject. Because it's such a vast topic, I can only scratch the surface in an article, but I hope to scratch it well.

I always like to remind readers to pursue all printed circuit engineering issues from three simultaneous perspectives when we design for X:

1. DFS–Solvability

Place and route dense critical circuitry to define optimal features and implementing constraints that meet three perspectives. Also, mastering an EDA CAD tool is a significant challenge compounded by accelerated development schedules.

2. DFP–Performance

Ensure that all SI, EMI, and thermal performance metrics are met. You can solve a complicated design, then build a perfect bare board, but if the signal energy does not go where it should, you can throw the board in the trash can.

3. DFM–Manufacturability

As our circuits become more advanced so do the challenges associated with building a bare board. With decreased feature sizes, the tolerance window becomes more precise. Therefore, the layout professional must be aware of the manufacturing capabilities and engage with their supply chain at the beginning of layout. The practice of selecting your supply chain once layout is complete is a flawed approach.



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DFS

The earliest challenges for a designer to solve a layout comes from the physical size of the board, the operational requirements, and its end-user environment. This can challenge X, Y and Z concerns for placement, routing, and then manufacturing. Will the parts fit, and will they be appropriate for assembly concerns? Will there be enough routing resources? Will there be enough signal layers with return planes? The other solvability challenge is derived from the smallest components, typically μ BGAs. This challenges the drilling of vias used to pin-escape the SMT lands and satisfy the HDI connection. It subsequently requires the use of advanced drilling of microvias and related fabrication concerns. The customer requirements for an IPC Class 1-3, requires the board be designed and fabricated to this specification. The creation of robust vias is perhaps one of the biggest fabrication challenges to ensure reliability.

DFP

Today's high-speed circuitry is not your father's high-speed. What were acceptable practices of interconnect are no longer allowed. How a signal is routed in the design and how it references everything it encounters is important due to its electro-magnetic (EM) field. It is one-half of a wave guide; the return path is the other with the EM energy field traveling through the dielectric material. Any piece of metal it encounters will affect or determine the actual impedance value. Any piece of metal can act as a return path but the question you should ask is, "Is it the best return path?" If

it's not GND, then my position is that it is not the best return path. You really have a choice to either fix a signal integrity problem or avoid creating one in the first place.

DFM

Understanding the fabrication process to some degree enables you to make intelligent, cost-effective decisions that can affect long term product yield and reliability. Understanding the yearly production quantity goals will focus your decision for cost vs. everything else. Knowing the production fabricator's capability matrix is key to building a high-yield, low-cost reliable product. When you are told about their capabilities, don't design to the minimum features; only use those when it is absolutely required, rather make every feature more robust as the norm. This makes for a build that has high producibility. (See IPC-2221 Producibility Levels).

I work for materials distributor Insulectro, representing Isola and DuPont laminates, so I'd be remiss if I did not emphasize the extreme value that laminates play regarding every perspective listed above: DFS, DFP and DFM. Material selection helps routing solvability allowing HDI with thin laminates and helps SI issues with technically appropriate laminates for signal energy flow. Lastly, it facilitates fabrication process constraints when proactively engineered.

Laminates are comprised of three basic elements: resin, glass weave, and copper. The resin is for bonding, the glass weave is for rigidity, and the copper is for conductivity. Each element plays a vital role in establish-

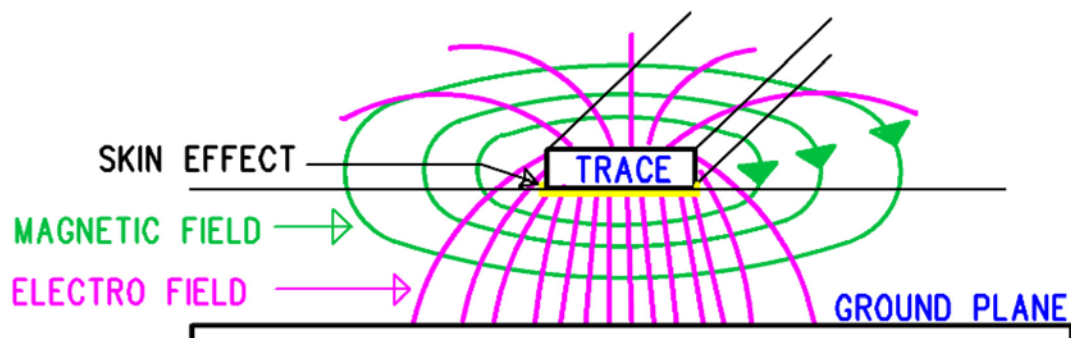


Figure 1: Energy fields travel through the dielectric material.

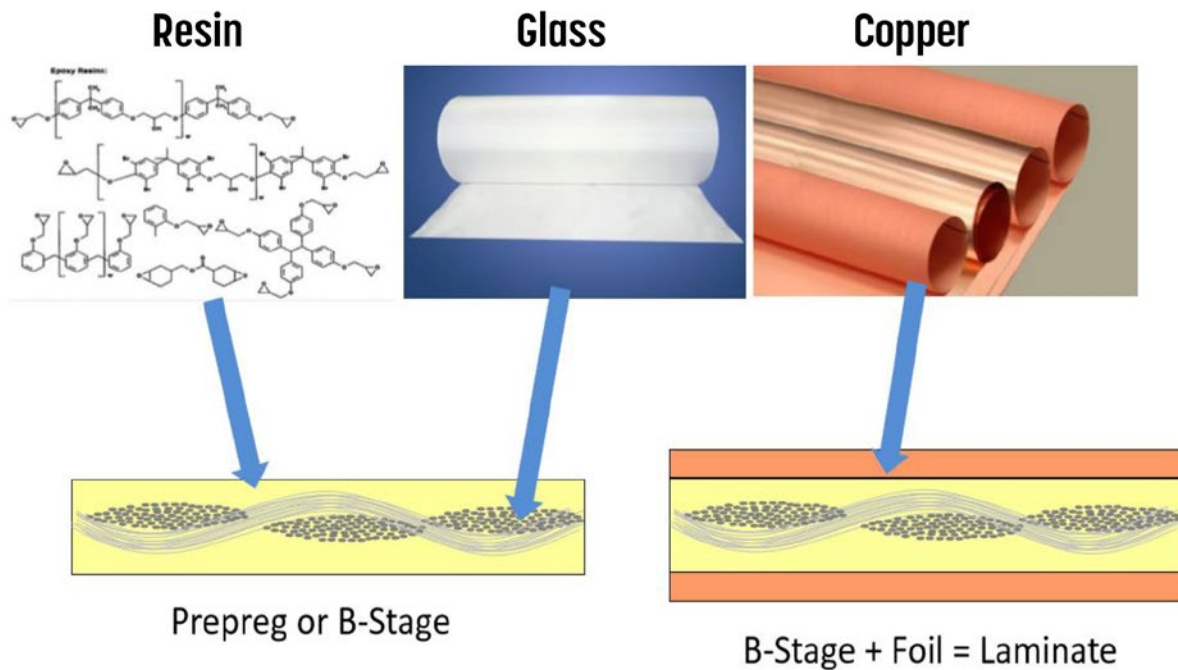


Figure 2: The three elements comprising rigid laminates.

Epoxy Materials Construction

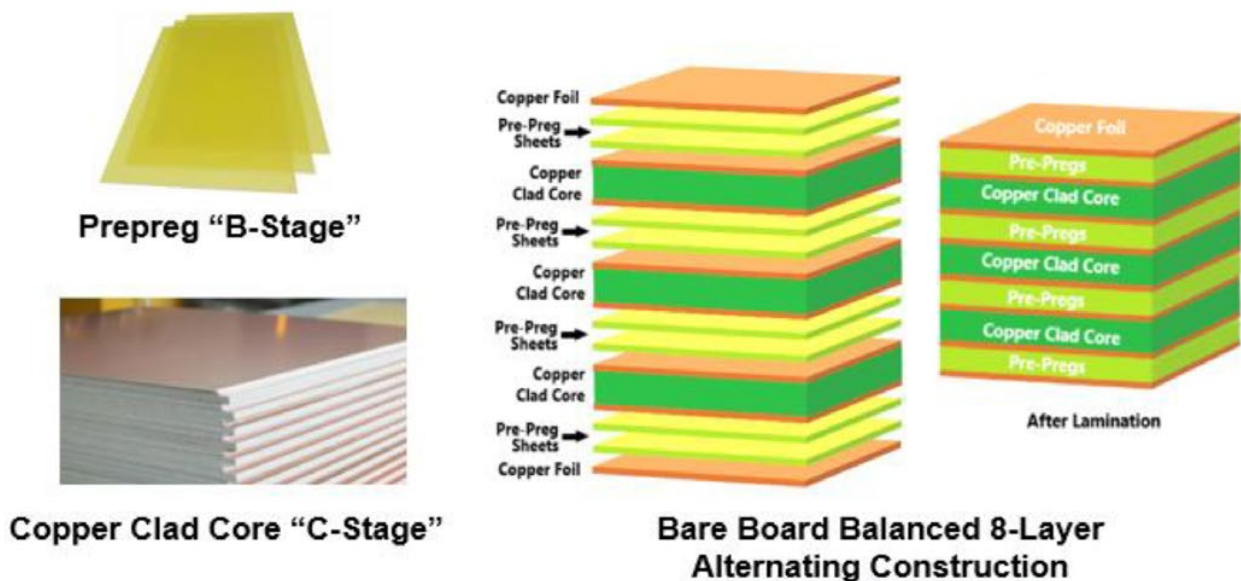


Figure 3: Rigid laminate types and a balanced construction method.

ing physical, electrical, and fabrication parameters.

The laminates for rigid boards come in two basic forms (copper-clad and prepreg) and are built in an alternating fashion from the center of the stackup outward. The prepreg acts as a

joining agent between two cores or a core and external copper foil layer.

Laminates have physical and electrical parameters which affect performance and the manufacturing process. These laminates and copper foils are supplied in many thicknesses

and are used in a multitude of combinations; your fabricator can help you find the best laminate solution for your needs. Chart 1 and Chart 2 show a variety of performance specifications for Isola and DuPont laminates.

Physical (thermal) parameters:

- (Tg)—Glass transition is the transition temperature at the lower end of the thermal excursion, whereby the resin changes from a semi-solid state to a rubbery state. This is very important for high layer-count boards.
- (Td)—Decomposition temperature is at the higher end of the thermal excursion, whereby the material may start to decompose or breakdown from excess heat. This is very important for boards that may


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ISOLA Product	Replaces These products	ISOLA products compatible for Hybrid Builds	Gbps	IPC Slash Sheets,UL, Comments and Recommended Bit Rate/Flame Rating & Frequency range	Max Operating Temp	Tg By TMA	Td	Dk	Df	VLP 2 Foil
370HR	Pan R-1755V and R-1655V	185HR, 408HR, I-Speed, I-Tera, Tachyon 100G, Astra	2 to 3 max	IPC-4101 /101 /98 /99 /126 UL E41625 Legacy High rel and lead free comp. FR4V-0 94	130 °C	180	340	4.04	0.0210	N/A
FR408HR	Nelco N4000-13 and 13EP	185HR, 370HR, I-Speed, I-Tera , Tachyon 100G, Astra	up to 12	IPC-4101 /98 /99 /101 /126 UL -E41625 Multifunctional low loss resin V-0 94	130 °C	190	360	3.68	0.0092	Available
I-Speed®	Pan Meg 4 R-5725 R-5620 EM-888, K	185HR, 370HR, 408HR, I-Tera, Tach 100G, Astra	Up to 20	IPC-4101 /98 /99 /101 /126 UL-E41625 Best Signal performance at this cost. V-0 94	130 °C	180	360	3.64	0.0060	Standard
I-Tera® MT40	Pan R-5775K, R-5670K Meg 6,G,N	185HR, 370HR, 408HR, I-Speed, Tach 100G, Astra	Up to 60	IPC-4103 /17 UL-E41625 Very good signal and thermal performance V-0 94	130 °C	200	360	3.45	0.0031	Available
TerraGreen®	EM-528	IS550H	Up to 77	IPC-4103 /17 UL-E41625 Halogen Free version of I-Tera MT40 V-0 94	130 °C	200	390	3.44	0.0039	Available
P95/P25	Arlon 85N, Nelco 7000-1	P96/ P26 *370HR when cured @ 375°F	up to 5	IPC-4101 /40/41 UL-E41625 HB-94 No Flow version of Prepreg available	140 °C	260	416	3.76	0.0170	N/A
Tachyon® 100G	Pan Meg 7, N R-5785, R-5680	185HR, 370HR, 408HR, I-Speed, I-Tera , Astra	Up to 125	IPC-4103 /17 UL-E41625 Ultra low loss and low Dk for HSD app. V-0 94	130 °C	200	360	3.02	0.0021	Standard
Astra® MT77	Rogers RO-3003 clad and bondply	185HR, 370HR, 408HR, I-Speed, I-Tera, Tach. 100G	Up to 125	IPC-4103 /17 UL-E41625 Ultra Low loss, Low Dk alt. RF V-0 94	130 °C	200	360	3	0.0017	Standard

Chart 1: Isola rigid laminate specs.

Property	Unit	Method	Kapton® HN	Pyralux® AP	Pyralux® AG	Pyralux® HT Bondfilm	Pyralux® TK
Thicknesses	mil	—	1 - 5	1 - 6	1 - 2	1-4	2 – 4
Dk @ 10 GHz	—	Method 2.5.5.5	3.4	3.2	3.2	3.0	2.5
Df @ 10 GHz	—	Method 2.5.5.5	0.010	0.002 - 0.003	0.007	0.003	0.002
% Moisture uptake	%	Method 2.6.2	2.8	0.8	0.8	0.8	0.6
CTE (x-y axis)	ppm/°C	50 to 250 °C	20	25	17-20	25	27
CTE (z axis)	ppm/°C	50 to 250 °C	115	90	90	90	102
Peel strength	N/mm	IPC-TM650	N/A	2.0 (ED) 1.6 (RA)	2.0 (ED) 1.6 (RA)	N/A	1.2 (RA)
Tg	°C	DMA	360 - 410	220	230	220	270
Tm	°C	DSC	—	—	—	—	300
Flammability	—	UL94	V-0	V-0	V-0	V-0	V-0

Chart 2: DuPont flexible polyimide specs.

experience multiple lamination cycles, such as HDI boards.

- (CTE)—Coefficient of thermal expansion occurs in both the X/Y-axis and the Z-axis. The glass weave moves in the X/Y-axis. This is of concern for warpage threatening solder joints. Boards are thin in the Z-axis as compared to the X/Y-axis; therefore, Z-axis can be of greater concern as it threatens the reliability of plated holes.

Electrical parameters:

- (ϵ_r or Dk)—Dielectric constant, also called permittivity or relative permittivity, is the ratio of capacitance of electrodes with a specific material. This is critical for impedance calculations and is of high value to high-speed digital circuits. It should be noted that the approximate Dk of resin is 3.0 and glass weave is about 5.0 with a resultant Dk of about 4.0.
- (Df)—Dielectric loss is the absorption of electromagnetic energy by the board material in a varying electric field. This is critical for minimizing dB loss calculations and is of high value to RF circuits.

Copper comes in several forms such as foil layers, electro-deposited or electroplated. Copper foil is typically utilized on the outer two layers and it has a smooth side and a rough side. The rough side provides adhesion to the resin in the prepreg and the smooth side is better suited as an energy transfer surface reducing energy loss.

There are many great laminate manufacturers in our industry. Yes, I think ours are the best and I'm always eager to make that case. But as designers, you need to pick the best material for your needs, always working early with your supply chain. What I want you to remember is to get the best use from the best material by understanding all three perspectives (DFS, DFP and DFM) and not just pursuing one or two perspectives. **DESIGN007**



Michael R. Creeden, CID+, MIT, is technical director of design education at Insulectro.

New Laser and Imaging Optics for High Powers and Harsh Environments

Edmund Optics, a renowned provider of optical components, continuously expands its product offering to reflect market developments and customer needs. New products are added each month to better serve the industry. EO just released Laser Grade C-Axis Sapphire Windows, which are ideal for use with high-powered lasers and TECHSPEC Cw Series Fixed Focal Length Lenses, which are designed for exposure to water, moisture, and humidity.

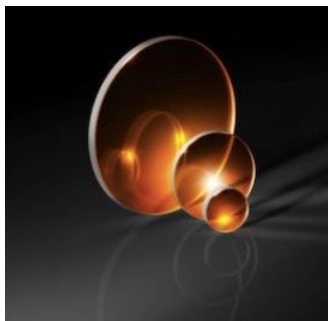
Laser Grade C-Axis Sapphire Windows are precision optical windows cut to the C-axis of sapphire eliminating inherent birefringence. C-axis sapphire provides high transmission from the UV to the mid-IR, excellent chemical resistance, and high surface hardness. These laser

windows feature 10-5 surface quality, $\lambda/10$ transmitted wavefront distortion, and are available uncoated or with an ion-beam sputtered (IBS) antireflection (AR) coating for 1000-1100nm Nd:YAG, Yb:doped fiber, or Yb:YAG laser applications.

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[Source: PRNewswire]





HELPFUL TIPS

Seven Tips for Your Next Stackup Design

Feature by Eric Bogatin
UNIVERSITY OF COLORADO, BOULDER

If interconnects were transparent, the stackup in your board would just be about how many layers you would need to route all the connections between components. In fact, some test boards that are strictly testing continuity and isolation do exactly this. Each layer is a dense packing of narrow signal traces connecting an array of pogo pin pads on the top side to an array of connectors to an ATE on the bottom side.

But rarely do we have the luxury of designing a board just for connectivity. When interconnects are not transparent, we must engineer them to reduce the noise they can generate. This is where design for signal integrity, power integrity and EMC—collectively high-speed digital engineering—are so important.

Seven Tips for Stackup

1. An important element in reducing the noise contributions from the interconnects comes from the stackup of the board and the layer assignments. The very first step is to engi-

neer all signal layers with at least one adjacent plane as the return path. This will reduce the crosstalk between the signal-return paths: the microstrip traces on the outer layers and stripline traces on the inner layers.

2. The striplines can be either one signal layer between two planes or two signal layers between two planes. With two signal layers between two planes, there is the danger of excessive crosstalk if signals on adjacent layers are routed broadside to each other.

3. To avoid this problem, it is best to route the adjacent signal layers in dual stripline stackups orthogonally. One signal layer is routed in the x-direction, the other in the y-direction.

4. When interconnects must distribute 10 A of current or less, traces as wide as 200 mils can carry the 10 A of current in 1 oz copper with an acceptable temperature rise. But, with larger currents, like 20 A or more, it may be necessary to use wide planes to distribute the current from the power generators to the power consumers on a board. This is when some of



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the planes should be allocated as dedicated power planes.

The challenge is balancing the requirements of power distribution with the requirements for reduced crosstalk from signals changing return planes.

In principle, a signal line will see exactly the same characteristic impedance if the return plane is at ground potential or 12 V potential or anywhere in between. The problem with using a different voltage plane than ground to carry return current is when the signals change layers.

The challenge is balancing the requirements of power distribution with the requirements for reduced crosstalk from signals changing return planes.

5. When a signal trace switches layers, we use a via to carry the signal current. If the return plane also changes, we will achieve the lowest crosstalk between all the signals switching layers when we also provide a via to carry the return current from the starting plane(s) to the final plane(s). This is a low-impedance via shorting between the two different return planes. This is only possible if the return planes are the same voltage. If they are at different voltages, we can't add a shorting via between them. This is a strong motivation to only use ground planes as the return planes for signals.

6. At best, if the two planes are a different voltage, we can add shorting vias between the two planes with a DC blocking capacitor between them. The loop inductance through a DC blocking capacitor can be as much as 5x higher impedance of a direct shorting via. It is a poor approximation to a shorting via, but the best we can do.

7. When signals change return planes and the planes are at different voltages, we run the risk of launching high bandwidth return currents into the cavity formed by the two planes. This is a source of long-range crosstalk and potentially a source of radiated emissions noise. One solution to reduce the noise in the power-ground cavity is by using very thin dielectric in these layers. This suggests that when power planes are used, they should be paired with closely spaced adjacent ground planes.

Once the order of the signal layers and planes is set, the dimensions can be calculated based on the line width of signal traces, the dielectric constant of the laminates used, and the target single-ended or differential impedance. This is where a 2D field solver comes in handy to define the cross section of microstrip traces, single layer stripline and dual layer strip line traces.

If you don't follow these tips, it does not mean your board will not work. Unfortunately, there is no way of knowing if your stackup design will work or not unless you do a detailed analysis based on the driver models and 3D electromagnetic analysis of all the worst-case signal and power paths. Implementing these tips is about risk reduction.

They are part of a balanced diet of best stackup design practices, best signal routing design practices, and best power distribution design practices. And like all design guidelines, buyer beware. Always consider the best design practices, but also always do your own analysis. **DESIGN007**



Dr. Eric Bogatin is currently the dean of the Teledyne LeCroy Signal Integrity Academy and an adjunct professor at the University of Colorado, Boulder in the ECEE department.

Eric has written a number of books on high-speed digital engineering, including *Signal and Power Integrity—Simplified*, *Bogatin's Practical Guide to Transmission Line Design and Characterization for Signal Integrity Applications*, and *Principles of PDN Design—Simplified* co-written with Micron's Larry Smith. To contact Eric Bogatin, [click here](#).

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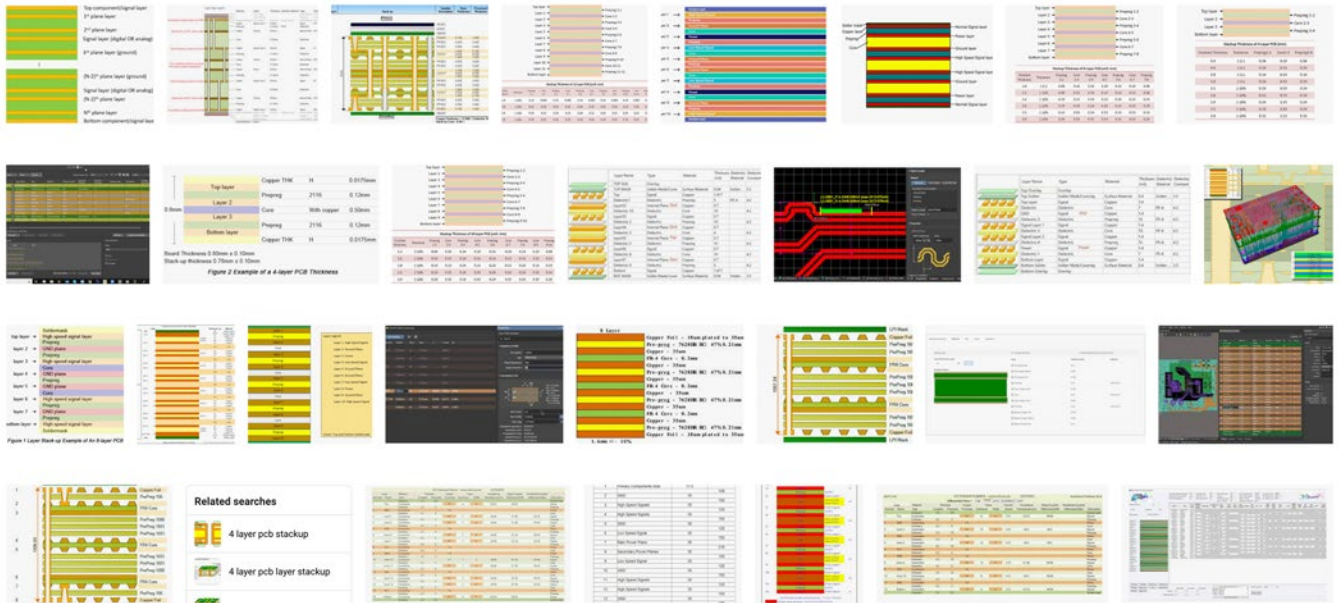
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Layer Stackup, Short and Sweet

Feature by Cherie Litson, CID+, MIT
LITSON1 CONSULTING

There are so many ways to do a layer stackup for your PCB, and lots of great articles on how to structure them. You can do an online search and I'm sure you'll find something that will work just right for your design.

Not a bad start, but pretty soon it gets confusing. There are so many options! And how do you know how many layers you're going to need anyway? Let's see if we can simplify the number of layers concept a little bit so that you can fine tune your search. How many layers do you need to start with?

First, what restrictions and features do you have?

Part area: The number, size, and type of your parts will play a large role in influencing the number of layers you will need. You will need the complete part area. The part area must include the "courtyard" area around the part. If you have a database for your parts, it's a good idea to incorporate this number in the attributes so you can get a quick total from the BOM. (Otherwise, it's a bit time-consuming to find this.)

If you have any components with a pin spacing of 0.5 mm (.020") or less, you're into HDI land. Depending on how many pins are on these small parts and the breakout pattern you'll need, you'll be using blind and buried vias which require at least a four-layer board and probably more. There are some new techniques and fabrication processes that are com-

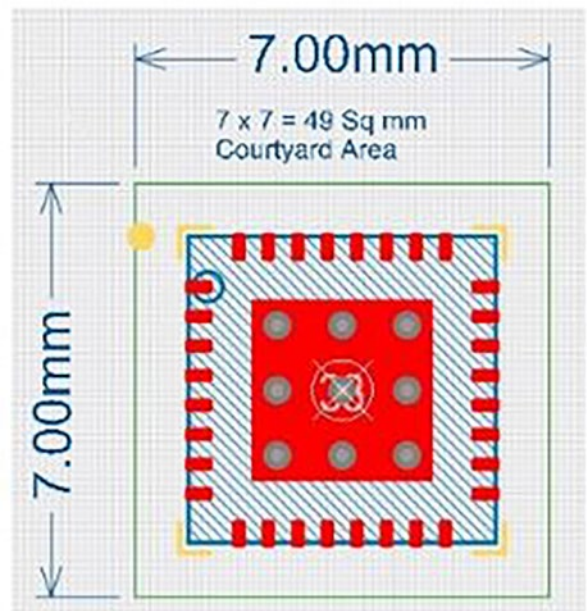


Figure 1: Don't forget to include the courtyard area around your part.

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ing soon to help offset issues with these small parts. (Very exciting stuff! More on this later.)

Number of pins: After you have the number of components, you'll need to know how many total pins you need to connect. This, too, can be put into the component attributes and extracted easily from a database.

Signal vs. power pins: You can subtract the number of power pins from the total pins to get the signal pins. When calculating the number of layers below, you'll just use the signal pins.

Return planes: Don't forget the return planes. All signals must have a return somewhere; the best practice is to place your return directly under the signal.

Board space: This is the size and shape of your board. Take out any keep-outs, edge relief, and areas around mounting holes. Include both surface areas. Avoid having any small "peninsulas" on the board edges if you can. These should not be counted as usable space.

If the board is too large or too small you can have placement issues. Too large and you'll probably waste a lot of space. Too small and the boards become difficult to route and place parts. Anything under 1.5" in any direction will require some attention. Also, odd board shapes can increase layer count due to limited

routing space. The size and shape of the board can influence the type of layer structure that will work easiest.

Trace and space: This is key. Your routing takes up room. Getting those connections made in the fewest number of layers really depends on your trace width and space width. You'll need to use an average of the largest and smallest trace sizes and the spaces between them that you're going to use. Or better yet, utilize a root mean square (RMS) of the different sizes you'll use. (Don't forget the spaces.)

Via area: How this affects your layers is going to depend on HDI. If you need to have blind and buried vias, you must add those separately depending on what you choose to use. (Just blind or blind and buried.) If you use through vias, then you will need to add them into the space used on all layers. Use the diameter of the [via pad] x [number of pins]. This may be a bit more than what you will need, but it will help allow for the area for test points.

Cost: This can limit the number and style of layers you can use. If cost is an issue, you've got to be creative and find ways to reduce your layer and via structures. Just a hint: HDI designs will usually not be in the cheap \$10-\$50 per board category unless you're ordering them in the 10K+ ranges.

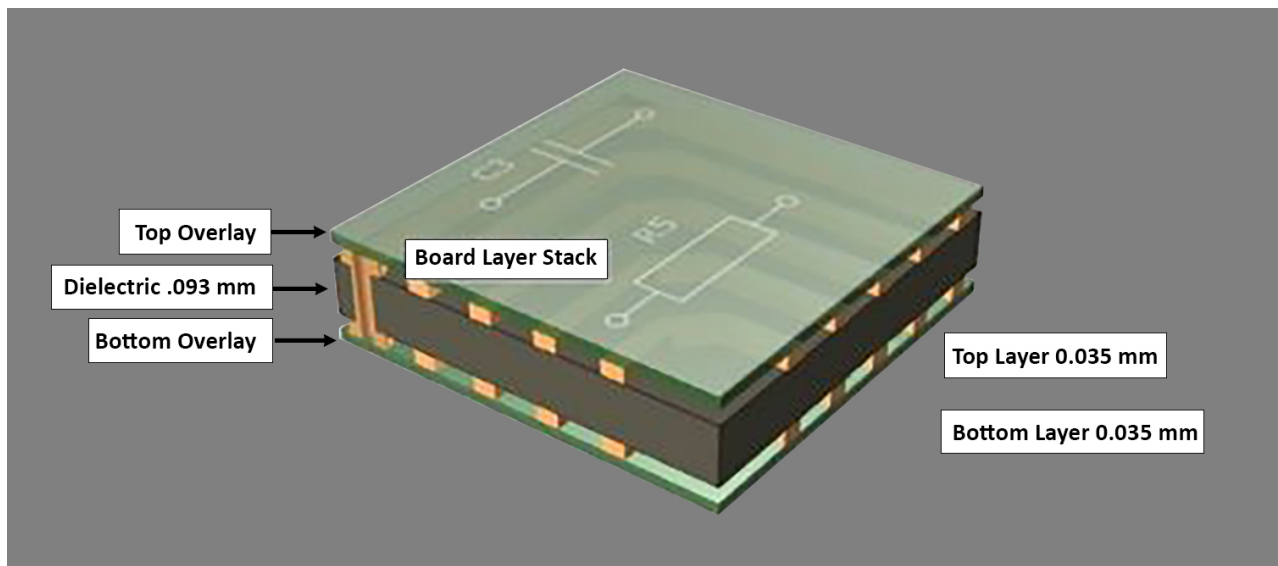


Figure 2: Example of a stackup for a simple PCB.

A Formula for Estimating Layer Count

Okay, now that we have a few guidelines to go by, we can start coming up with some numbers. Now, you're probably thinking "Holy crap, that's a lot of work!" Yep, it can be, but each item is not that difficult by itself. And this gets you in a reliable ballpark for the number of layers that you'll need.

I have not found anyone else willing to quantify and share a good formula for calculating the number of signal layers needed for a design (Table 1). I did have such a formula once, but I lost it when a virus invaded my computer. So, let's create one with the information we have. Then, if you come up with more ways or things to add to this one, we can keep sharing so we don't lose it again.

Number of signal layers	Ls
Part Area	PA
Signal pins	SP
Board space (usable)	BS
Trace and space RMS	TSR
Ratio	R
Through via area	tVA
Blind and/or buried via area	bVa

Table 1: Information needed to create a formula for calculating the number of signal layers needed for a design.

Ratio of Part Area/Bd Space: $R = PA/BS$

The "usable" board space available is important. This gives you your first estimate of layer count needed.

Some layout packages offer this ratio in the program after you import the footprints. If the ratio starts to get around 0.9:1, you're going to need some special via structures to get everything connected. As the ratio gets closer to 1:1, more layers become necessary to route the board. If you're going over 1:1, you'll need more surface area or lose some parts.

If your ratio is equal to or less than 0.5, you will probably need only 1-2 layers to complete the routing. If all your routing and returns are

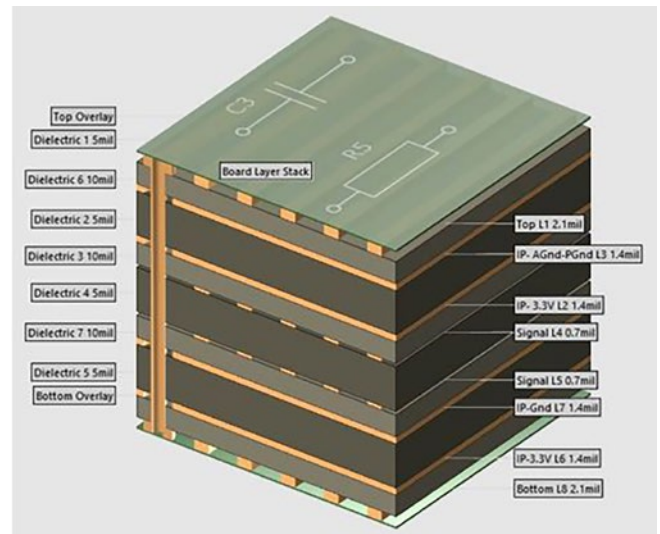


Figure 3: Planning the stackup of a multilayer PCB involves many design trade-offs.

on just the two layers, you'll need about as much space as the components consume to route it and not get too much noise.

When the ratio is over 0.5, then we need to add more factors into our layer count estimation.

$$Ls = \frac{(SP \times TSR) + tVa}{1/2 (BS)}$$

Then add in 2R + Power Planes needed + 2bVa

(The 2R is for component placement area on the top and bottom layers.)

There are more factors you may have to consider depending on how complex your designs get. This should get you in the ballpark. Plus, there are some additive processes that are coming out (Averatek's A-SAP™ process, for one) that will help to reduce the TSR and help to cut down on the number of layers needed.

Then search for and read anything written by instructors like Rick Hartley, Lee Ritchey and Eric Bogatin for tips on how to structure these layers.

Let me know if this works for you as well as it has for me. **DESIGN007**



Cherie Litson, CID+, is an IPC Master Instructor for EPTAC, and founder of Litson Consulting.



OWN IT!

OEMs Must Own the Stackup

Feature Interview by the I-Connect007 Editorial Team

Who owns the stackup design process? Is it the OEM's design team, which is familiar with all the electrical requirements of the PCB, or the fabricator, who knows far more about the manufacturing process?

We recently asked Bill Hargin, CEO of the stackup optimization software tool company Z-zero, to share his thoughts on stackup design. Bill built Z-zero around the need for software tools that can help designers facing stackup challenges. As Bill sees it, OEMs need to start exerting ownership of the stackup—and stop asking their fabricators to be responsible for stackup design.

Andy Shaughnessy: I'm here with my colleague Happy Holden, and Bill Hargin, the CEO and founder of Z-zero. How are you doing, Bill?

Bill Hargin: I gave myself the title Director of Everything.

Shaughnessy: And you had some fairly big news recently: Z-zero is collaborating with

Siemens EDA to help optimize the creation of better stackups, which is the topic of today's conversation.

In our surveys, designers talk about how tough it is getting stackup right and all the trade-offs they have to make. What are your thoughts on why it's so hard to get stackup right?

Hargin: I think the answer to that is simpler than what people might think, but it's very detailed. But what engineers and designers have been doing for the last 25+ years is throwing their requirements over the fence to their fabs and trusting the fabs, who over time have acquired impedance calculation and simulation tools. We know most of the tools that are out there.

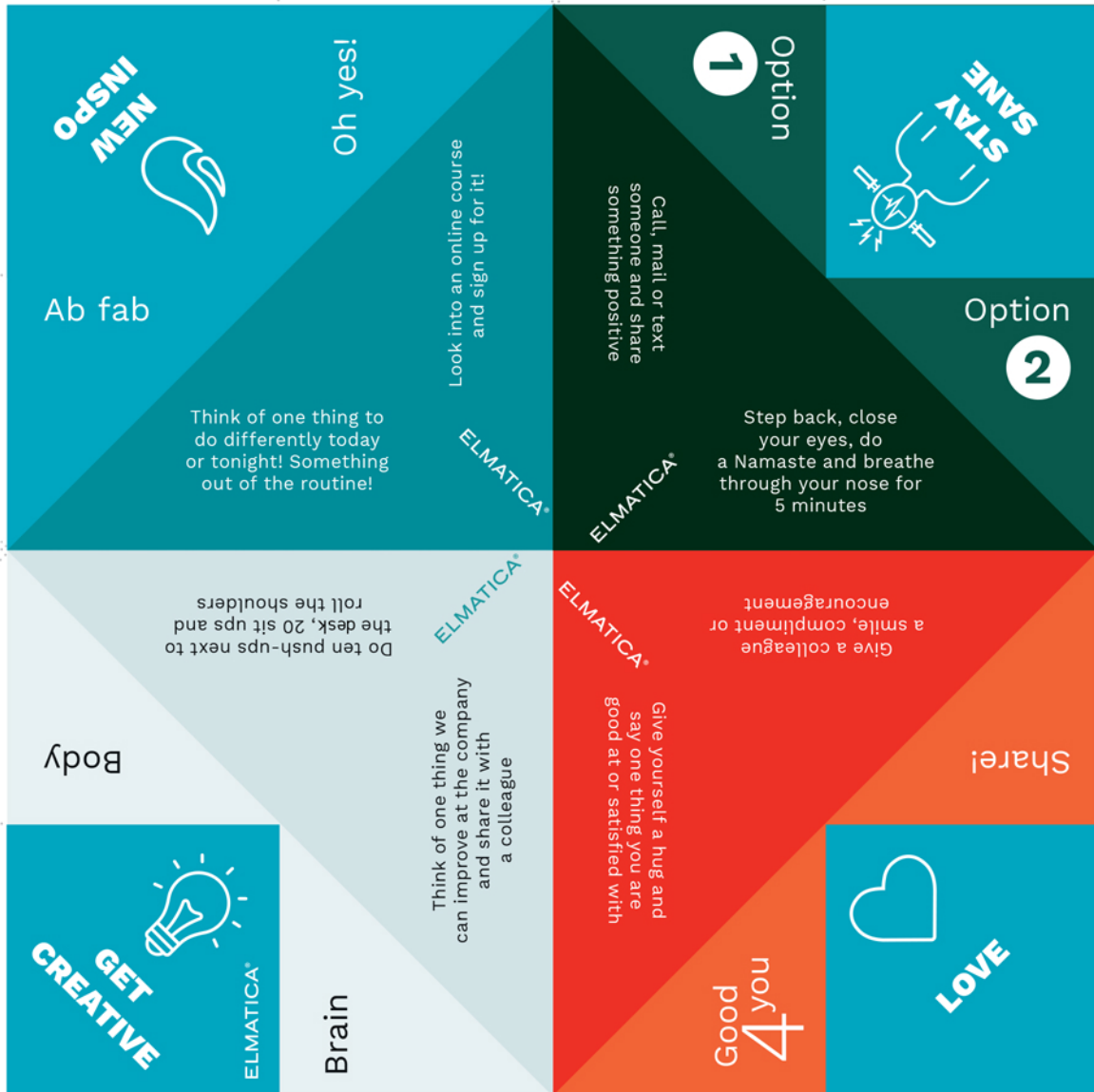
But that part of the PCB design process has been delegated to the fabricators for the last 25+ years. And my view is that designers and engineers need to take more control of what's happening in the stackup design process and own more of it. Bring it in-house.

Siemens EDA calls it a shift-left strategy, and the concept is to take things that are known in the fabrication world and bring them to the left in the design process so that you're making

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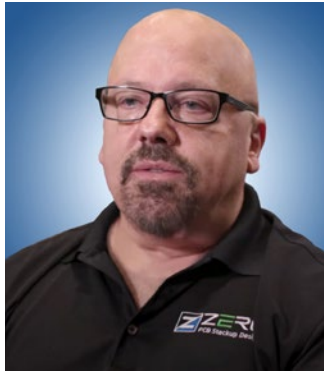
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decisions that are going to affect the manufactured PCB earlier in the design process. And you're bringing fabrication knowledge back to the OEM engineers and designers.

Shaughnessy: So it's a matter of designers needing to know more about the fabrication process.



Bill Hargin

Hargin: Right. For instance, I went to a doctor this week, and this is a perfect analogy. I go to this particular specialist every six months or so, and he doesn't remember what we've discussed in the past.

He just had a patient leave his office. He got my file folder out, and I can see him thinking right in front of me, looking through my folder. I whip out my laptop and flip it open, and I've got graphs and Excel tables. I've mapped out my history of medications and the resulting symptoms in Excel, and I'm showing it to him. I have better data than he does.

I used to hear that engineers are the toughest consumers in the world to sell to, because they analyze everything. Well, engineers need to do that with stackups and materials. Don't just kick the can down the road and think your fabricators are going to do everything perfectly.

And I've had engineers say to me, "Why do I give the same set of requirements to three different fabricators, and I even specify the materials, and I get three different stackups back?" In response, I've told them that they need to take more control of the process and leave less margin for the individual fabricators to figure things out separately.

Shaughnessy: In their defense, wouldn't the fabricators say that three different fabricators are naturally going to be optimizing for different processes, chemistry, and sweet spots?

Hargin: I think that's a myth, and I don't fault you for saying that at all, Andy. I think that's a common perception. But I think it's a mythological perception that a guy in Shanghai manufacturing a board has a different process than

one in Guangdong. I know there are differences in chemistry and how they do things, but in the end, you are specifying a board with impedance targets and tolerances, thickness targets and tolerances, and they all need to meet those specs. What I'm talking about is at the field solver level: they're coming back with different results from different tools.

Why is that? I think it comes down to operator differences. When you get a stackup back from PCB fabricator A and PCB fabricator B, it's two different people probably running two different field solver tools. So right there you've added two degrees of freedom to the stackup design process.

And different fabricators will send stackups back to you in different formats, too. One will send you a PDF, the other will send you an Excel spreadsheet, and if you have a third fabricator, they're going to send you a JPEG. The cattle have gotten out of the barn, as it relates to stackups. Who owns the fact that the cattle are out of the barn? It's the OEM design team; it's their hardware, and it's their jobs on the line.

So if your cattle are out of the barn, what do you need to do if you're a farmer? I come from farming people way back when in the Midwest. And the first thing you need is a barn. You can't get them back in the barn if you don't have a barn, and to me, the barn is the stackup software.

The second thing you need is a fenced area, which is a process to get those roaming cattle back inside the fenced area leading to your barn.

Shaughnessy: That's interesting. So, a lot of this confusion could be eliminated if OEMs took ownership of the stackup design process.

Hargin: Yes. Don't rely on your fabricators to do all that. They don't talk to each other; you're the only one talking to each one of them as the OEM design team. They don't collaborate; they compete with each other. And so, you've got to own the entire process.

I get in these discussions every week, often every day: Which Dk numbers can we trust? One fabricator says it's this, and another fabricator says it's that, and the laminate vendor says it's another thing. Which values can design teams trust?

I'd like to hear Happy's opinion on this. But the common mythology is that those differences are due to individual fabricator processes, and that's not true. It's fundamentally illogical.

Happy Holden: It's interesting that you talk about field solvers. In your expertise, is it the different way that people have put their field solvers together, or is it the independent variables like thickness and Dk that would result in fabricators coming back with a different stackup? Not so much whose field solver it is but that each one of them has their own numbers for thickness and Dk that may or may not be close to what it really is.

Hargin: Look at it in terms of degrees of freedom, which is usually used in modeling motion. You can have two degrees of freedom; you can have three degrees of freedom. Here we have at least four, if not five, degrees of freedom. We use HyperLynx field solver, but others may use different field solvers. There's one set of Maxwell's equations, but field solver A and field solver B might use slightly different meshing techniques. Now, do the field solvers usually agree? Yes, they do. But let's say that the field solver is one degree of freedom.

The second one is this: What parameters are being fed to the field solver? Are they the same, or are they slightly different? The third is the operator as a degree of freedom: Person A versus Person B at two different fabricators. They're not sitting side by side, comparing their work. That doesn't happen until the stackup gets back to the OEM. So, that's a third degree of freedom.

They could be using different Dks and many times they are—a fourth degree of freedom. Then the fifth degree: They could be using different percent copper values, and therefore different prepreg thicknesses. So you can get all

that variation. That's five degrees of freedom that we've identified that can lead to divergent stackup results, right?

Let's talk about Dk. This week, I was asked, "Which Dk do we use? Do we use the laminate vendor's Dk? My fabricators use slightly different Dk values." Some fabricators will send a stackup back to you and they won't even tell you the Dk they used.

They'll just tell you trace widths and dielectric height. And sometimes they'll include their calculated impedance values. Sometimes, if you give them a 50-ohm or 100-ohm target, they'll just say, "Oh, yeah, it's 100 ohms." As if everything was exactly 100 ohms right on the button. And they won't give you the Dk numbers. So you get all of this variation, and that's why I say you need to fence those cattle in. I feel bad because I'm referring to people as cattle, but it's just a metaphor.

Shaughnessy: Designers have been called much worse.

Hargin: You need to have a process by which you rein this whole thing in. If you take a big fabricator like TTM that's worldwide, they'll use different Dk numbers at different sites. I believe what people do is they take their test coupons from boards, and they backward-engineer the Dk from using the IPC impedance equations. Is that special sauce? No, I don't think that's the special sauce; I think it's some guy using Excel. Is that due to their special processing? No, I think it's a guy sitting in front of Excel, typing in equations, and pulling a number out of it, right?

Shaughnessy: Right. It's a matter of communication, but that's just part of it.

Holden: At HP, we were in the business of making test equipment, and one of the challenges with test equipment is it has to be about 10 times better than what it's trying to measure. Being very accurate on these things was a hallmark of Hewlett-Packard excellence. Now, the second thing was that we made dielectric testing machines. The first generation went to 1.8

gigahertz, but you could put in a 30-mm disc of a core laminate, and it would give you back all the characteristics of that material.

You could program the computer to do these measurements from 10 megahertz to 10 gigahertz, and from zero to 120° C, and from 30% to 75% relative humidity, and it would give you back a three-dimensional measurement. And the one thing about all FR-4s is that nothing is ever flat, because it changes with frequency, it changes with temperature, it changes with humidity. So, the first thing was that there's no such thing as one Dk for your board. If you're going to do it exactly, you have to run a range of what you think the actual environment is that it's going to operate in.

**If you're going to do it exactly,
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you think the actual environment
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It was so important that I put a separate chapter in the *Printed Circuit Handbook* about characterizing materials because, the more expensive the material, the more stable and less variation you're going to get. If you're sticking with FR-4, it's a very good mechanical platform, but electrically, it's all over the map.

Hargin: Yes, but I think what the fabricators are doing is simpler than what you just described. They're not looking at temperature or humidity or fall results versus summer results, etc. They have a number, and it's at one gigahertz. Your signal may be at 10 gigahertz, but the Dk they'll use is most often at one gigahertz. And they just plug and chug, and here's your stackup.

Holden: Everybody is working with a different set of data books that they created themselves.

Hargin: Correct. And they did it based on backing Dk out of an impedance equation. They

do an impedance measurement and then they solve for Dk in the impedance equation, plug in the impedance that they saw, and try to pull their own home-grown Dk number out of it. To me that sounds primitive; it's not the way I would do it.

Shaughnessy: Is it a matter of the OEMs just claiming ownership of the design, the stackup, everything? I keep going back to what you were saying about the OEMs punting to the fabricator who, as you say, doesn't know all the stakeholders nor has all the info that the OEMs do.

Hargin: Let's say I'm a fabricator front-end design guy, and I'm designing stackups. I might do five or more stackups in a day serving different customers. One of those stackups is the one I'm doing for you, the OEM. But you're doing it the opposite way. You have one stackup that you're doing, let's say, with three different fabricators. In the end, who needs to own the divergent results? It's the OEM that owns it. And, if they own it, they own the result. They need to take more ownership of how the process is done.

If one fabricator is using a Dk of 3.75 and another one is using 3.6, and the laminate vendor has in their tables 3.65, well, you need to understand the frequency of the assumption. Okay, the fabricator is assuming one gigahertz, but what's my signal frequency? And engineers on the design team need to take more ownership of the process. Which laminate numbers would I use? My way of looking at it is I'd measure them myself. Not just on impedance coupons, but if I'm using a material on a consistent basis, I would bring in some of that laminate and measure the raw laminate myself.

Methodologies exist to do that. Our Z-field product does that. And you can remove the uncertainties. You could say, "Well, look, I've measured it myself from zero to 20 gigahertz. Here is the Dk and Df profile for this particular laminate construction." It's all about removing the uncertainty in my mind—unless you're making some boards in Penang, Malaysia, and other boards in a drier climate, and humidity



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is a factor, like Happy was highlighting. Unless that's happening, there shouldn't be a strong reason that one location would have systematically different Dk numbers than another one.

To be honest, philosophically, I don't understand why design teams will spend dozens of hours laying out a circuit board and owning the CAD layout, then maybe dozens more hours using up to \$100,000 worth of EDA tools, to design and simulate designs. Why don't the same people that are putting that kind of investment into the board layout and SI and PI simulation process pay more attention to the spinal cord of their design—which is the stackup—and why do they delegate that to the fabricators? That's a design-philosophy question.

Shaughnessy: You mention TTM. Julie Ellis at TTM recently said, "How can any designer possibly know all of this stuff that I've been working with for 30 years, and I'm still learning?"

Hargin: I actually talked to Julie a week or two ago, and we were talking about pressed prepreg thickness calculations and percent copper. One of the gaps in the design flow is that for a lot of stackups, the fabricators are calculating pressed prepreg dielectric thicknesses based on round numbers. For example, for the percent copper on a specific layer, they might say that, signal layers are 35% copper, or they might say 40% copper, or 50%, whatever they calculated. The fabricator then might use those percentages all day for signal layers, and they might have a number like 90% for plane layers.

But your design has a different percent copper on the various signal layers. Some CAD tools know that. Valor NPI knows that and those numbers could be used in the stackup design flow to refine prepreg dielectric thicknesses and therefore get more accurate impedance numbers. I find that people in this space who I deal with every week get confused about manufacturing process variation. Let's say impedance can be plus or minus 10%, okay? And that's a common standard; some people target plus or minus 5% and pay a bit more with a more expensive fabricator for tighter control. But that manufacturing variation includes copper

thickness variation, Dk variation, percent resin variation, and a thickness variation; all these things that add up to impedance variation.

But you don't want to give away some of that plus or minus 5% or 10% on your nominal values. If you don't center your nominal, and you're off on the nominal, that's a terrible design practice. And people get confused about that. They think, "Oh, it's only a 1% difference. Oh, it's only two, two and a half percent different." But those percentages are eating into your tolerance-tolerance band. So, there's the manufacturing tolerance and then there's the engineering tolerance.

Shaughnessy: It sounds like they're making decisions based on these numbers that may or may not be accurate. I mean, every little trade-off you do can affect something down the line. And like you said, you don't know what the numbers are for each for a prototype shop, much less for overseas. So it sounds like a lot of it is kind of a crapshoot.

Hargin: I would say that an informal description of the design team's job is to reduce uncertainty in their designs. If you have first-pass prototype success, and production is all done on schedule, you've reduced uncertainty down to an optimal level. I'm not really saying it's a crapshoot; what I'm saying is, it's our job as designers, engineers and design teams to reduce uncertainty wherever we can in our design flow. Just because I didn't get bit by something on my last design doesn't mean that I'm not going to get bit by the same issue on my next design.

Glass-weave skew is an example of that. Just because it worked yesterday doesn't mean it's going to work tomorrow. That's how my son thinks when he's driving to and from college. He says, "I don't get tickets." Well, until he got a speeding ticket for going 20 over the speed limit. Anyway, I think we need to reduce uncertainty. That's why I use the metaphor of getting the cattle back into your barn and keeping track of more things than you were keeping track of yesterday. Because when speeds increase, the margin of error decreases.

Your margins decrease as speeds increase. You've got to be improving your design methodology; you can't do what you were doing two years ago, you've got to be improving. That's what engineers and designers are getting paid to do. If you're starting to work on PCI Express 5, you can't use the same techniques you were using with PCI Express 3.

Shaughnessy: Are standards helpful in doing the stackup?

Hargin: Yes and no. The IPC-4562 standard for copper foils is helpful in terms of copper thickness; it gives you a definition of copper thicknesses: how thick is half-ounce copper, and how thick is one-ounce copper. But it handles copper roughness, which is much more important these days, in a nebulous way. The definitions in 4562 about copper roughness are not universal, and they're not current.

Glass is defined in IPC standards, but each manufacturer can create their own wrinkle in how they implement that standard. Some companies like Nan Ya, where both Happy and I used to work, have their own glass manufacturing. But other laminate vendors source their glass from multiple sources. That could be a source of variation.

Holden: Does the Z-zero impedance analyzer replace the HyperLynx analyzer? How exactly is this used by Siemens EDA?

Hargin: We both use the HyperLynx 2D field solver. I've been using that from the get-go in an OEM relationship with Siemens EDA. The HyperLynx 2D field solver is also used by the HyperLynx SI and PI simulator, and it's also used in Xpedition.

The Z-zero software, Z-planner Enterprise, can send data to and from the stackup editor that Xpedition and HyperLynx use. In our environment, there's a lot more detail. For example, in the materials library, we have about 150 materials, and probably another 10 materials, I would say, by the end of this year. We have a lot more granularity, as it relates to stackup and materials, and we send that data to and from Xpedition or HyperLynx.

The other thing we do that's a little different is that our tool realizes that a given production part number may have multiple versions of a stackup. Fabricator A, B, and C, version one, version two, etc. A lot of people think of impedance and stackups as kind of a monolithic concept, but they're pretty nuanced, in fact.

A lot of people think of impedance and stackups as kind of a monolithic concept, but they're pretty nuanced, in fact.

Shaughnessy: Bill, is there anything we haven't covered that you'd like to mention?

Hargin: Just that stackup design has been a passion of mine for a long time. The seeds of Z-zero were planted in my mind back in my HyperLynx days. And I thought that a tool should exist that does what my Z-planner Enterprise product does. I thought that if speeds kept increasing, engineers would need to have a tool that handles the granular details of stackups. And that's the journey that I've been on with Z-zero.

We spoke with you a few months ago about Siemens EDA distributing my Z-planner Enterprise product. As Max Clark and I mentioned at the time, we realized we were both pursuing the same goal: To take manufacturing knowledge and move it to the left in the design process with an EDA tool that would handle all the uncertainties in stackup design.

Shaughnessy: Well, congratulations, Bill. Thanks for speaking with us today.

Hargin: Thank you, Andy, and Happy, it's always great talking with you.

Holden: Thanks, Bill. **DESIGN007**

Stackups: Properly **Conveying Your Info** to the Fabricator

The Bare (Board) Truth

Feature Column by Mark Thompson, CID+, MONSOON SOLUTIONS

In this column, I will discuss how to create the perfect board stackup, specify what you truly want to convey to the fabricator, and eliminate conflicting information about stackups.

What Is a Board Stackup?

The board stackup is the Z-axis stackup showing layer configurations, all specific dielectrics, copper weights, material types, and any information regarding controlled impedances. This is critical to make sure your design works as expected but is a frequently overlooked and underrated part of your output package that is often left up to the fabricator. This can work if you don't have any special dielectric or controlled impedance needs.

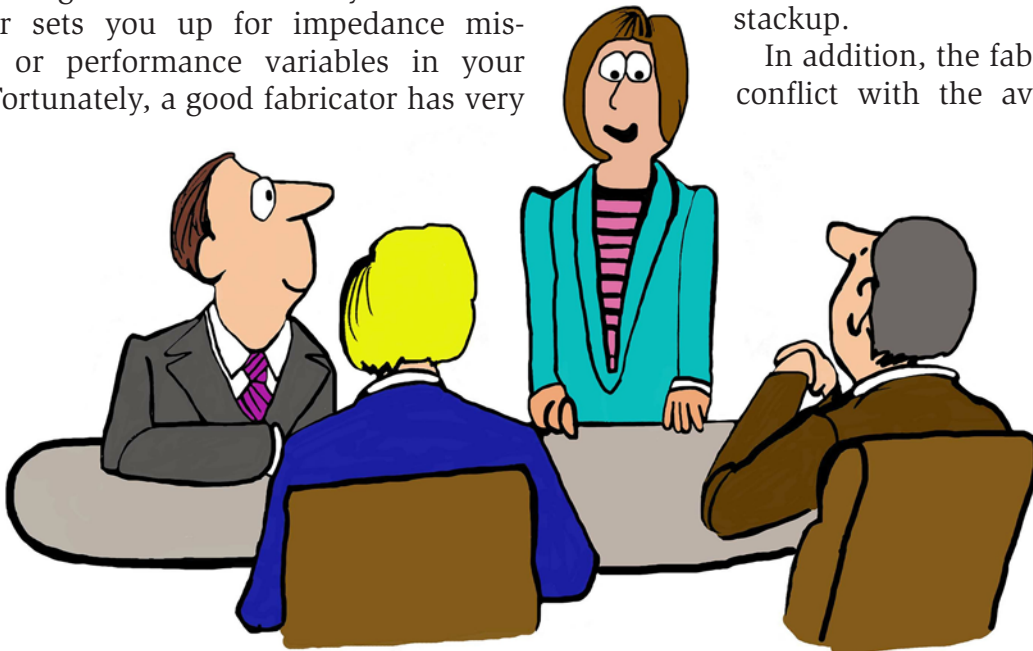
Not sharing those needs with your desired fabricator sets you up for impedance mismatches or performance variables in your design. Fortunately, a good fabricator has very

experienced CAM folks who can recognize serpentine traces as single-ended (SE) structures, differential pairs as controlled structures, and CPWGs likewise as controlled structures. This should lead to an email, or at the very least, a phone call from your fabricator to clarify your stackup intent.

1. Where to Place This Information

The Z-axis depiction of a board stackup is typically on the fab drawing, in a README file, or as a separate sheet depicting the Z-axis stackup, such as a PDF, DXF, spreadsheet, or some other type of document. It is important to remember if you call out material type, copper weights, and controlled impedance information on the fab notes, they should not conflict with what is shown on the separate stackup.

In addition, the fab notes cannot conflict with the available space



"What if, and I know this sounds radical, we clarify our stackup intent for the fabricator?"

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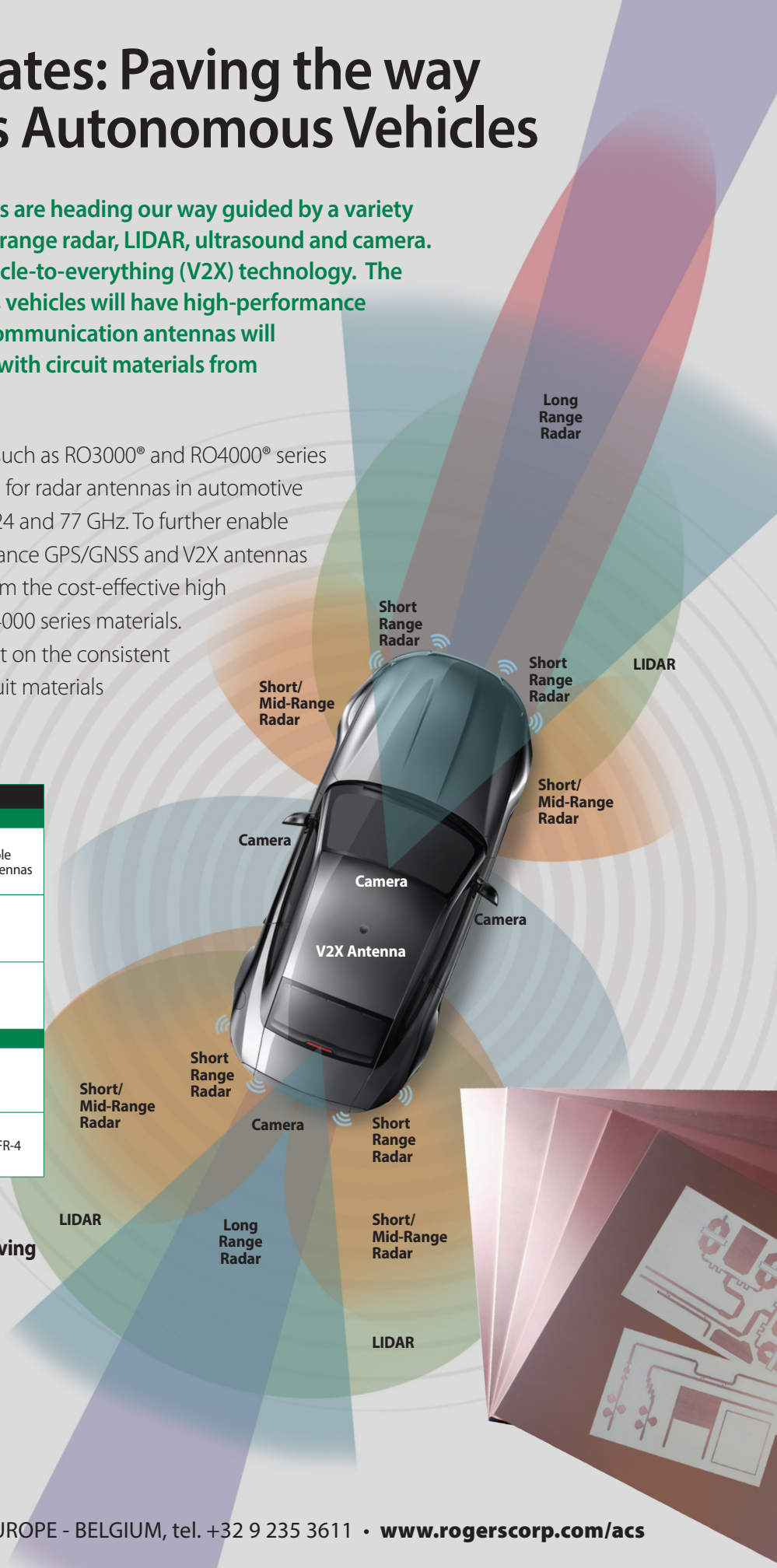
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on your board. For example, if you call out 1-oz inner layers and 2-oz finished outers after plate, the internal and external layer space should not exceed 0.005" or 0.125 mm, and the external layer space (copper feature to copper feature) starting on half-ounce with a 1-oz plate-up should not exceed 0.004" or 0.1 mm. This will save you a lot of grief from a fabricator calling you to tell you your chosen stackup copper weight does not support your available design space.

2. What to Call Out on Your Fab Notes and Stackup

Here is a short list of what to call out on your fab notes and possibly even on your stackup. This information should exist somewhere; whether you choose to have it on both the stackup and in the fab notes is really up to you. But again, if you choose to have the following information on both, they should not conflict with each other, such as:

- Material type
- Desired copper weight (as long as it does not conflict with your available space)
- Specific dielectrics
- Controlled impedances
- Layer configuration

First, call out the material type. I recommend calling out your material by the 4101/# as opposed to calling out a specific material type unless directed by the end-user to do so. This can save you some time in negotiating with the board fabricator, as not all fabricators have all materials in stock or even normally carry them. Some materials, such as the Rogers 3000 and 4000 series of materials, should be built as a core-cap type construction. I would recommend calling out material by name if you have a specific function that requires said materials—things like high temp, high speed, low Dk, low loss tangents, or even the use of very thin dielectrics to take advantage of the inherent decoupling properties of thin dielectrics.

Note: Any use of thin dielectrics for this purpose should reside near the external layers and not in the center of the board stack if at all possible. If you need to call out a specific

material type, consider adding a few alternatives so that whoever builds your part has a shot at having or stocking it. Having said that, some research on your part will be required to evaluate the various materials you are adding as alternatives. They should be true alternatives and consistent with your performance expectations.

Second, call out the copper weights involved. Can you mix copper weights internally? Yes. Many designs depend on the use of core material with a lighter copper weight on one side and a heavier weight on the opposite side, such as a signal side with lower space values and a plane side with higher space values.

However, you should not have a huge mismatch between copper on each side for the sheer processing of the cores through develop, etch, and strip. Something like two- or three-ounce on one side and three-eighths or half-ounce on the opposing side should be avoided, but half-ounce on the signal side and one-oz on the plane side is not at all out of the question. I may be "beating a dead horse," so to speak, but once again, your stackup notes should not conflict with the stackup depiction. I cannot stress this enough. And, as before, the copper weight must fit your available space. Enough said.

Next, call out in the stackup any specific dielectrics but not necessarily on the fab notes as well. Specific dielectrics do not necessarily mean the part has controlled impedances. Some designs require thin dielectrics for close to the outer layers and thicker dielectrics in the middle of the stackup for performance reasons, such as having an eight-layer stackup with a stackup as a signal top, plane layer 2, signal layer 3, plane layer 4, plane layer 5, signal layer 6, plane layer 7, and then signal layer 8, increasing the distance between layers 4 and 5 and keeping layers 1, 2 and 3, and 6, 7 and 8 as thin as possible works well for both impedances and performance characteristics. Additionally, as mentioned before, the use of very thin dielectrics can work well for inherent decoupling and minimizing the amount of decoupling caps needed on the outers if used between PWR and GND layers.

Controlled Impedances

Next, I'm going to cover controlled impedances (Figure 1 and Table 1).

As I have said in numerous columns, first, consult your chosen fabricator to have them assist in specifying the trace widths, spaces, and dielectrics for various impedances. This ensures you won't have to rip up and re-route your impedance tracks and potentially your component placement. I realize many folks do their own calculations, but as I have said

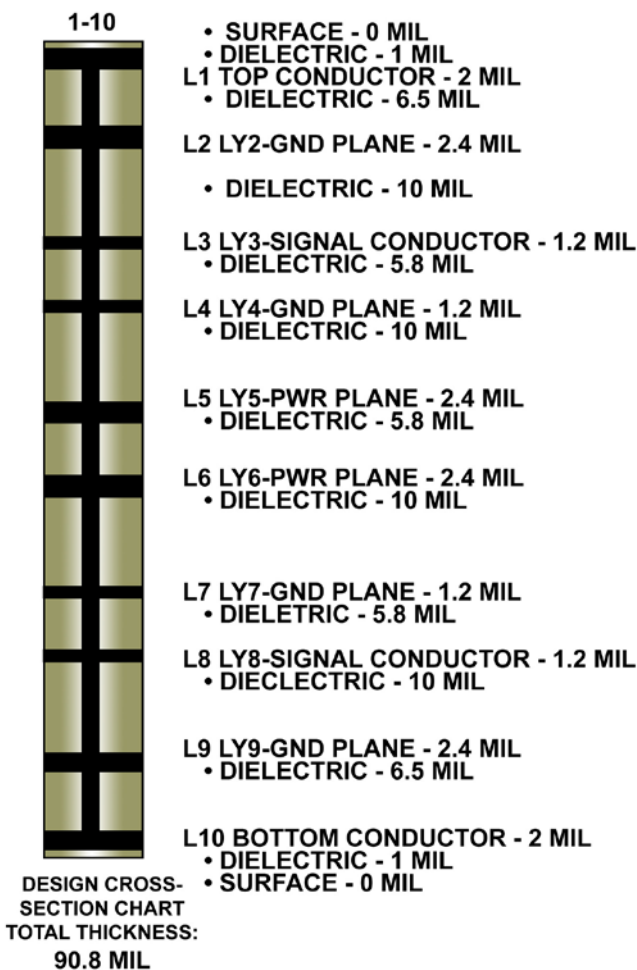


Figure 1: Typical 10-layer stackup.

before, as a designer, all you have to do is to get within 10% of your precalculations, and the fabricator will take it the rest of the way to get even closer to your desired impedances. Simply call out all the impedances that reside on each layer. If you use a template for this description, that is fine, but make some mention if they don't all reside on the called out layers.

As a former fabricator, I understood that they may not exist on the design today but may exist on the design at some point in the future. Thus, when I corresponded with the customers, I would simply say we have calculated for them all but have only included calculations that reside on the design as it exists. Be sure to add a tolerance for the impedances, wide traces, such as CPWGs, on surface layers, which can have as little as $\pm 5\%$. But thinner tracks for single-ended and differential pairs should have a larger tolerance like $\pm 10\%$. If the part has impedances that reside on a blind plate-up layer, the fabricator may even ask for $\pm 15\%$.

Lastly, layer configurations must match the description for both the layer names and the stackup. Any mismatch can cause a delay in your project. Make sure the layer names are also in sequence. For example, a 10-layer board should have layers 1–10 in sequence, not layer 1, 3, 5, and then back to layer 2, 4, etc. This could cause a serious stackup error at fabrication.

Likewise, as I said before, the layer names should be the same in the image data and the stackup. Some mismatches are tolerated and understood, such as calling out a PWR plane on the stackup and calling the actual layer + 5V. This should be understood by the fabricator, but if the names aren't even close, you should expect a phone call or email from your chosen fabricator to clarify.

LAYER	IMPEDANCE	TRACE / SPACE	REFERENCE	TOLERANCE
1	100 OHM DIF	6 MIL / 6 MIL	LAYER 2	$\pm 10\%$
10	100 OHM DIF	6 MIL / 6 MIL	LAYER 9	$\pm 10\%$

Table 1: Typical impedance chart.

Blind/Buried Via Stackups

For a blind or buried via stackup, you will want to remember a few things if you want to be able to send the stackup to just about any fab shop (Figure 2). Most fabricators can do

blind/buried vias, but some have constraints on what they can do based on their process.

First, try to make the blind vias terminate on a plane layer, such as a GND or PWR layer or even a split plane, not a signal layer. (See the

Layer	Base CU / Plt	Thick	Type	Stackup	Subs	Imp	Material	Dk
Silkscreen		0.00					Taiyo-SS - White	
Soldermask		0.60					Taiyo-SM - Green	3.90
Lyr1	0.25oz / ML-1010	1.80	P			1,2		
Prepreg		8.60					R-5670K - 1080_64%	3.40
							R-5670K - 1080_64%	
Lyr2	1oz	1.20	P					
Core		12.00					R-5775K - 12.0mils	3.64
Lyr3	1oz	1.20	P			3,4,5		
Prepreg		11.27					R-5670K - 3313_54%	3.64
							R-5670K - 3313_54%	
Lyr4	0.5oz	0.60	P					
Core		4.00					370HR - 4.0mils	4.23
Lyr5	0.5oz	0.60	P			6,7		
Prepreg		11.73					R-5670K - 3313_54%	3.64
							R-5670K - 3313_54%	
Lyr6	0.25oz / BV1	1.50	P					
Prepreg		5.33					370HR - 106_76%	3.74
							370HR - 1080_71%	
Lyr7	0.25oz / BV2	1.50	P					
Prepreg		7.46					R-5670K - 3313_54%	3.64
							R-5670K - 3313_54%	
Blank		0.00	B					
Core		12.00					R-5775K - 12.0mils	3.64
Blank		0.00	B					
Prepreg		4.00					R-5670K - 3313_54%	3.64
Blank		0.00	B					
Core		12.00					R-5775K - 12.0mils	3.64
Blank		0.00	B					
Prepreg		4.00					R-5670K - 3313_54%	3.64
Blank		0.00	B					
Core		12.00					R-5775K - 12.0mils	3.64
Lyr8	0.25oz / Std	1.50	P					

Required Thickness

Type	Req. Thick	Tol% +	Tol% -	Act. Thick	Measured
Overall	117.0	10.0	10.0	114.9	
Over lamination	114.6	10.0	10.0	111.6	
Over laminate	113.4	10.0	10.0	111.0	
Over metal	117.0	10.0	10.0	114.3	
Sub-assembly 1 - 6				51.8	
Sub-assembly 1 - 7				58.6	

Figure 2: Typical blind via stackup.

reason not to do this in my second point later.) Having said that, we see many high-speed and RF designs where this is a negative. Having any via stub can be an issue.

Second, avoid having signal integrity needs such as controlled impedances on a blind plate-up layer if you want to be able to send the job to any fab shop. Many fabricators process a blind or buried via scenario where they laminate the blind or buries and then drill the scenario instead of doing controlled depth type drilling to drill said scenario after final lam. This means the layers are typically imaged and plated for the termination layer, such as a layer 2 in a blind 1-2 or layer 3 of a blind 1-3 after they have imaged/plated then laminated the blinds in the first cycle press.

Since this plate-up can have some slight copper thickness deviations after plate due to the plating process variable, they ask that you do not have the blind plate-up layer 2 or the layer 3 for an impedance layer in such a scenario as the ones described previously. If this cannot be avoided, and a controlled impedance layer must reside on a blind plate-up layer, they may ask for a higher tolerance for the impedance, such as $\pm 15\%$.

Third, having a controlled impedance layer on a blind plate-up layer means that controlled dielectrics as the interface where the blind via controlled impedance resides requires a specific dielectric to achieve said impedances. This is where it gets tricky if the termination

layer is controlled, as attempting to emulate a thin dielectric with prepreg between cores or foil internally for a blind scenario means you will have to consider the additional blind plate-up. This is usually a typical value of 1 additional mil of plating, reducing the thin prepreg dielectric even further and setting yourself up for high resistance shorts and an impedance mismatch.

These three things should be considered if you don't want to pay more, increase your lead time, or live with a higher impedance tolerance. And you'll be able to send your design to just about any fabricator.

Conclusion

These are the things on a short list of what every stackup should have. I hope this has helped. As usual, if you would like to comment on this column, please do; I greatly appreciate the feedback. I can be contacted at markt@msoon.com with your questions and comments, and, as always, thanks for reading! **DESIGN007**



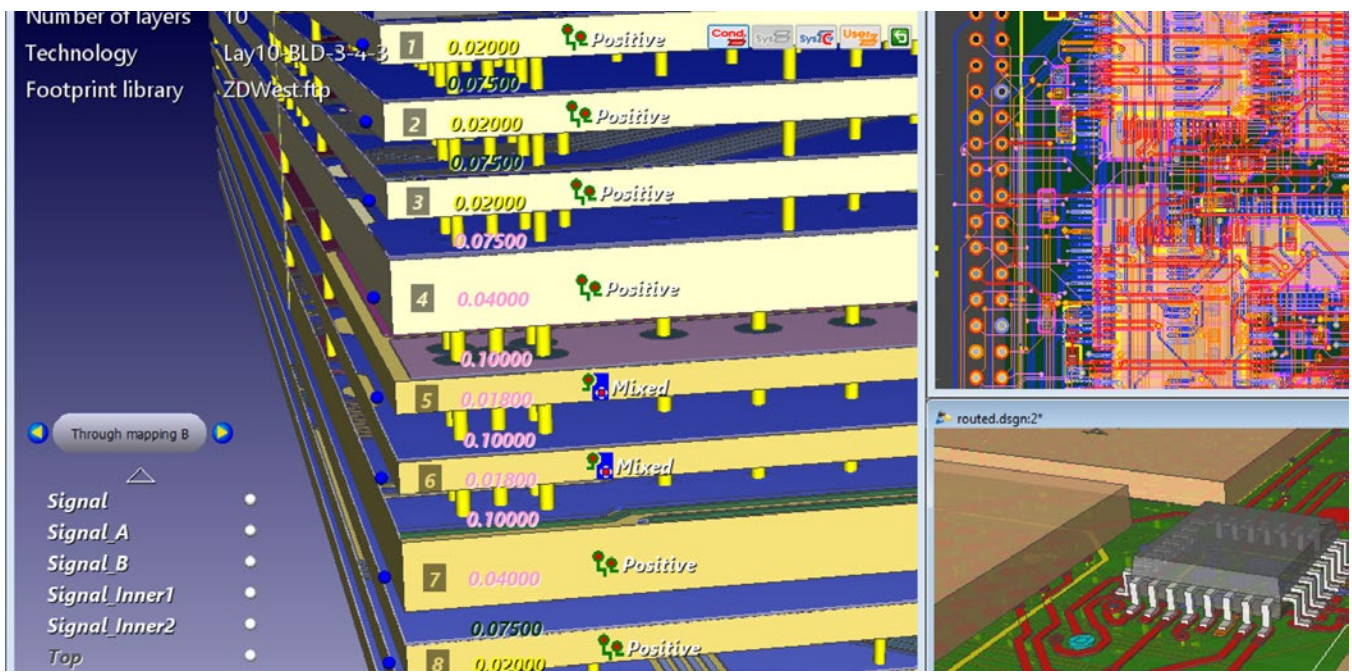
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Martyn Gaudion on Stackup Design Considerations

Feature Interview by the I-Connect007 Editorial Team

The I-Connect007 team met with Martyn Gaudion of Polar Instruments to discuss the ins and outs of stackup design, and why designers seem to be getting stackups wrong, especially if a board is going into volume production overseas. Martyn explains the many trade-offs involved in even the simplest PCB stackup, and why many OEMs are now using brokers staffed with former fabricators to help them address complex stackup challenges.

Andy Shaughnessy: Martyn, why don't you start by explaining why it's so important to get stackup design right? And why do we keep seeing all these problems with stackups?

Martyn Gaudion: One of the main things is really about designers and fabricators communicating with each other. Also, what has happened in the last 10 years is a huge proliferation of materials. You can get materials that are great for thermal, materials that are great for high speed, and materials that are great for reliability. Suddenly, every material

vendor, instead of having just FR-4, now has a whole range of specialized materials that do different things at a suite of price ranges as well. I think it's important to make the point that at Polar we don't see ourselves as stackup experts; instead, we see our customers as the experts. We always want to make sure that the fabricator, who's got the expertise on the fabrication side, really communicates strongly with the design authority, because that is when communication can break down. The problem starts when you don't have sufficient communication between fabrication and design.

Shaughnessy: There are so many tradeoffs that must be made by the designer on each stackup.

Gaudion: With ultra-high-speed designs, we sometimes find that designers want to specify the design very rigorously, and they're not fully aware that the fabricators are going to plate the copper. They'll specify very smooth copper on the cores. But then, of course, you're going to drill and plate it. Then, actually, what you have on the core, once it's plated, or once the holes are plated up, the roughness isn't going to be the same as on the base material.



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Martyn Gaudion

Understanding where the drillings are and all of that is really, really important to make sure that you get what you think you're going to get. We certainly see that culture in some big OEMs where they say, "Just listen to us; we're this major OEM and you do it the way we say." The fabricator says, "But there's drilling on that layer, so we're going to plate it." And the OEM replies, "No, no, we specified the copper to be this level of foil," but they forget that it's plated. It gets worse when there is a supply chain involved where it might be prototyped in one place and put into volume somewhere else.

Dan Feinberg: Martyn, what percentage of boards do you think are FR-4 now? It's certainly not close to 100% like it was 20 or 30 years ago. Is it still mainly FR-4?

Gaudion: We tend to see the high-end fabricators, so we see a huge number using modified FR-4s or ceramic-filled materials and higher speed materials. But there's still an awful lot of boards that are four layers for general purpose use that stay with basic halogen-free FR-4s. What we start to see are people mixing mate-

rials where they've got the low-speed layers on basic materials and then they'll mix them with a more expensive material to carry the high speed. You get stacks which are a mix of different materials, and there it's really important that the designer talks to the fabricator to make sure they can actually laminate them and they actually bond them together because that becomes an issue.

Feinberg: That's always been a thing for me. Designers and suppliers should communicate better, and it seems like they are starting to communicate better. They didn't communicate at all years ago.

Gaudion: Communication has improved because it had to, and we see that reflected in requests to put even more detail into our stackup tools. I guess where we see a challenge is in terms of where we carry the data in our stackup tool, which isn't necessarily carried along with the CAD data. So if ODB++, IPC-2581 or Gerber doesn't have the right data for the stackup, you still need to carry a stackup file separately from the CAD because there's a lot of Z-axis information in the stackup which isn't always in the CAD tools.

We've also noticed that in the last 20 years, certainly in the U.S. and Europe, many of the skilled people from fabricators have ended up working for a brokerage. Now, there are some really good high-end brokers who have a number of PCB fabricator people there who can talk to designers, and that's been a big difference.

Historically, you might have thought, "Why would a broker want a stackup tool?" But now a lot of brokers use a stackup tool because they're actually assisting the designer because they're PCB people. Sometimes I find the designers don't really want to communicate too much because they might feel they're exposing their limited knowledge of PCB fabrication. They can be quite reticent about that sometimes—certainly the European designers—and we encourage them to ask those sorts of questions. The high-end brokers are very good at providing that interface between fabrication and design.

Happy Holden: Stackup has been a fundamental characteristic of PC boards ever since we moved off double-sided. That's always important because, even a long time ago, certain signals were transmission lines, which means they needed a reference plane for the return. What has always been in contention was what thicknesses people used because, with material that you buy, it depends on the process what the final thickness is going to be, which then determines the impedance. Electrical engineers, not knowing enough, looked at the material specs of the raw material to determine thicknesses. Those in the know realized they had to go to the PC shop to say, "For this particular material in your process, what will be the finish thickness?"

Gaudion: We still see that, Happy. Somebody says, "But I've seen the spec and this is what it is. It's 75 microns plus or minus four microns." And you say, "Yes, but that's pressed. You're already going to find the finished thickness, and it's going to depend on the copper density, the layer, and vary from fabricator to fabricator." Certainly, within our tool, we can simulate the pressing, but the simulation is still only a simulation.

Holden: I remember the big change when we finally had to go to field solvers from equations, because the errors in the equations were beginning to be significant. Suddenly, field solvers were required to really get the right numbers.

Gaudion: That was a big change for us. Certainly, back 25, 30 years ago, we had an equation-based tool and then moved on to field solvers. Then, as the speed pushed up past 2, 3, 4 gigahertz, then bringing insertion loss in again, that became an ever increasing and important part of the equation. It's a thing we're seeing now where the focus is more on how smooth the copper is, and actually, we've done some tests for some customers where they want to look at the pretreatment of the copper to see when they're using adhesion promoters; more and more, newer adhesion promoters are being made smoother and smoother, so that they're

not actually roughing the copper up as much as they used to.

Holden: That brings up an area of stackup that we never talk about, but we ran into a lot of problems with—the stackup has to include what's going to be on the printed circuit board, through assembly and afterwards. It took a lot of education for designers to understand that these magnetic fields go out into space. Number one, we assume that it's air, it's dielectric constant. But if you put on a thermal grease, and then put on a heat sink, and it's covering over traces, then it is more than just the solder mask and air. Now you had better add in your thermal grease or adhesives, and your heat sink, because they're going to affect the transmission line. It's not just the material, it's a three-dimensional issue.

Gaudion: That's right. Sometimes, we recommend that you maybe put critical traces like that on inner layers so that they're away from the surface. If they're running as striplines—rather than microstrips—you have better control over that kind of thing because you've got at least a plane between you and what's going on the surface to keep the surface stuff out of harm's way. But it's not always possible, and if you are doing stuff on the surface, you need to route around some of those problems.

That's an area we're doing some work on—not with conformal coatings, but with shields. Certainly, we see a significant number of PCBs where there's an EMC shielding material on the outer layer, so looking at how that impacts things is an area, and actually documenting just the sheer fact that whether it does have a shield on the outer layer is something that we're finding increasingly important. It's something we're looking at adding into our tools next year, because certainly in cellphones and tablets and things like that, you see a lot of shielding.

You have to think about designing the whole of the Z-axis, whereas the CAD designs the X and the Y. We're looking at the Z-axis all the way through to the enclosure, the air, or whatever is at the boundary layer.

Holden: Yes, and now with the VeCS, the 3D aspect of the stackup has added another layer of complexity. Have you started looking into how you're going to handle the vertical conductive structure?

Gaudion: I met Joan Tourné last year and we talked about VeCS. We haven't looked at it yet, but we're usually driven by our customers. When our customers start to approach us with questions on VeCS, then that's a technology that we would look into. We tend to be driven by customers. We get so many requests for enhancements on our stackup tools that just juggling them to find which one we need to focus on is tricky. VeCS is a very exciting technology, Joan is a very creative guy, and so we sit and wait for our customers to come out and say, "We're using this. How are you going to document it?" It opens the ability to increase the interconnect density without really increasing the complexity of the board, which is a very clever piece of engineering.

Holden: I gave a keynote talk on VeCS at the Electronic Circuits World Convention in Hong Kong with some of the new diagrams. It's really quite interesting to go from layer one to layer 18, which we can't do with HDI or anything else. But in the same channel, we could go to layer six, or layer four, or layer 12, or layer 28. And, interestingly, we could do this with excellent reliability, and the signal integrity improves significantly.

Gaudion: Certainly, what Joan was explaining is that the beauty of it is you can use conventional manufacturing technology to do it. The challenge is getting the CAD tools to support it, and that's really the interesting path forward on that technology. The ability to not need to up the technology in the fab shop, and actually get a lot more interconnectivity without needing more complexity, is very creative.

Holden: I'm looking forward to fabricators experimenting with it. Since they don't need to drill microvias, if they have laser drilling, they can use their lasers to produce the channels a lot

faster than we can with a drill router machine. I always talk to students about this—if you're choosing the electronics industry, the innovations and changes are constant. The only thing you've got to recognize is this is not the last time you're sitting in class. If you're going to go into electronics, you're going to be in a classroom and learning for the rest of your career.

Feinberg: That's so true.

Holden: Nothing is static in this industry. But with circuit boards, for some reason, we're still making single-sided phenolic print and etch (laughs).

Gaudion: It's interesting that the old technology stays, doesn't it? Then you get all this new stuff laid on top of it. At one time, we thought as speeds go up people won't really need to be worrying about just reflections and impedance. Insertion will also become the primary thing, but with most PCBs, there are some parts that run next to DC, there are other parts that run at a few hundred hertz, and other parts that run at a few hundred megahertz; then, some are two-, three-, 30-gigahertz and you've got a whole range of frequencies and everything needs to be designed to work for the right price for the kind of performance level that's needed. It's interesting that the need to check for opens and shorts doesn't go away just because there's a new high-speed technology.

Shaughnessy: I don't know if it's tribal knowledge, but I've seen designers approach the stackup process in so many different ways. Maybe that's a big part of the problem?

Gaudion: If you look at the money, the fabricators jokingly say that the designers who think about stackup last will keep asking to add another couple of layers of HDI. If you're a prototype manufacturer, and the designer has to build a stackup first and they make a 12-layer board, and then they spin it to 14 and then 18, it's happy days for the fabricator, but it's not the most efficient way of doing things. If they can start on a stackup first, then actually that's

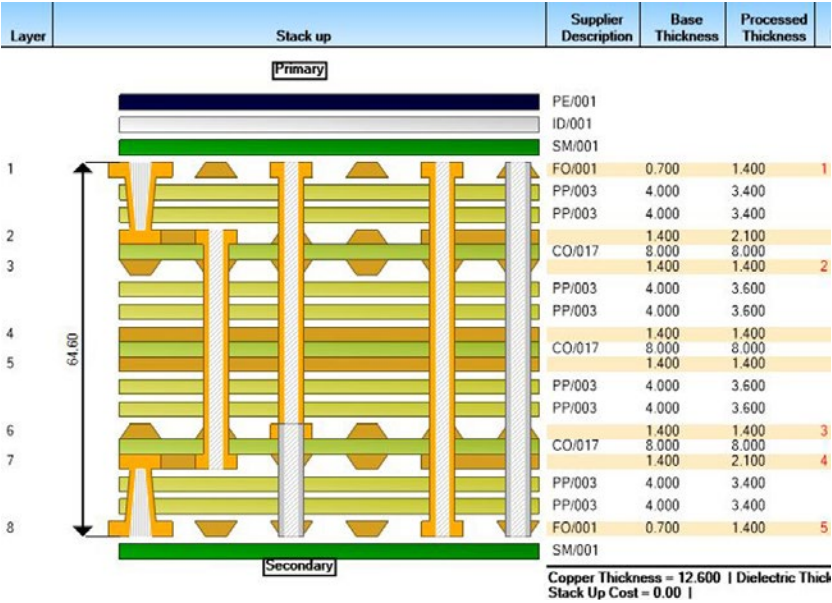
a better way of doing things. With very complex boards, the bigger OEMs certainly work on stackups and have recommended stackups for different types of design. It's certainly our recommendation for complex work that you think about stackup first.

Shaughnessy: We hear these horror stories where somebody will design a board, it gets prototyped in America, and it'll have five-mil traces, and then they want to send it to their Chinese volume guys who say, "We can't do that; we can't go that small." It's like they didn't even think about that. Of course, the designers, in their defense, often don't know where it's going to go for volume.

Gaudion: And that's where I was talking earlier about brokers. Some of the brokers are very good. If you speak to these brokers and say, "We'd like a prototype shop and a volume shop," they'll know who to speak to about both the prototype and the volume. I think brokers have got quite a role to play in that area because they're doing this for lots of people. If you're a designer, you're going to spend most of your time designing, not doing stackups. You don't get that skilled on stackup because you're spending all your time doing the layout. Using somebody who's familiar with stackup is a good thing.

Shaughnessy: Since you haven't plugged your own company, I have to mention that someone recently told me, "Thank God for Speedstack." They were manufacturing a fairly complex board overseas and the CAM people didn't speak much English, but the software was so visual that they could look at the stackup and see, "Oh, yeah, that's what they mean," and it worked fine.

Gaudion: Yes, we're lucky that the lead engineer on Speedstack has a background in fabrication. We've got some really good graphic



arts people who make printouts look crystal clear, which makes the stackups easy to read, and that's useful.

Shaughnessy: When you're planning these tools, is it primarily based on feedback from customers? I'm just curious what the process is.

Gaudion: It's feedback from customers. It's a huge challenge, because every four months or so we have a planning meeting to run through maybe 200 to 500 requests from people who say, "I really need Speedstack to do this." Clearly, we can't do all of the requests. We have to prioritize and figure out which thing we do, and which will be useful to the most people. The challenge to make the enhancements benefit everyone is quite an interesting process, because you want to make sure that what you do for one customer doesn't mess things up for another. I'm sure you're aware of software where you get an update, there's lots of new features, and your favorite feature in the old one has gone away or it doesn't work quite the same. We try to avoid getting stuck in that trap, and sometimes that limits us as to what we can do.

But it is customer-led rather than us having a good idea. I think when we started off we had a good idea and then the customers took over and drove it; and that's where we are now.

Shaughnessy: Do you think out of ODB++, IPC-2581 and Gerber that any one of them do a better job at representing stackup intent?

Gaudion: They all do a job. The challenge we have is that because our tool is dedicated for stackup, we can end up putting more information in our tool than the other formats can take. We can output 2581. We have an XML format which contains all of our stackup information, but there probably isn't any one CAD tool that can take all of the information. If somebody says, "I think there are tolerances in the plating on this particular layer," and we put that into our tool, it may be that there isn't a container for that in the other format. Where do you put that data that's been requested by some customers that isn't in the CAD tools yet? There's always a lag between us putting things into the stackup and the formats out there taking them.

Shaughnessy: I just wonder how much of it goes back to designers being incomplete or, as we found out in our fab notes issue, everybody does their fab notes differently and the designer is just providing incomplete or erroneous data.

Gaudion: We see a huge range of designers, PCB technologists, and those guys in the bigger OEMs that work with designers to make sure that they understand the difference between finished thickness, plated-up thickness or unplated thickness. Those skills are increasingly important to have, especially when things are running at high frequencies where it is as important to consider the copper finish as it is to consider the base material. Take the best laminate for high-speed performance—if you put a very rough copper on it then it's not going to perform so well because you're going to lose signal in the copper. That's interesting for us. We keep seeing ourselves exposed to

different parts of the industry as technology changes. When we started doing impedance, we just calculated impedance for fabricators, and then the laminate suppliers got interested. Past that, the foil suppliers started to get interested. What we're saying now is we're having more and more communication with chemistry suppliers because they're working on chemistry to promote adhesion that is smoother.

Also, moisture is certainly very bad where high-speed designs are concerned. If you've got humidity, water has got very high dielectric absorption. If you get any kind of hydroscopic nature in solder mask and you have traces on the surface, humidity can affect the high-speed performance. You want the outer layers to not be hydroscopic. When you talk to the manufacturers, they say, "Our ink is really good, but it's actually dependent on how well the fabricator cures it." Again, it's an area you wouldn't have even thought of before, but now there are things that come into play

that wouldn't have otherwise come into play maybe 10 years ago.

Shaughnessy: I think a lot of it does just seem to come down to communication, like 90% of the problems that we write about.

Gaudion: We talked about different countries, and certainly in some countries I've heard designers say, "We really want this specified, and we don't want to speak to a PCB fabricator. We'll get all the data, and all the material data sheets, and we'll put everything together. And if we spec it right, then it will work." It doesn't happen all the time, but maybe in 5% or 10% of the time, a designer would further think that actually by specifying the materials out of the datasheet they will get what they want. As Happy explained, fabrication isn't taking standard materials and gluing them together, you're actually plating, pressing things



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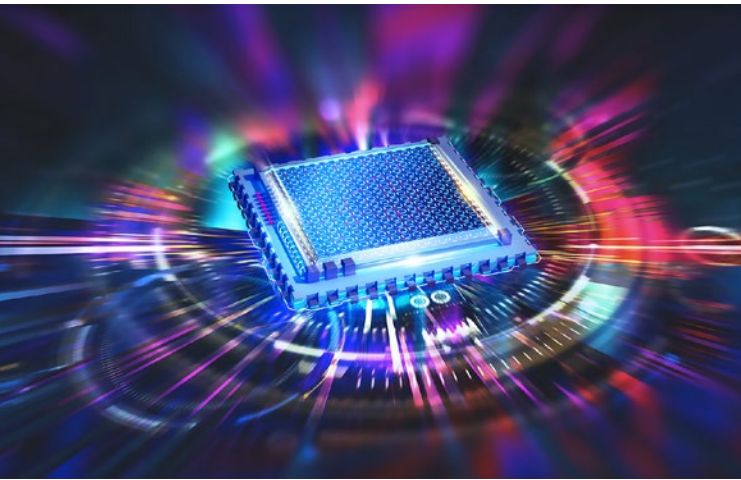
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together and squashing out some of the resin. All those manufacturing processes change the raw material; you've taken the shelf stock into something else once they've gone through the pressing and curing processes. That's really the big difference compared with an assembly of a product versus the fabrication of product. You're actually doing stuff and changing the materials in the PCB manufacturing process.

Holden: The one thing that is important to stackup that we haven't covered, is the fact that we're now going to need more accurate dielectric constant dissipation factors for different prepregs in different cores and the different materials, and we're going to need it measured out not at one megahertz or 10 megahertz, but at 10 gigahertz and above. I don't know if the material suppliers are going to step up and actually provide the technical information about their materials, because it's not simple.

Gaudion: It's not simple, but some of them are. In our material partner program, we deal with 20 or 30 different material suppliers, and some do a really good job of giving data at 1, 10, 20 gigahertz so we've got different frequency data. In that case, some have more frequency data than we can cope with. It's an interesting area where some of the guys that want to push the high frequency area, they're actually working very hard on qualifying the material. There's been an improvement on that, I would say, in the last five years. There are some well-known material fabricators, if you ask them,

they've got good art applications people who will give you VNA data and TDR data, and actually will have extracted the Df up to 10, 50, or even 70 gigahertz, say for automotive applications. That's a big improvement.

We've done some experiments where we bake the boards, and you can see the insertion loss fall off once you bake them; some perform better than others. In terms of high-speed digital, one thing that's a bit more forgiving is that you're looking at the new high-speed serial comms chipsets. They have adaptive pre-emphasis and equalization, and dynamically, the silicon can be a bit more forgiving. At the lowest speeds when you're worried about reflections, the chipsets tend to send a higher load and you have to deal with the reflections. But at the ultra-high speeds, they're using pulse-shaking techniques and things like that, which gives a bit more wiggle room so they can do a bit of dynamic tweaking to minimize the error rates.

Shaughnessy: Martyn, do you have any final words of advice for designers dealing with stackup issues?

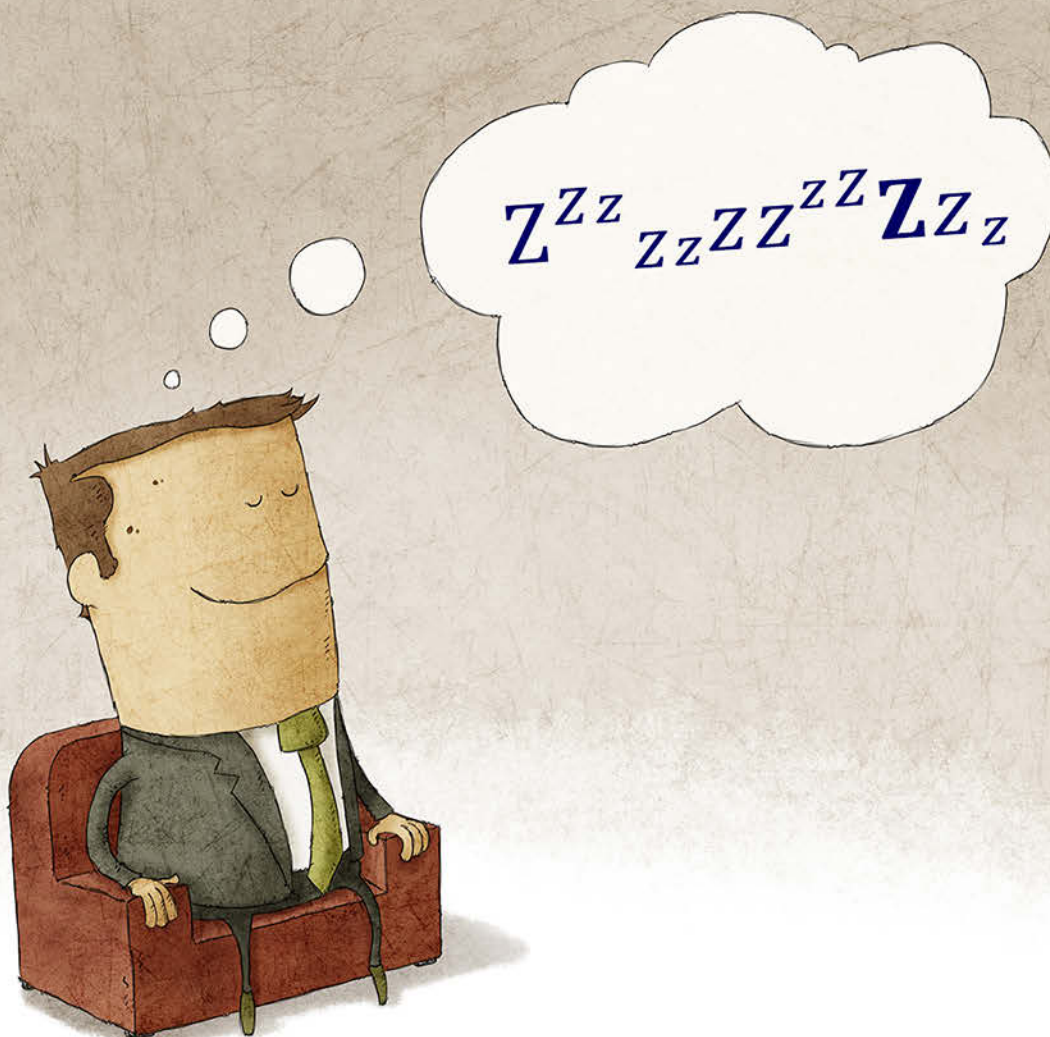
Gaudion: I think it's the same as I always say: Speak to your fabricator and if you're not in close contact with your fabricator, then use one of these value-added brokers who has fabrication people who understand stackup themselves. They are invaluable to work between you and a fabricator. And other than that, establish a direct connection with the fabricator to go through any stackup issues. Don't just assume that the material you get off the stock shelf is what's going to end up in the finished product because it gets processed first. That would be my conclusion.

Shaughnessy: Good stuff. Thanks for talking with us, Martyn.

Gaudion: Thank you all. **DESIGN007**

For more information, read Martyn Gaudion's I-Connect007 eBooks *Secrets of High-Speed PCBs, Part 1* and *Part 2*.

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Stackup Planning: Three Decades of Innovation

Beyond Design

Feature Column by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

The multilayer PCB is the most critical component of an electronics assembly. If it fails, your system fails! The PCB is so fundamental that we often forget that it is a component, and like all components, must be chosen based on specifications to achieve the best possible performance of the product.

Stackup planning involves careful selection of materials and transmission line parameters to avoid impedance discontinuities, signal coupling, unintentional return paths, high AC impedance and excessive electromagnetic emissions. Materials used for the fabrication of multilayer PCBs absorb high frequencies and reduce edge rates thus putting the materials selection process under tighter scrutiny. Ensuring that your board's stackup and impedances are correctly configured is a good basis for stable product performance.

In the late 1980s, my colleagues and I were designing relatively high-speed broadband

communications products (Figure 1). We knew that the impedance of the digital transmission lines had to be between 50–60 ohms but had no way of determining the exact value. Then, in April 1990, the IPC-D-317 standard was released. This was the first guideline for Electronic Packaging Utilizing High-Speed Techniques that incorporated transmission line equations. Problem solved?

However, punching the numbers of the lengthy equations into my scientific calculator seemed to always result in different values. As frustrating as this was, I tolerated it for years until finally in 1995 I had the idea to simplify the process by creating an online multilayer impedance calculator that everyone could use. This tool was based on the IPC-D-317 standard (now IPC-2251) closed-loop equations which are, in reality, just approximations—but it was the “best guess” for its time. Field solvers first appeared about five years later but were too expensive for the average punter.

Free online tools are great but to realize some return, in 2010 I imported the equations to a Windows application, coined the term “stackup planner” and started to build on its functionality. Later, a 2D Boundary Element Method (BEM) Field Solver was integrated into the iCD Stackup Planner to achieve industry-leading accuracy. iCD then continued to develop applications with high-speed design features specifically for PCB designers. These included the iCD PDN

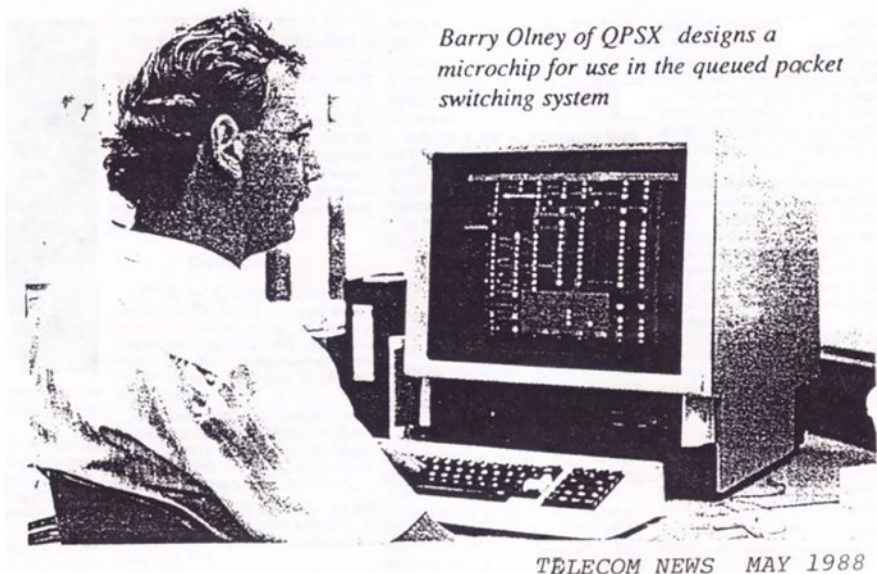


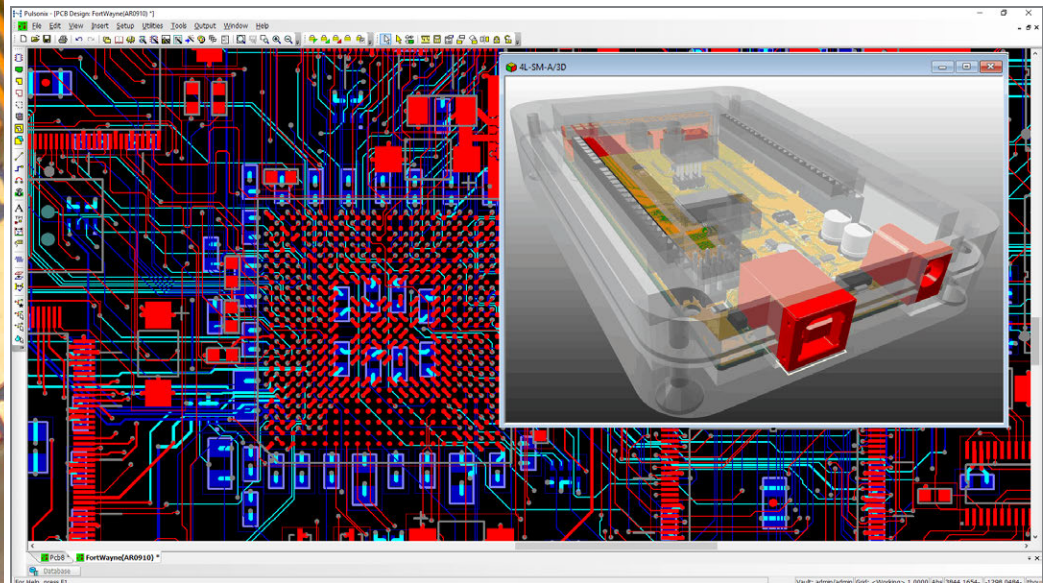
Figure 1: Designing a multilayer PCB using Daisy, Board Master, Unix software.

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Planner, iCD Coplanar Waveguide Planner and the more recent iCD Materials Planner software.

Over the years, I have also written many stackup planning and material selection application notes and columns. Rather than repeat all the valuable points, made in these articles, I will list them below:

1. Arguably the most downloaded (and most plagiarized) is **Multilayer PCB Stackups**. You can find this article in numerous sites on the internet but sadly not attributed to me. It covers stackup planning basics and looks at the most common multilayer configurations (4-16 layers) and their associated pros and cons.
2. **The Perfect Stackup**: This application note discusses how to plan a multilayer PCB stackup to obtain the ideal stackup for high-speed design. Stackup Planning Parts 5 and 6 elaborate on this.
3. **Stackup Planning and the Fabrication Process**: Before starting a PCB design, we need to plan the PCB stackup for optimized performance, ensure that the selected substrate materials are available and clearly document the stackup so that it can be fabricated to engineering specifications.
4. **Stackup Planning Part 1**: The PCB substrate must be selected based on specifications to achieve the best possible performance of the product.
5. **Stackup Planning 2**: Comprises definitions of basic stackups starting with four and six layers. Of course, this methodology can be used for higher layer count boards—36, 72 layers and beyond.
6. **Stackup Planning Part 3**: Looks at higher layer-count stackups. As the layer count increases, these rules become easier to implement but decisions regarding return current paths become more challenging.
7. **Stackup Planning Part 4**: Ten plus layers require very thin dielectrics to reduce the total board thickness. This naturally provides tight coupling between the adjacent signal and plane layers reducing crosstalk and electromagnetic emissions.
8. **Stackup Planning Part 5**: To achieve the next level in stackup design, one needs to not only consider the placement of signal and plane layers in the stackup, but to visualize the electromagnetic fields that propagate the signals through the substrate.
9. **Stackup Planning Part 6**: Impedance variables. Interconnect Impedance is a trade-off between the variables—trace width, trace (copper) thickness, dielectric thickness and dielectric constant. Then, if you also need to include differential impedance, the trace clearance comes into play. For minimum crosstalk, coupling also must be considered.
10. **Material Selection for Digital Design**: What types of materials are commonly used for digital design and how to select an adequate material to minimize costs.
11. **Material Selection for SERDES Design**: Many challenges face the designer working with new technologies. For SERDES—high-speed serial links—loss, in the transmission lines, is a major cause of signal integrity issues. Loss can be mitigated by the correct selection of materials.
12. **It's a Material World**: Precise material selection is crucial to the performance of the today's multi-gigabit designs.

Design techniques constantly change and the current best practice for high-speed stackup design is:

1. Closely couple GND/PWR planes on layers 2 and 3 and the second and third layers from the bottom (Figure 2). This lowers the AC impedance of the PDN and provides low inductance power to the devices.

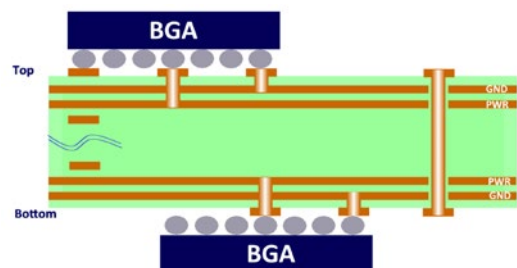


Figure 2: Plane pairs close to BGAs.

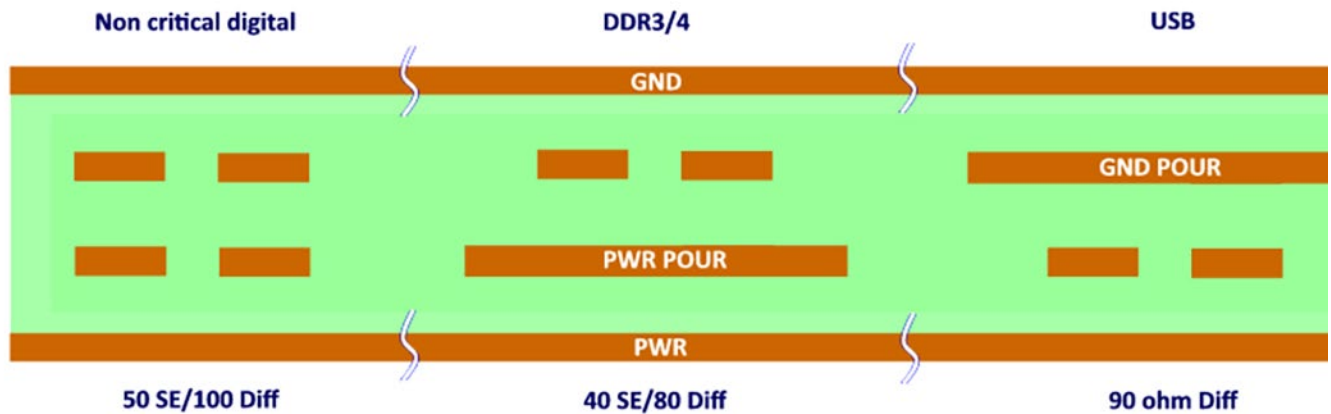


Figure 3: Three technologies accommodated on the same stripline layers.

II. Control electromagnetic fields by using dual stripline mixed signal/plane pour layers to isolate critical signals.

In Figure 3, there are three technologies on the same stripline layers. This is accomplished by using a combination of copper pours on one or the other signal layers. Trace width and spacing can also be modified to trim the impedance.

There are many advantages to this configuration including:

- This configuration isolates critical signals and accommodates all the necessary power supplies in complex designs
- DDR3/4 data or address busses can be routed on separate regions using the DDR supply and GND as reference planes
- Adjacent signal traces for the noncritical digital signals should be routed orthogonally to avoid crosstalk

III. Closely couple the signal layers to the reference planes to reduce crosstalk and radiation.

After reading all the above, you will now be extremely knowledgeable about stackup and material planning. But what is crucial for a good stackup design?

A. Field Solver Precision

As mentioned, closed loop equations are in reality just approximations. You can make do with approximations on low frequency, non-

critical designs but they just don't cut it in today's high-speed environment. Equations particularly come unstuck in dual asymmetric stripline configurations.

The most essential design tool for optimizing the stackup of a PCB is the 2D field solver (e.g. Figure 4). It is used to predict the characteristic impedance, edge-coupled and broadside coupled differential impedance for all topologies, including microstrip, stripline and dual stripline. In addition to the accuracy, the other advantage is its ability to include second-order effects such as trace thickness and the influence of air, solder mask, and multiple adjacent prepreg dielectrics. 3D field solvers are not more accurate than 2D field solvers in stackup design. When interconnects have a uniform cross-section, a 2D field solver can be more precise, faster and much easier to use.

To give you an idea, iCD now has a choice of over 700 series of rigid and flexible dielectric materials, from over 60 different manufacturers, in its dielectric materials library. When each material is used for the right target application, the resultant PCB will have the lowest possible cost while still satisfying the design and performance goals of the project. Choosing the best material for an application is often a daunting task. However, you can quickly sort through the vast array of choices, to make an informed decision, with the right tools.

Typically, when the impedance of a substrate is first calculated, virtual materials are used as the basis. In other words, we choose a

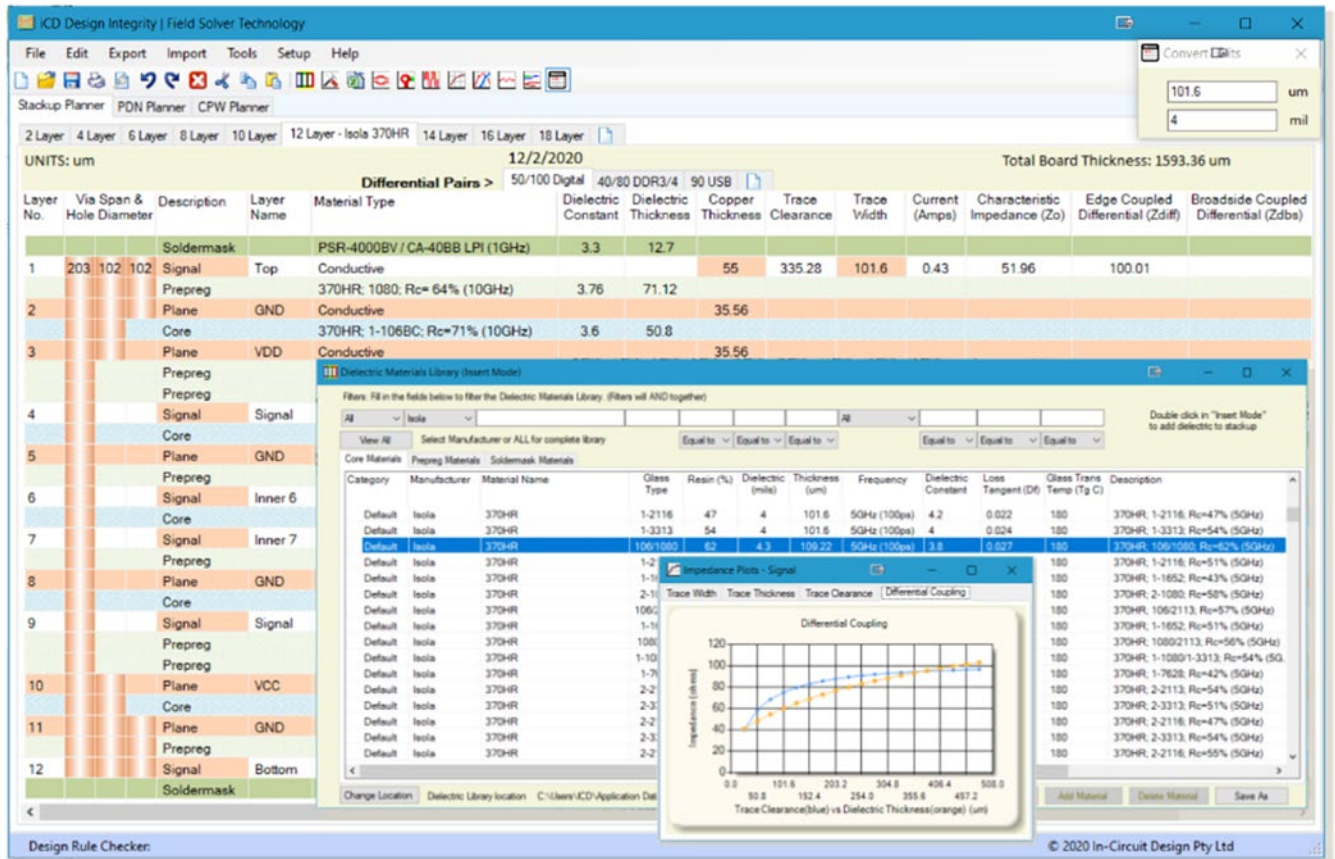


Figure 4: 2D Field Solver used to predict microstrip and stripline impedance (iCD Stackup Planner).

rough number to represent the dielectric constant, dielectric thickness, and the attributes of the trace thickness and width to establish a solution. However, these are not the attributes of the actual materials used by the fabricator to manufacture the board and are inherently inaccurate. There is no point in employing a field solver if your numbers are wrong.

Once the ballpark virtual material numbers are established, the material needs to be selected for the correct frequency of operation. Choosing the materials that are stocked will result in up to 5% better accuracy. Obviously, what you select is based on what is available at a reasonable price. Figure 5 is a graph of the low loss dielectrics stocked by a particular fabricator. One can clearly see which is the best material.

B. Incorporating Multiple Technologies

The iCD Stackup Planner is the first controlled impedance tool to enable field solver

computation of multiple differential pair definitions per layer. This allows you to incorporate differential 50/100 ohm Digital, 40/80 ohm DDR3/4, 90 ohm USB, etc., sharing the same layers (Figure 6). This is important as it is extremely rare to just have a 50-ohm single ended impedance. Usually, many different single-ended and differential impedances have to share layers throughout the substrate. And these variations have to be documented.

C. Seamless Integration to EDA software

For PCB designers, it is also important to be able to transfer the impedance variables and material properties to their EDA tools. Planning the PCB stackup in the early stages of the project reduces unnecessary iterations and optimizes the costs by increasing manufacturability and electrical performance. Far too many designers leave stackup design, which is critical to signal and power integrity, to the

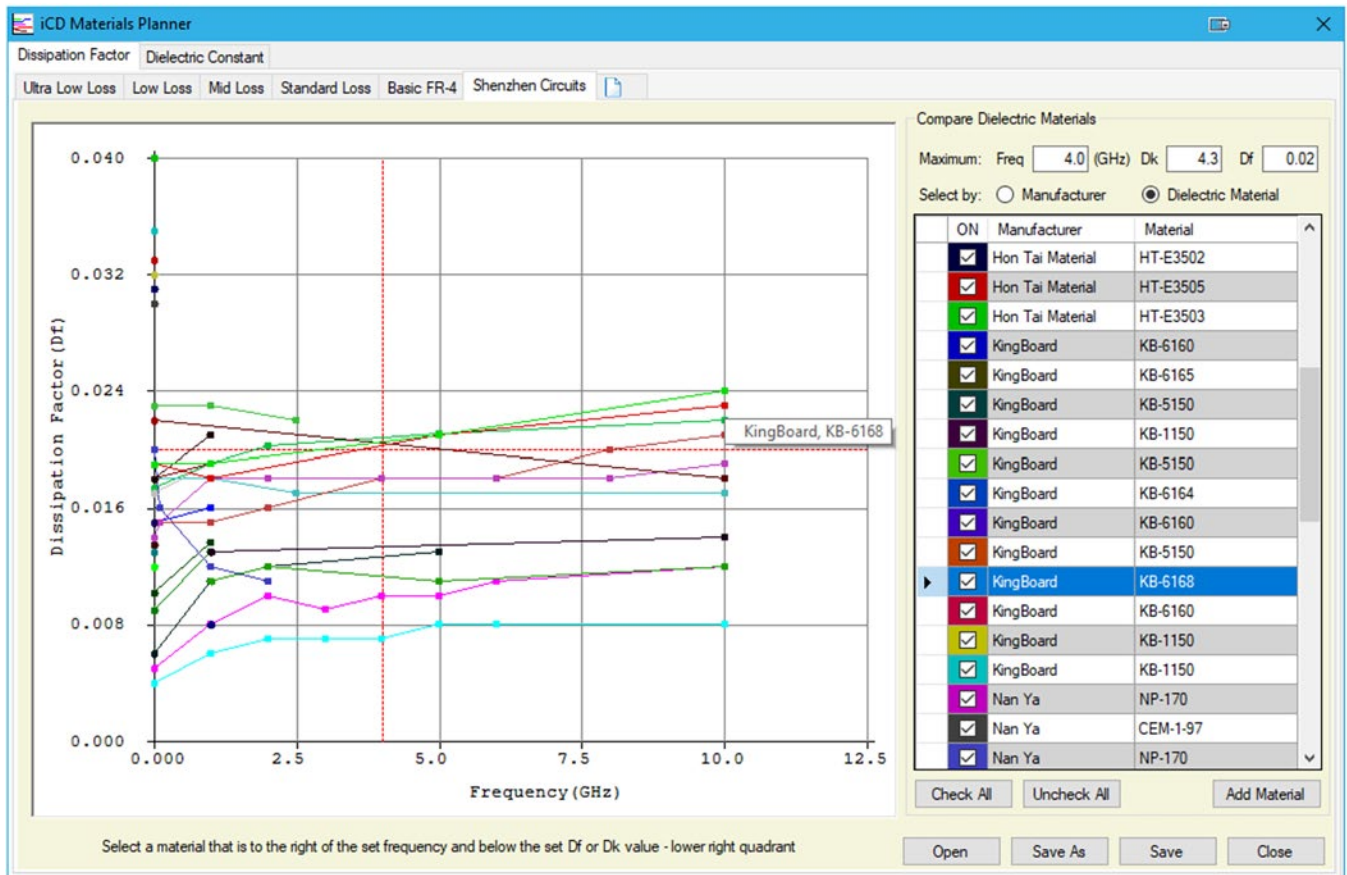


Figure 5: A fabricator's dielectric materials loss profile (iCD Materials Planner).

Differential Pairs >		50/100 Digital	40/80 DDR3	90 USB						
Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)		
PSR-4000 HFX Satin / CA-40 HF LPI...	3.5	0.5								
			2.2	6	4	0.43	51.67	90.63		
			2.2	12	6	0.58	42.53	81.33		
			2.2	12	4	0.43	51.67	98.65		
370HR : 1080 : Rc= 66% (1GHz)	3.97	2.9								
Conductive			1.4							

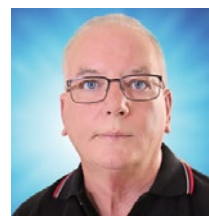
Figure 6: Multiple technologies on the same layer (iCD Stackup Planner).

PCB fabricators. The stackup should be created at the schematic capture stage and flow through the project to CAM deliverables. This avoids expensive design changes at the end of the project.

Stackup planning enables users to quickly explore alternatives in their substrate dimensions and material parameters to quickly assess the impact on performance. The right stackup strategy can reduce crosstalk and suppress EMI, ensuring that the signals will remain stable in the intended environment. **DESIGN007**

References:

1. *Beyond Design* by Barry Olney as referenced in the text.



Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner is a PCB Design Service Bureau and specializes in board-level simulation. The software can be downloaded from www.icd.com.au. To read past columns or contact Olney, [click here](#).

Now, Where Were We?

The Digital Layout

by Kelly Dack, CIT, CID+, PCEA

Introduction

In this month's column, I share a few terms I've been contemplating lately, and which I have been trying to put into context regarding the role of the PCEA within the electronics industry. Then, I hand it off to our PCEA Chairman Stephen Chavez to inspire us for a fresh start in the new year. Finally, I'll provide our readers with a list of events which are coming up.

PCEA Updates

Like me, you may have noticed the use of three concepts used extensively in 2020: "Believe the science and data," "Speak truth to power," and "Consider 'systemic' causes for problems."

Indeed, these concepts were associated with some particularly challenging, if not nasty, dis-

plays of societal failures in 2020. It has been easy for us to see that in an agitated and desperate social climate, the time-consuming, methodical approach to collecting data and applying it to science can give way to convenient conspiracy theory. Speaking truth to power was shown to have the short-term potential to get a person fired overnight. The term systemic was used to point to long term causes for some particularly blatant failures of a society to set people up for success.

Will our society's negative issues be addressed? Will any good come through lessons learned from science, speaking truth to power, and examining systemic causes for our problems? I hope so.

As I begin 2021, these concepts continue to challenge me. And considering these concepts, how can an organization like the PCEA help the electronics industry see positive movement in our industry? I think there is a lot our organization can do to inspire our membership in the long run. Where would our printed





Facing challenges in analyzing system-level electromagnetic effects?

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[READ HOW](#)

circuit engineering technology be without science? Our leaders within the PCEA are actively engaged in partnering and promoting the science and research data of the many electronics PhDs, whose work continues to help PCB designs advance in the areas of layout, materials, processing and overall performance. The goal of the PCEA Educational Committee is to pull industry stakeholders away from conspiracy theories, which can include:

- An EE degree automatically makes one an experienced PCB engineer
- Just because the finishing spec for copper says “2 ounce” your supplier is plating up to a full two ounces.
- Your electronic component app notes are 100% correct for all applications

They want to give our members exposure to the science that can be leveraged to make PCB design, manufacturing, and test and procurement run better. Our educational committee in the PCEA is tasked with teaching our members solid, scientifically sound, core PCB engineering concepts. The concept here is to give our members the education and confidence to speak the truth about design, manufacturing, and test and procurement to fellow stakeholders, project managers, and even CEOs or legal representation during the most agitated and desperate times of a project development cycle.

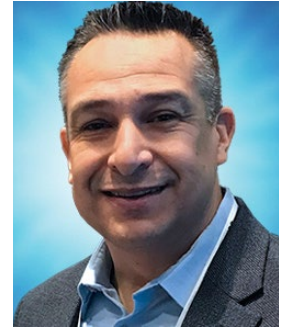
Rejecting radical PCB engineering conspiracy theories, embracing science, and becoming educated enough to speak truth to powerful management and customer contacts are keys to overcoming systemic PCB engineering failure. Systemic success models include proliferation of relevant, real-time data to be accessed and rightly used to promote the well-being of one’s fellow PCB engineering stakeholders and their individual responsibilities. A customer must truly define their needs. A program manager must truly understand those needs, select appropriate project stakeholders, work to gather data, and feed them truth. The PCB design, manufacturing and test engineers must be enabled to work within a company

culture that promotes front-loading projects with a healthy respect for science, data and educated stakeholder feedback.

Message from the Chairman

by Stephen Chavez, MIT, CID+

Happy New Year! 2021 is finally here. Thank goodness that 2020 is behind us! We view 2021 as a new year filled with lots of potential and great opportunities. Most people set resolutions when they start each new year. For many, they consist of



Stephen Chavez

a handful of new resolutions mixed in with some of the same old resolutions. These “carried over” resolutions may or may not get filed or accomplished, yet remain on an annual list, year after year. Personally, I don’t make New Year’s resolutions. I used to make them and write them down. Is this a good or a bad thing to do? I guess it’s up to how each of us perceive this annual form of goal setting or form of “good intentions” to enforce a change or improvement in our respective lives. Everyone handles the beginning of a new year a bit differently when it comes to annual resolutions or goal-setting.

Usually during my year-end holiday break/vacation, I simply take some personal time and do some deep-level self-assessments and evaluations. I think about how the previous year unfolded and how I adapted to it. I review my attained successes, failures, opportunities taken and missed, and opportunities that I simply did not take advantage of. Then, I ask myself several questions such as these:

- “Are you truly happy with who is looking back at you, while looking into a mirror?”
- “Did you do better than the year before?”
- “Did you honestly try your hardest and give your best each and every time?”
- “Did you practice what you preach?”
- “What do you think you could have done better?”

- “Did you learn from any failures or shortcomings?”
- “Did you treat others as you would like to be treated?”
- “Did you live each and every day outside your comfort zone?”
- Finally, here is a big one I started asking myself about 10 years ago: “Did you make a positive difference in someone’s life?”

After this deep self-assessment and self-evaluation, I identify areas to improve and ways to evolve. Then I go after it, continually telling myself, “Steph, you can do better, so much better! There is always room for improvements! Attack each day as if it’s your last and have no regrets as this year unfolds! Positive attitude is everything, even when things don’t go as planned or as expected! Remember Steph, don’t be afraid to fail, because being afraid in itself will cause a self-induced mental roadblock to success.”

For PCEA, 2020 was our birth year, a year we will never forget, for many reasons. It was a year that unfolded with lots of challenges, especially with adapting, evolving into and incorporating our virtual existence in today’s industry, due to COVID-19. Like many, PCEA adapted and overcame these challenges with much success. As we continue our positive momentum and successes in 2021, we take time to look back and review how PCEA came about, where we started, where we want to be and what it’s going to take to get there, and how we will make it happen.

It’s similar to my yearly self-assessment, which has been very instructive for me. As a collective, we all agree that we’ll continue striving to be and do better in all aspects of what PCEA stands for. Collaborate, inspire, and educate are at the core of our values and mission. For the good of the industry, PCEA will be even better at this in 2021. This is a year that we eagerly attack and do so much more, from years of lessons learned and feedback from many within our industry. So, are these a form of New Year’s resolutions? Are these goals? I’ll let you decide. I personally

challenge you to do your own self-assessment going into 2021. I also challenge you all to stay outside your comfort zone for personal growth and do whatever it takes to be and do better, as each of you chase your own definition of success.

I continue to wish each of you and your families health and safety. Best of success to all as 2021 unfolds.

Warmest regards,
—Steph

Next Month

Just as it looked as though some new live printed circuit engineering events would be opening up—not so fast; 2021 will require from all of us an ounce of prevention in order to pound out the cure for new electronics jobs and technology. Help is on the way! PCEA is traveling at warp speed to feed our diverse electronics industry data in hopes this may lead us to mutate our thought process or at least provide us with antibodies to help ward off career stagnation.

Upcoming Events

Below is a list of upcoming event cultures which may lead you to mutate your thought process or at least provide you with antibodies to help you ward off career stagnation.

- March 6–11: **IPC APEX EXPO** (virtual)
- April 13–15, 2021: **DesignCon** (Santa Clara, California)
- May 10–12, 2021: **PCB East** (Santa Clara, California)
- May 11–13, 2021: **IPC High-Reliability Forum 2021** (Baltimore, Maryland)
- August 31–September 3, 2021: **PCB West** (Santa Clara, California)
- November 10, 2021: **PCB Carolina** (Raleigh, North Carolina)

Spread the word. If you have a significant electronics industry event that you would like to announce, please send me the details at kelly.dack.pcea@gmail.com, and we will consider adding it to the list.

Refer to our [column](#) and the PCEA website to stay up to date with the scheduled industry events. If you have not yet joined the PCEA collective, please visit us at pce-a.org and find out how to become a PCEA member.

Conclusion

The most productive, long term changes within a society do not come through negative agitation but through education, science, and truth. In our PCB engineering culture, we are occasionally affected by “disruptive technology.” Though sadly, disruptive technology can wipe out an entire industry—think of what troubles the LED caused to the incandescent light bulb industry. We might consider this an example of technologists inciting “good trouble”—a significant change in technology based upon the long-term benefit of the entire

society considered. Long-term benefits for all.

The PCEA doesn’t want to help educate our industry stakeholders so we can all speak truth to power and get fired the next day by management or customers who can’t handle the truth. Our organizational goal involves collaborating to help create and inspire an entire industry of informed people who have their industry’s long term best interests and success for all in mind.

See you next month or sooner! **DESIGN007**



Kelly Dack, CIT, CID+, is the communication officer for the Printed Circuit Engineering Association (PCEA). To read past columns or contact Dack, [click here](#).

Qualcomm, Great Wall Motor Work to Deliver Premium Smart Mobility Experiences

Qualcomm Technologies, Inc. and Great Wall Motor Company Limited (GWM) have announced the companies’ working relationship in autonomous driving, under which GWM will use the Qualcomm Snapdragon Ride Platform to build its advanced intelligent driving system of high computing power—GWM “Coffee Intelligence” system—and adopt the system in its premium production vehicles starting in 2022.

The Snapdragon Ride Platform, one of the automotive industry’s most advanced, scalable and open automated driving solutions, aims to address the complexity of autonomous driving (AD) and Advanced Driver Assistance

System (ADAS) use cases across industry segments by leveraging its high-performance, power-efficient hardware, industry-leading artificial intelligence (AI) technologies and pioneering autonomous driving stack to deliver a comprehensive, cost and energy efficient systems solution for multiple classes of vehicles.

“GWM and Qualcomm Technologies have deep and longstanding relationship across many technology areas. The Snapdragon Ride Platform brings forth Qualcomm Technologies’ deep expertise in computing, AI, connectivity and security, and is designed for demanding automotive safety,” said Lei Xian, vice president of sales and business development, Qualcomm International (Shanghai) Co., Ltd.

“Data explosion in the era of AI has driven a huge demand for data processing throughput and computing power. Thanks to the high computing capabilities and scalability of the Snapdragon Ride Platform, GWM will be able to offer comprehensive multi-segment capabilities in our future vehicles, from driver assistance system to high-level autonomous driving,” said Kai Zhang, head of Intelligent Driving for Great Wall Motor.

(Source: Qualcomm Technologies)





PCB007 Highlights



Dr. John Mitchell on IPC APEX EXPO Going Virtual ►

On Monday, December 14, 2020, Barry Matities and Dr. John Mitchell, IPC president and CEO, discussed the decision to move IPC APEX EXPO to an all-virtual platform. In this interview, Dr. Mitchell confirms that IPC is committed to delivering a cutting-edge experience, including a strong technical program, exhibitor and visitor support, multiple keynotes and a wide variety of online networking events. Matities and Mitchell also analyze the challenges for IPC in hosting the show, as well as some of the unique opportunities that a virtual show presents for IPC and attendee alike.

EPTE Newsletter: The Printed Circuit Industry in China ►

Market data provided by the Taiwan Printed Circuit Association (TPCA) is very comprehensive. Unfortunately, any news or data from the PCB industry in China is not easily accessible. Dominique Numakura provides an update on the printed circuit industry in China based on available market data.

Rogers Corporation Appoints Megan Faust, Keith Larson to Board of Directors ►

Rogers Corporation has announced that its Board of Directors appointed Megan Faust and Keith Larson to serve as members of the Company's Board.

ECWC15 Virtual Conference Keynote: 5G PCB Technology and Material Challenges ►

The second day of the Electronic Circuits World Convention began with a keynote from Dr. Shih-Kao Chiang, managing partner of Prismark, describing the PCB technology and

material challenges presented by the introduction of the fifth-generation cellular wireless communication network—the roll-out of which was continuing despite the coronavirus pandemic. Technical Editor Pete Starkey has more.

Batteries and Data Centers ►

The I-Connect007 team met with electrical engineer Mike Mosman, who has spent the majority of his career designing some of the country's largest data centers. Mike recently sold his engineering company CCG Facilities Integration; he is now the vice president of electrical engineering in mission-critical facilities for Morrison Hershfield, and is still designing leading-edge data centers for large internet companies. In this discussion, Mike explains how evolving battery technology and a strong demand are playing a key role in this area and others.

Standard of Excellence: Going Public with Your Partner ►

One aspect of a great partnership with your vendors is to show the world how you are working together. Demonstrating how a great partnership can serve both your companies well and is beneficial to your industry too. Anaya Vardya shares nine ways to go public with your partner.

Pacothane on the Future of Laminate Technologies ►

Nolan Johnson recently spoke with the Pacothane Technologies team about the current drivers of circuit board technology and how that has influenced and increased their product development of lamination and lamination assist products.

Six Design Tips to **Avoid** Part Fit Problems

Connect the Dots

by Bob Tise and Matt Stevenson, TEAM SUNSTONE CIRCUITS

“Will my parts fit on the board?” That seems like it should be a rhetorical question that needs no answer, but reality tells us, as you transition from the design stage to manufacturing, issues with parts fit are one of the most frequent causes of delays and cost overruns.

We see it every day. Designs are submitted that can’t or shouldn’t be manufactured because the parts will not fit properly. This creates issues with performance and durability—effectively reducing the overall quality of the board.

Following are six methods that will help you avoid common, parts-related manufacturability pitfalls.

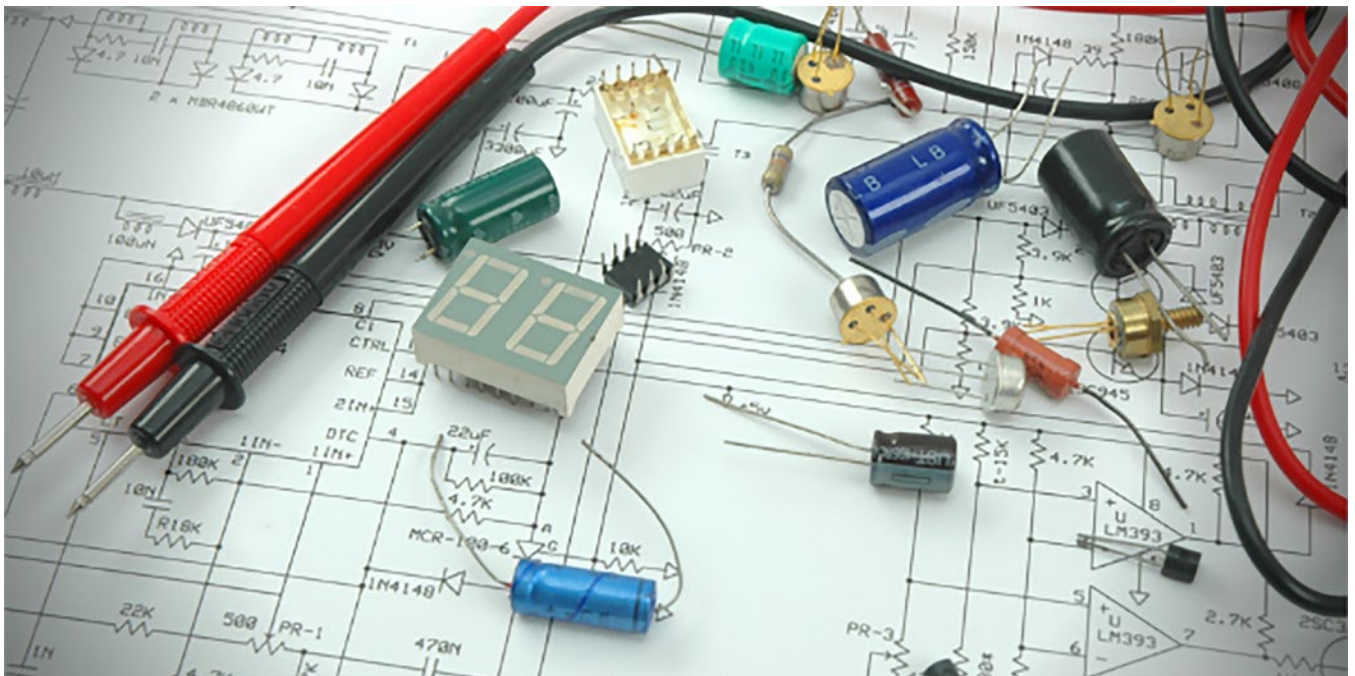
1. Avoid pinhole pitfalls.

It’s important to check component physical dimensions. Height is an often-overlooked por-

tion and can create issues at or after assembly. Take dimensional tolerances into consideration and account for variation that can impact fit. Through-hole pins can be the wrong size or have the wrong spacing, and components can actually be much larger than their footprint or land pattern might indicate. Surface mount parts take the pin diameter and tolerance out of the equation, making them easier to verify. It is far easier to take the time up front and be right than to have to re-spin a design or try to find an alternate part that fits your board.

2. What to do when the land pattern and pin size differ.

One of the most frustrating mistakes with through-hole parts is when the land pattern matches, but the pin size is too large to fit reliably.



Integrated Tools to Process PCB Designs into Physical PCBs



Visualize

Use manufacturing data to generate a 3D facsimile of the finished product.



Verify

Ensure that manufacturing data is accurate for PCB construction.



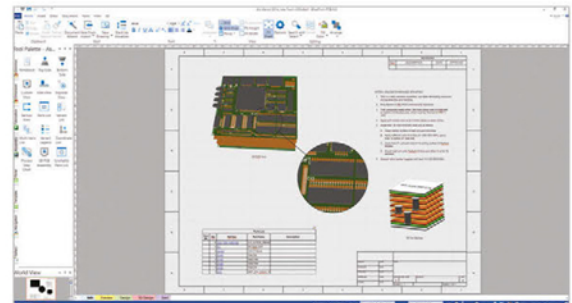
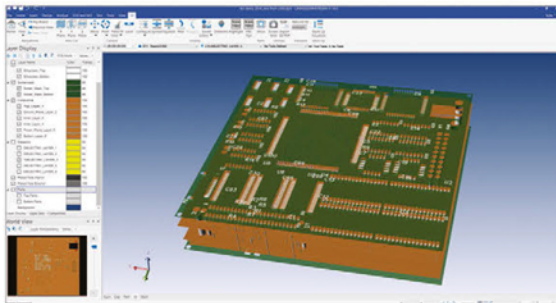
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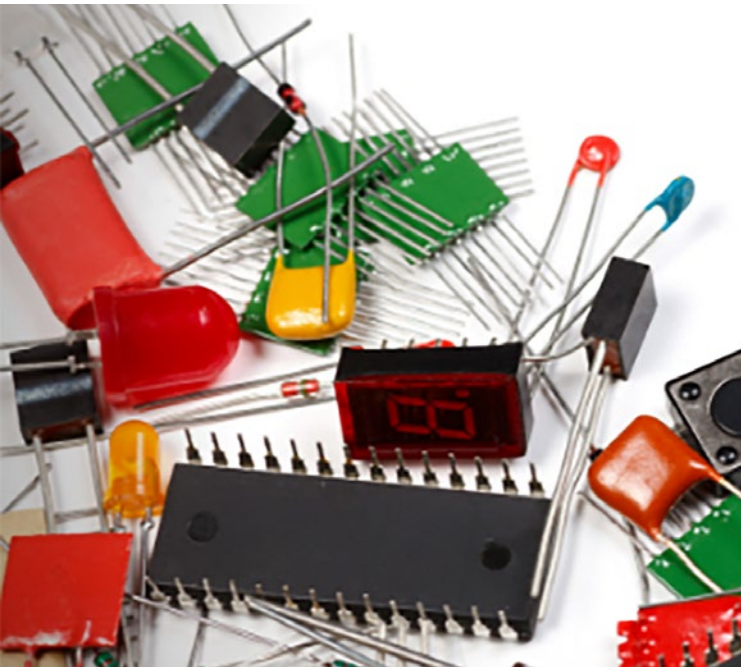
DownStream Technologies, offers an integrated manufacturing data preparation solution for PCB post processing including manufacturing data visualization, stack-up definition, PCB panel visualization and support for 3D PCB documentation. This environment allows PCB designers and engineers to visualize, verify and document a printed circuit board before manufacturing.



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If hole sizes are too tight, pins may not fit into the holes, pins bend during insertion, or they go into the holes but may not solder well. Proper through-hole soldering requires solder to flow up through the gap between the pin and the hole barrel. If there is not enough space to allow enough solder mass to flow up through the hole, a cold solder joint can result and premature failure of your circuit is likely to occur.

To avoid this issue, make sure that when designing, you know the pin size and tolerance range for your components. Component holes should be sized correctly to allow between 12 and 16 mils diameter larger than the component pin at maximum material condition (MMC) when possible.

MMC is the condition in which the hole is drilled at the low end of the tolerance range, and the pin measures at the high end of the tolerance range. Pin locations should be placed at nominal location or the basic dimension shown on the datasheet.

3. Data sheets can disagree with CAD software.

Third-party CAD libraries can contain millions of different parts, so it should not come as a surprise that a few bad apples lurk among them. When the data sheet and the library part

don't match up, your project is dead before you make the first connection. Always check any library part for accuracy before you use it the first time.

The data sheet for a part usually tells the real story, and it's usually just a few lines that provide you with the information you need to make the crucial decisions about sizing. It's important to read and comprehend the data sheets so problems in CAD don't lead to the wrong sizing and spacing on the PCB.

4. Pay attention to pinouts when using alternate vendor parts.

Even if you've paid attention to pin size and through-hole size, and you've made sure your solder joints are good, a part can still not work as expected. Similar parts with the same footprint might look like they should act identically, but they won't always have the same pinout. Sure, each transistor has a gate, drain and source, but different manufacturers can differ in what goes where.

A Motorola part can differ from a Texas Instruments (TI) part, and if you're just buying generics, all bets are off. The same basic component will come in multiple packages. Sometimes the variations are tossed into the back of a data sheet as an afterthought, but these can be critical. Similarly named packages can even come in different widths.

5. Be aware of mechanical fit.

It's not just the footprint and through-holes that you need to pay attention to. The physical size of your component body can keep parts from fitting into designated spaces. Again, MMC is the rule, and with maximum component body size, paying close attention to the tolerance range is critical.

As parts get larger, or you start sourcing your parts from multiple vendors, your footprint size may need to expand considerably to accommodate all the dimension and tolerance variables. When combining multiple part body dimensions, always take the largest dimension, or you could end up trying to violate the Pauli exclusion principle, which states that two identical fer-

mions (particles with half-integer spin) cannot occupy the same quantum state simultaneously. In short, you are going to smash something.

6. Data sheets are helpful, but not a replacement for experience.

When it comes down to it, the data sheet is considered king, but that doesn't mean you shouldn't question it when necessary. Many problems with fit can be unintuitive or difficult to diagnose, so understanding size requirements will prevent a lot of headaches. Every dimension needs to be looked at, from pin and through-hole size, to capacitor height.

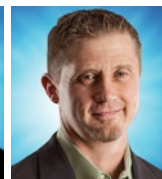
Frequently these issues will crop up when replacement components are used. Watch those

tolerance ranges carefully. When you are evaluating replacements, make sure your replacement parts fall between maximum and minimum measurements stated in your original part data sheet. You could get away with parts that are smaller in some regards, but this should be carefully evaluated. And don't forget to pay attention to pinouts and alternate packages. **DESIGN007**

Bob Tise is an engineer and **Matt Stevenson** is the VP of sales and marketing at Sunstone Circuits. To read past columns or contact Tise and Stevenson, [click here](#).



Bob Tise



Matt Stevenson

Light-Carrying Chips Advance Machine Learning

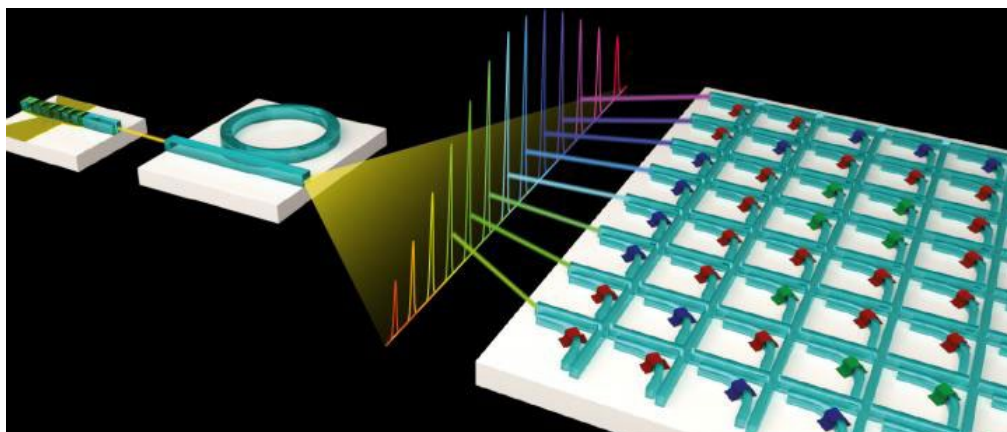
In the digital age, data traffic is growing at an exponential rate. The demands on computing power for applications in artificial intelligence such as pattern and speech recognition in particular, or for self-driving vehicles, often exceeds the capacities of conventional computer processors. Working together with an international team, researchers at the University of Münster are developing new approaches and process architectures which can cope with these tasks extremely efficiently. They have now shown that so-called photonic processors, with which data is processed by means of light, can process information much more rapidly and in parallel - something electronic chips are incapable of doing. The results have been published in the journal "Nature."

Light-based processors for speeding up tasks in the field of machine learning enable complex mathematical tasks to be processed at enormously fast speeds (10^{12} - 10^{15} operations per second). Conventional chips such as graphic cards or specialized hardware like Google's TPU (Tensor Processing Unit) are based on electronic data transfer and are much slower. The team of researchers led by Prof. Wolfram Pernice from

the Institute of Physics and the Center for Soft Nanoscience at the University of Münster implemented a hardware accelerator for so-called matrix multiplications, which represent the main processing load in the computation of neural networks. Neural networks are a series of algorithms which simulate the human brain. This is helpful, for example, for classifying objects in images and for speech recognition.

In the experiment the physicists used a so-called convolutional neural network for the recognition of handwritten numbers. These networks are a concept in the field of machine learning inspired by biological processes. They are used primarily in the processing of image or audio data, as they currently achieve the highest accuracies of classification. The results have a wide range of applications.

(Source: University of Münster)



2021 Updates to IPC Design

Design Circuit

by Patrick Crawford, IPC—ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES

A year of COVID-19 has taught the world how to operate more efficiently in the virtual amphitheater, and IPC is no different. While standards development meetings have historically occurred via teleconference, and most internal IPC business is conducted remotely, our larger programs—training and educational activities, full-day development meetings, hand-soldering competitions, etc.—have always relied on face-to-face collaboration. In the case of IPC Design, which debuted only weeks before lockdowns commenced around the world, it became clear that the initial model would not provide affiliate members with the promised experience. The drawing board was dusted off—although it didn't have too much time to collect dust—and a newer, sleeker model was devised.

Before explaining what has changed, it's important to detail what hasn't changed. The key goals of IPC Design have always been to

facilitate the professional development of its affiliate members, to enable professional networking among its affiliate members, to provide liaison between the professional printed board designers (and electronics manufacturing experts, in general) and academia, and to generally advance the art and science of printed board design engineering. It is still free to join and will always be free.

As for the changes, in short, IPC Design is now easier to join than ever. By migrating the community to Discord—a popular, free-to-use, multi-platform community building tool—many of the steps to affiliate have been eliminated, and the time-to-join has been reduced to 10 minutes (or less). There are no more forms to sign or bylaws to understand. The affiliation form can be found on the new [IPC.org](https://www.ipc.org) ^[1], which has recently been updated to offer a better experience to users—both IPC members and visitors alike.



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Once you've signed up, you will receive a reply from IPC within two business days that includes instructions on how to join Discord.

By migrating to Discord, we have also formally eliminated the Chapter model, and coalesced all the previous affiliation types into one, unified affiliate. Discord is a server-based utility, and in general, "server" and "group" can be considered synonymous for the remainder of this column. As an affiliate, you can belong to as many servers as you would like, and you can request to create a server for your local design community, special interest group, project, or any other activity.

**Once you've signed up,
you will receive a reply from
IPC within two business days
that includes instructions
on how to join Discord.**

Upon signing up, you can choose which server you would like to belong to as an active affiliate, with the ability to use the chat and video features at will, as well as upload and download files. You will also be automatically enrolled in the global community as an affiliate with full permissions. (Currently, the global server will operate in English; however, Discord does offer built-in translation for its UI, and most browsers support translation of text within the Discord chat itself.)

One exciting aspect of the new Discord-based model is that any affiliate can join any other region's server at will, allowing them to access materials and conversations therein (albeit in that server's language). We are experimenting with enabling observer permissions for all affiliates in all servers, so that you can keep tabs on what activities are occurring around the world.

As of now, there are a few designers who have acted as pilots for the various IPC Design iterations, and I extend my thanks to those

few. At this point, we are opening the floodgates for the new future of IPC Design, and I welcome all to come and give it a try.

The benefits of joining IPC Design are simple: By accessing a network of global design engineers (for free), you unlock hundreds of years' worth of design engineering experience with whom to ask questions, disposition new ideas, forge new business relationships, and unlock new perspectives. By integrating IPC Design with the IPC Education Foundation, we will also be enabling established engineers to seek out new talent in the industry for mentorship, internship, or employment.

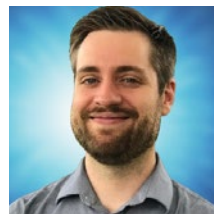
There are also no obligations, yearly meeting quota or dues to be paid, and there is no implicit promise of resource or time expenditure on your end.

IPC is dedicated to helping the industry build electronics better, and industry members associated with IPC Design have already been asked by IPC to provide input on new educational courses, participate in brainstorming sessions for upcoming design competitions (yes, this idea is not dead—there will be a board design competition in 2021), and provide feedback on which IPC standards should be translated into new languages. So, while you have no obligations, we hope to leverage your experience in design beyond what is available in standards development meetings alone.

I urge you to stop by and take a look. As the program grows, there will be even more members available with whom you can create a community. The new IPC Design is sleeker, more lightweight, and more accessible than ever—just another way that IPC strives to help you make your life easier and your designs better. **DESIGN007**

Resources

1. Find the affiliation form at ipc.org/affiliate-ipc-design.



Patrick Crawford is the manager of design programs and related industry programs at IPC. To read past columns or contact him, [click here](#) or email PatrickCrawford@ipc.org.



MilAero007 Highlights



Use of IMS Thermal Materials in Multilayer Stackups for Power Applications ►

This roundtable discussion brings together the expertise of Ventec International Group's Global Head of IMS Technology Chris Hanson and Technical Manager Denis McCarthy. Rax Ribadia of Excello Circuits provides hands-on fabrication experience from a specialist PCB manufacturer, and I-Connect007 editors Andy Shaughnessy and Pete Starkey contribute to a conversation that explores applications, materials, design considerations, and mechanisms of heat transfer.

The Government Circuit: Looking Ahead to 2021 ►

Before the 116th Congress adjourned for the holidays, IPC expected to secure some policy victories for the electronics manufacturing industry and keep its policy agenda moving forward. Read on—and watch this space—to learn how it all turns out.

2021 Symposium on Counterfeit Parts and Materials: Call for Abstracts ►

The Surface Mount Technology Association (SMTA) and CALCE University of Maryland are inviting the industry to submit technical papers for presentation at a virtual 2021 Symposium on Counterfeit Parts and Materials. The event is scheduled August 3–5, 2021.

Defense Speak Interpreted: What's a VITA? ►

Ever wonder how military electronics users could swap out circuit cards rapidly and keep their defense systems running? What about a “hot swap” of a circuit card that was questionable. The DoD has helped private industry develop a highly sophisticated set of standards for circuit card input/output (I/O) to make quick change possible.

Understanding MIL-PRF-31032, Part 6 ►

Concluding this six-part discussion on understanding the military printed circuit board performance standard MIL-PRF-31032, Anaya Vardya covers the remaining procedure required to address the unique requirements of the military.

Stephen Chavez and Happy Holden on Designing Reliable Vias ►

Andy Shaughnessy and Happy Holden speak with Stephen Chavez, a staff engineer with an aerospace company and chairman of the Printed Circuit Engineering Association (PCEA), about designing vias for greater reliability. They also address several areas where they can look to improve reliability, a variety of steps that designers should take to help ensure more robust vias, and some testing and educational resources that PCB designers and design engineers should be aware of.

U.S. Congress Approves Funds for R&D on Lead-Free Electronics in Aerospace, Defense and High-Performance Applications ►

On Monday December 21, 2020 the U.S. Congress approved \$10 million for research into the issues surrounding lead-free electronics in mission-critical applications. IPC and its allies had called for these funds to be included in the Fiscal 2021 defense appropriations bill.

Raytheon and United Technologies Merger: Stronger Together ►

The 2020 merger of Raytheon Company and the United Technologies Corporation aerospace businesses brought together two companies with distinctive legacies of developing and deploying advanced technologies to solve some of the world's most pressing and complex challenges.

Demystify Flexible Stackups

Flex Talk

Feature Column by Tara Dunn, AVERATEK

The sheer number of flexible laminate materials and constructions can be a bit daunting for those new to flex and rigid-flex design. I sat down with Jeff Martin from Omni PCB for his insight into flexible laminates and his advice when working on a flex stackup.

Tara Dunn: Hi, Jeff, thank you for taking time to speak with me today. Before we dive into today's topic, can you give a brief introduction to what you are doing now and what your background is with flex and rigid-flex?

Jeff Martin: Hi, Tara. I am currently the chief technology officer for Omni PCB. I provide our customers with a high level of negotiation and

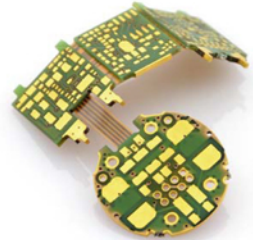
project management support, technical consulting, and industry insight. I have been in the printed circuit board industry for 25-plus years. A number of those years were working as a front-end engineer and project manager for flex and rigid-flex manufacturing.

Dunn: That is a long history with flex materials. For the many people who are new to designing with flexible materials, can you give us a basic understanding of flexible laminates?

Martin: Absolutely. Flexible laminates come in a variety of materials. Probably the most used and what people typically think of when starting to design a flexible circuit is polyimide



Focused on Flex

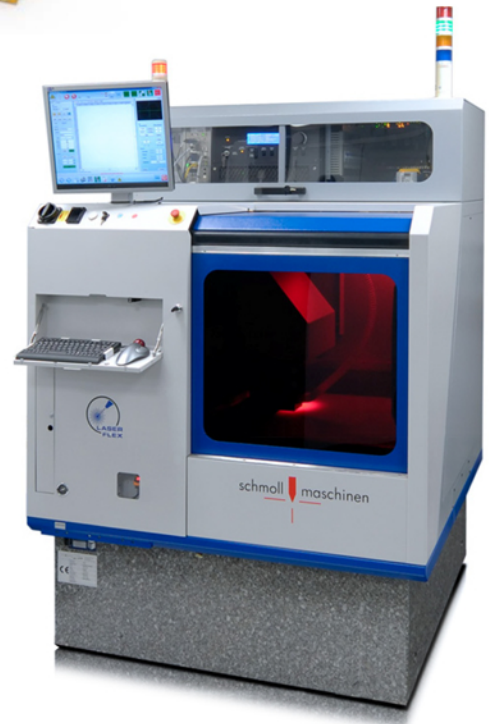


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dielectric. Breaking that down, the laminate will consist of a layer of rolled-annealed copper bonded to the polyimide and this is done in two different ways. Adhesive-based cores are made up of a polyimide core, a layer of adhesive and a layer of copper which is bonded together using heat and pressure. The adhesive commonly used is either epoxy or acrylic. A typical adhesive thickness is one-half to 1 mil. Adhesiveless based cores have the copper directly attached to the polyimide core without the use of any adhesives. Adhesiveless cores are typically recommended for applications that have a thickness constraint and also when working with rigid-flex constructions.

Dunn: If the adhesive thickness is one-half to 1 mil, what thicknesses are available for the copper and polyimide?

Martin: Although you can likely get nearly any combination of dielectric and copper thickness, the laminates will typically have some combination of half-ounce to 2-ounce copper, with anywhere from half-mil to 5-mil polyimide. When you factor in options for adhesiveless construction or adhesive-based, with or without flame retardant formulations, there is a wide variety to select from.

Dunn: I imagine that can be overwhelming for those new to flex design and trying to select the best materials. Are there certain materials that are more common than others and likely to be in stock with a fabricator?

Martin: This one is a little difficult to answer because it really does vary from fabricator to fabricator, but in general constructions using half-ounce and 1-ounce copper and 1 and 2 mils of adhesive are probably the most stocked materials. If a fabricator builds a lot of rigid-flex, they may be more likely to stock adhesiveless materials. It is risky to assume that



Jeff Martin

materials may be in stock, so working with your fabricator as you are creating the stackup to understand what is in stock is very beneficial. If you are able to use materials in stock, that can greatly reduce your lead time and if you identify early in the process that there is a material that does need to be ordered, that material can be pre-ordered while the design is being completed.

Dunn: I agree, working with your fabricator early in the design is always a good idea. Flexible circuit stackups also need to include any polyimide or FR-4 stiffeners that are being used. Can you explain the function of each?

Martin: Sure. Stiffeners are used to create a support area where the flex will not bend and will support components and connectors. An unclad piece of FR-4 is a common solution. Another common type of stiffener is polyimide. This, too, can add support to component areas and is also often used to build up the termination area with ZIF terminations, thickening that specific area without increasing the overall thickness of the flex.

Dunn: We have been speaking primarily about flexible circuits, what are the key things to keep in mind regarding materials and stackups for rigid-flex designs?

Martin: First, as I mentioned earlier, check with your board manufacturer to see what material they stock. This will help when you are considering your stackup. With rigid-flex it is very important to keep acrylic adhesive outside of any rigid area that will have plated through-holes. So, selecting adhesiveless flex materials, and using bikini cut with the coverlays is highly recommended. From there, keep in mind the form, fit and function of the circuit. How will it mount? Where will it flex? How often does it flex? What will it plug into? And so on.

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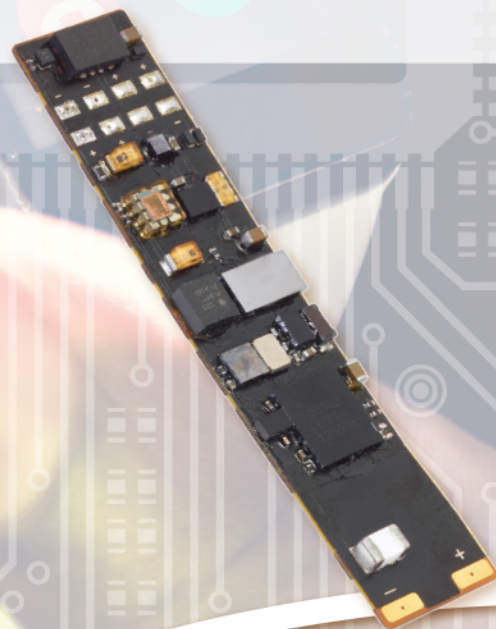
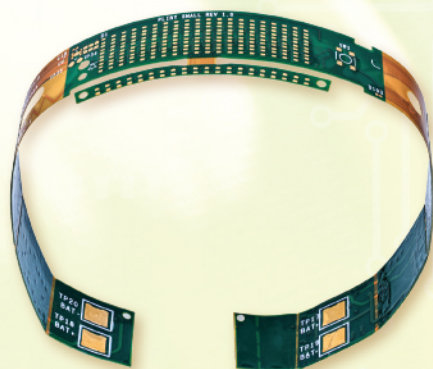
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Dunn: I often share my experiences with the “flex that didn’t flex.” Do you have any flex war stories and lessons learned you would like to share?

Martin: I honestly do not have a recollection of one.

Dunn: Wow, that is a great track record after working with flex and rigid-flex for 25 years. As we wrap up, please share your best advice regarding flexible circuit stackups.

Martin: As I have mentioned a few times, I think my best advice to people new to flexible materials, or even those experienced flex designers, is to get in touch with your board house early in the process. Find out what materials

they stock, all the way down to the adhesives they stock, and work with them to dial in the stackup. They are the experts and that simple step can prevent a lot of headaches later in the design.

Dunn: Great advice. I couldn’t agree more. Thanks, Jeff, it has been great talking with you today and I am sure this will be informative for designers just getting started with flexible materials. **DESIGN007**



Tara Dunn is the vice president of marketing and business development for Averatek. To read past columns or contact Dunn, [click here](#).

Exro Validates Intelligent Battery Technology for Second Life Applications

Exro Technologies Inc., a leading clean technology company which has developed a new class of power electronics for electric motors and batteries, is pleased to announce that it has completed the technology validation on its Battery Control System (BCS), formerly known as the intelligent battery management system.

The BCS can expand the capabilities of batteries by enabling a greater depth of control on the cells. The cells

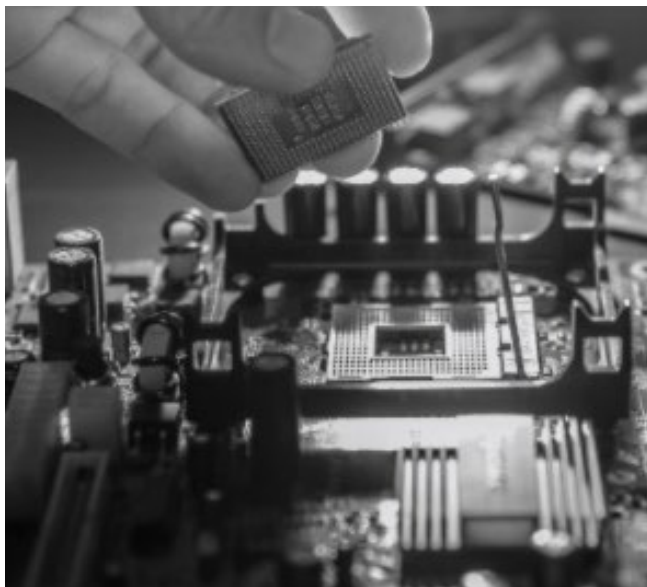
remaining in a battery at the end of first life can be optimized to rejuvenate the same battery into a new second life. Exro can establish a greater depth of control on battery cells because the same principles that govern coil groupings in electric motors can also apply to managing cells in a battery.

As more electric vehicle batteries reach end of first life, there is a growing number of batteries that can be utilized for second life energy storage. The BCS can help Exro to lead the rapidly accelerating energy storage markets. Second life energy storage is a dynamic growth market with CAGR projections of 23.1% through 2030.

Simulations in the lab have demonstrated the principles required for optimized second life operations. The system is able to regulate grid current, charge and discharge at cell level, and manage cells with different states of charge. Exro will move forward to demonstrating the Battery Control System in operating applications in 2021.

“Now it’s just about scaling this up”, said Eric Hustedt, Chief Engineer of Exro. “We’ve confirmed the operational principles with our simulations and are very excited about the potential for this system in new environments.”

[Source: PRNewswire]





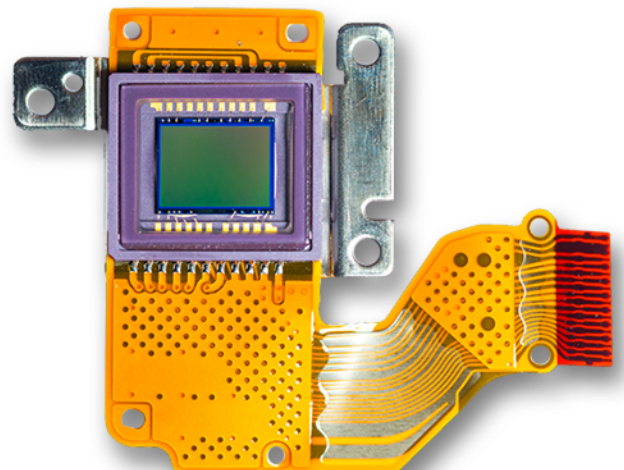
Online Training Workshop Series:

Flexible Circuit Technology

with Joe Fjelstad

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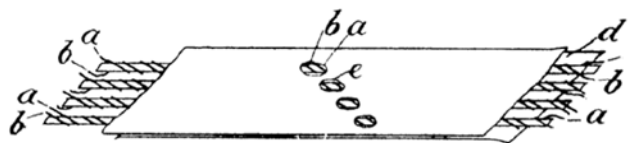
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Flexible Circuits Versus Flexible Hybrid Electronics—Where's the Line?

Flexible Thinking

by Joe Fjelstad, VERDANT ELECTRONICS

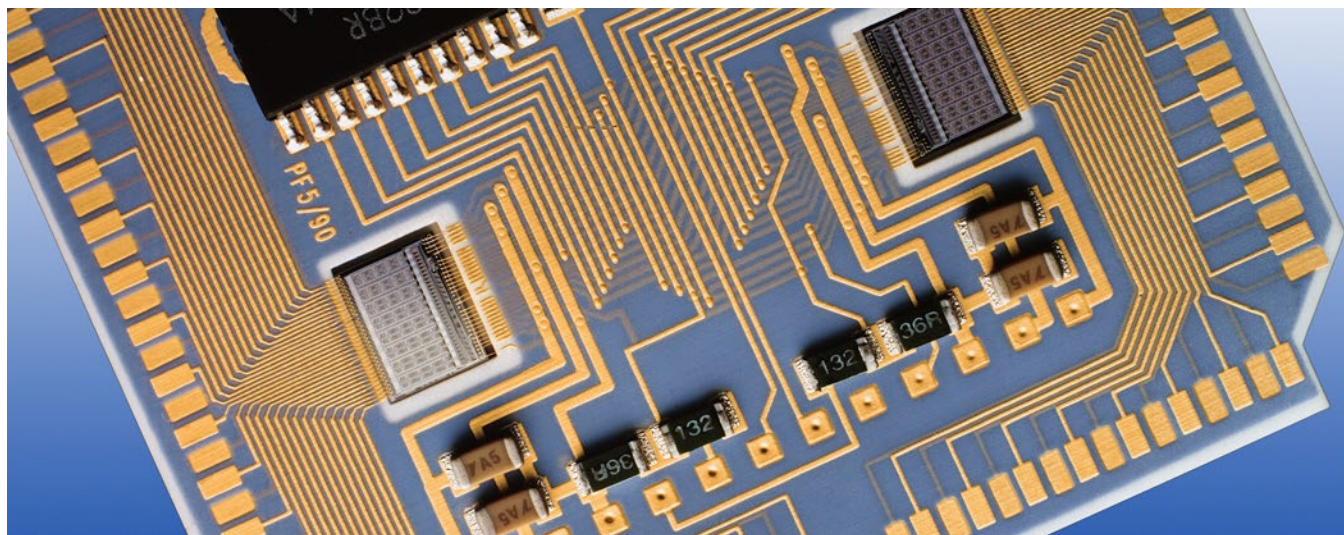
The basic idea of a flexible circuit is arguably more than a century old, based on the interpretation of a 1903 patent by Albert Hanson, which circuit industry maven and historian Dr. Ken Gilleo found in his research on industry origins some years back. Fundamentally, it was an ordered pattern of wires on a wax paper-like insulator. This is still a suitable definition to this day.

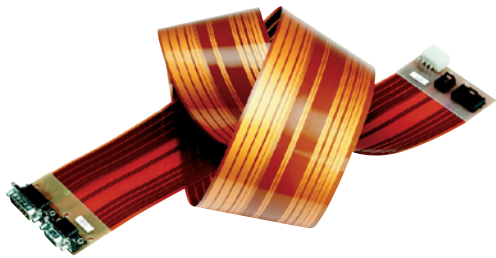


However, today's flex circuit technology is many orders of magnitude beyond its humble beginnings in ways likely far beyond the imaginings of Hansen in his day. Moreover, the materials and processes used to produce flexible circuits have been on a steady evolution-

ary path with advances coming routinely. Not all the advances are ground-breaking but each one adds to the designer's tool chest to create the product needed to solve a general problem or particular issue.

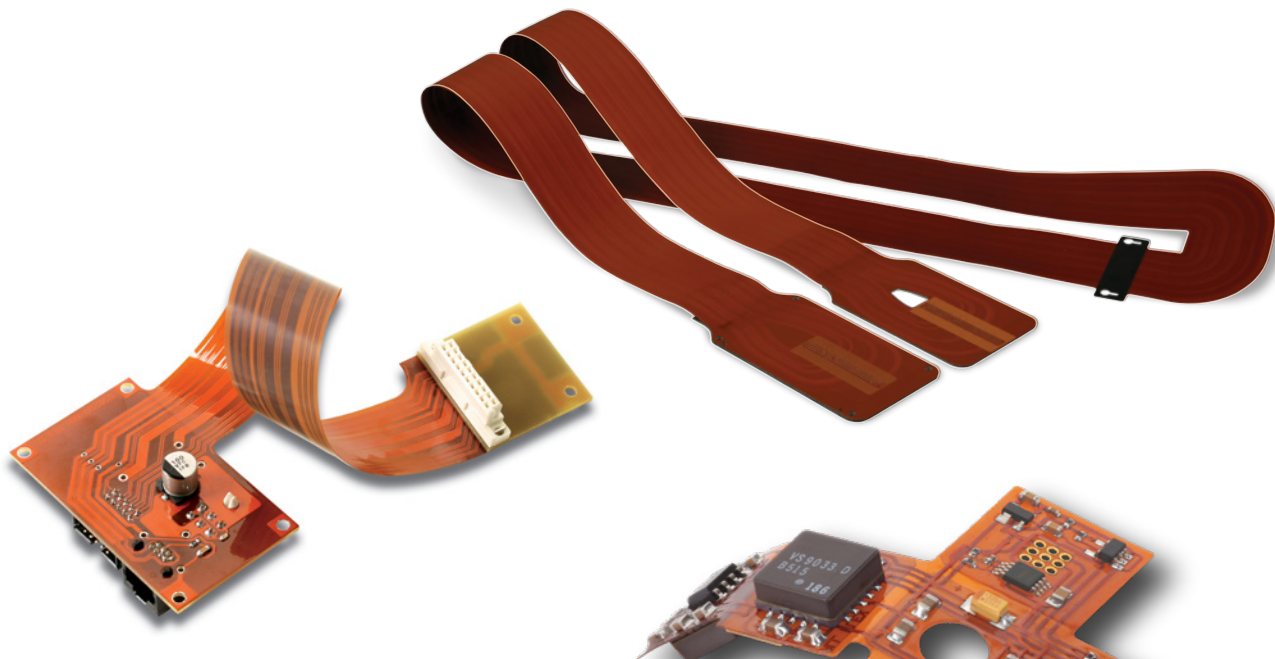
The term flexible circuit is the fundamental and most universally accepted term for the class of products that meet the simple description. Flexible circuits can be simple one-metal-layer devices to replace discrete wire assemblies, or complex multilayer or rigid-flex assemblies that are often populated with all manner of electronic components, both through-hole and surface mounted normally using solder. The most common materials used are copper for conductors, which are commonly etched from a thin copper foil, and either polyimide or polyester for the flexible base material to which the copper foil is bonded. In most cases flexible circuits are designed to conform to the surfaces of the housing in which they



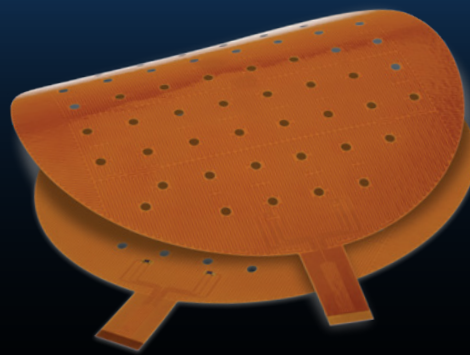


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are contained. Dynamic flexing is required in a relatively small percentage of applications; however, it is important that the designer be familiar with dynamic flexing guidelines as naturally occurring vibrations encountered in use can result in flexing-related failures if their frequency and amplitude are sufficiently high.

That covers in broad brush strokes what a typical flexible circuit is, so what then is a flex hybrid electronic assembly or FHE? The term “flex hybrid electronic” is a relatively new term that has been coined to rebrand a lower-cost type of flexible circuit historically called a polymer thick film circuit; it seems to have caught on likely due to the large amount of government and industry in-kind funding to promote use of digital inkjet printing technologies and low-cost substrates along with conductive adhesives to make novel low cost elec-

The term “flex hybrid electronic” is a relatively new term that has been coined to rebrand a lower-cost type of flexible circuit historically called a polymer thick film circuit.

tronic assemblies. Polymer thick film circuits are also typically produced by printing but by screen printing conductive silver-based inks onto a thin, typically polyester polymer film. The features are generally coarser, and the silver conductors have historically tended to be more resistive and thus less suitable for higher power or higher performance applications, but they have proven to be very well suited to applications where power is lower and higher voltages are used. One of their most common applications has been in the manufacture of membrane switches and keyboard circuits, but the technology has been adapted to the manufacture of numerous other products.

Another distinction between the two is that FHE not only has greater demonstrated interest in the use of inkjet printing but also increased focus on the integration of electronic components and function into the designs facilitated by sequentially inkjet printing conductive, resistive, insulating and even semiconductive materials to realize unique flexible circuit designs. This includes the prospective printing of resistors, capacitors, and inductors of some precision. There is also demonstrated interest in building in sensors and thinning of semiconductor ICs to make them flexible as well.

In summary, the line separating polymer thick film flexible circuit assemblies from flexible hybrid electronics exists, but it is not hard and bright. The introduction of new flexible circuit manufacturing technologies and materials including stretchable substrates has created a surge of interest in their use. This is due in no small part to the versatility they offer. As a nearly half-century veteran of the electronics interconnection industry, including participating in a startup that sought to produce flexible circuits on a moving web in 1990, I have a bit longer view and perhaps a bit more appreciation of the evolution of flexible circuit technology.

The advances being offered coming from and being exploited by those newer entrants to the industry have injected a new vitality to a venerable type of flexible circuit in the form of FHE. That energy and creativity is resulting in FHE proving itself to be highly useful in ways heretofore unseen in the past. For that, my hat is off to them. **DESIGN007**



Joe Fjelstad is founder and CEO of Verdant Electronics and an international authority and innovator in the field of electronic interconnection and packaging technologies with more than 185 patents issued or pending. To

read past columns or contact Fjelstad, [click here](#). Download your free copy of Fjelstad's book *Flexible Circuit Technology, 4th Edition*, and watch his in-depth workshop series “Flexible Circuit Technology.”

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Flex007 Highlights



Flex Talk: Communicating Outside the Box Is Key to Flex DFM ▶

What do you do when you are designing a flexible circuit and need to go “way outside the box” to get the desired end-result? Tara Dunn looks at a few success stories, including gold conductors and complex rigid-flex, and emphasizes the power of communication.

Lenthor Engineering Adds 3 MicroCraft EMMA Flying Probe Testers ▶

Lenthor Engineering, Inc., a California based designer, manufacturer and assembler of Flex and Rigid-Flex printed circuit boards, has announced the installation of three new EMMA E4M6151 Flying Probe test units from Microcraft.

Pacothane on the Future of Laminate Technologies ▶

Nolan Johnson recently spoke with the Pacothane Technologies team about the current drivers of circuit board technology and how that has influenced and increased their product development of lamination and lamination assist products.

MKS Sees Strong Sales for its Latest Flexible PCB Laser Processing Solution ▶

MKS Instruments, Inc., a global provider of technologies that enable advanced processes and improve productivity, announced that a leading PCB manufacturing customer in the Greater China region has purchased 80 units of the company's ESI CapStone system for near-term delivery.

Just Ask Tara Dunn: The Exclusive Compilation ▶

We asked for you to send in your questions for Averatek's Tara Dunn, and you took us

up on it! We know you all enjoyed reading these questions and answers, so we've compiled all of them into one article for easy reference. And if you'd like to hear more from Tara, be sure to view her Flex007 column series “Flex Talk.”

New Orbotech Flex PCB Manufacturing Solutions Enable Future Generations of Advanced Electronics ▶

Orbotech, a KLA company, announced two new roll-to-roll (R2R) manufacturing solutions for flexible printed circuit (FPCs), enabling the design and mass production of new generations of electronic devices, including 5G smartphones, advanced automotive and medical devices.

Consider This: Buried Capacitance Power Planes ▶

Why do we need capacitance between the power and ground planes? When you think of voltage, remind yourself it must be a loop. What you send out to power the chip you have to get back to ground to complete the path. Basic electrical law states that every power or signal line needs a ground or return. John Talbot explores this and more.

Stretchable Micro-Supercapacitors to Self-Power Wearable Devices ▶

A stretchable system that can harvest energy from human breathing and motion for use in wearable health-monitoring devices may be possible, according to an international team of researchers, led by Huanyu “Larry” Cheng, Dorothy Quiggle Career Development Professor in Penn State's Department of Engineering Science and Mechanics.

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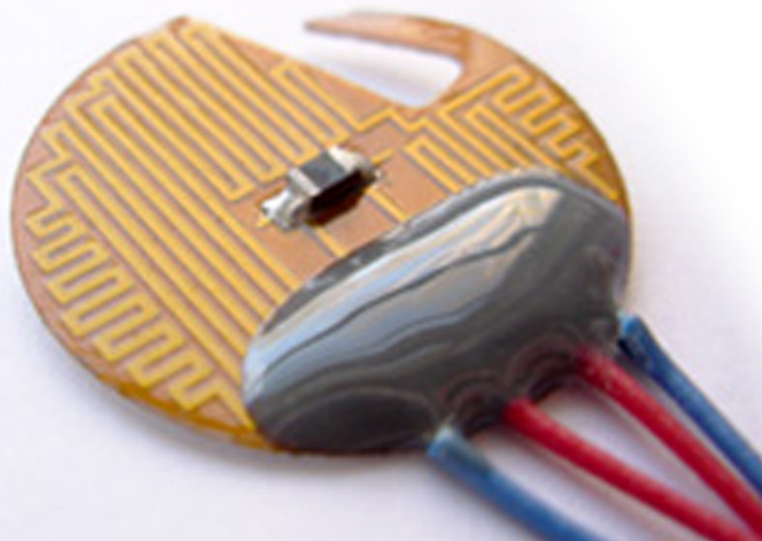
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PCB Industry Statistical Data

EPTE Newsletter

by Dominique K. Numakura, DKN Research LLC

Just about all electronic equipment uses printed circuit boards or flexible circuits for wiring and packaging materials. Electronic companies design their products and then place orders for PCBs. Supply chains order accordingly, and business trends begin to unfold from the PCB industry. This sounds simple enough, but countries and regions collect manufacturing data differently, so you have to understand statistical industry data before making forecasts.

The Ministry of Economy and Industry (METI) in Japan provides monthly shipping data from manufacturers that include volume and revenue. This data is categorized into three buckets: rigid circuit boards, flexible circuits, and module substrates. The METI collects shipping data from Japanese manufacturers

monthly, but these manufacturers outsource to other countries and this data does not include outsourced production. It is difficult to determine the percent of business shifted to other countries, but most of us believe the number is about 60%.

The U.S. standards organization IPC provides a monthly book-and-bill ratio comparing shipping data within North America. The data compares revenue changes from the industry collected from manufacturers. This data is not absolute revenue, so the industry results cannot be compared to other regions.

The Taiwan Printed Circuit Association (TPCA) provides monthly shipping revenue from publicly traded companies listed on the Taipei Stock Exchange. There are 40 companies categorized into two groups: rigid boards or





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flexible circuits. The shipping data is provided within three weeks after the month ends and is reported quickly enough to determine business trends from the global electronic industry. The data is a little convoluted because production for many manufacturers is from Mainland China, and revenue includes shipments from here.

The TPCA also provides quarterly shipping data from 22 publicly traded companies in China (many manufacturers are headquartered in other countries). There are two industry associations in China: The China Printed Circuit Association (CPCA) and the Hong Kong Printed Circuit Association (HKPCA). Data from some manufacturers could be counted twice, and there are a few thousand PCB manufacturers in China that do not report their volume.

ZVEI, the PCB industry association in Germany provides quarterly market data from the German region that includes Switzerland and Austria. Similar with data collected by the IPC, it is not absolute revenue so the industry results cannot be compared to other regions.

The Korea Printed Circuit Association (KPCA) provides an annual report from the industry, so trends are difficult to detect in a timely manner.

There is no uniform method of collecting data from our industry.

There is no uniform method of collecting data from our industry. Evaluating numerical market information is difficult for the global market. The World Electronics Circuits Council (WECC) publishes an annual market report, but the infrequency of its release makes it difficult to see emerging trends.

The good news is the global PCB industry is growing! Business continues to shift from the U.S. and Europe to the Far Eastern region and a uniform method of reporting could provide a solid platform to make informed decisions.

Recent Headlines

1. JDL (Major display manufacturer in Japan) 12/9

Has demonstrated a new touch panel switch. It works without actual touch. But it has a high resolution by capacitance sensors. JDL will start the production in 2021.

2. AIST (Major R&D organization in Japan) 12/10

Has co-developed a new hCFET (heterogeneous Complementary-Field Effect Transistor) assuming 2 nm process with TSRI in Taiwan.

3. Tohoku University (Japan) 12/10

Has unveiled new tiny magnetic tunnel junction device with 2.3 nm diameter. It works at 150°C.

4. SCREEN Semiconductor (Major equipment supplier in Japan) 12/11

Has commercialized a new large scale wafer scrubbing machine "SS3300S." The machine is capable of processing 1000 wafers per hour.

5. AGC (Major glass product supplier in Japan) 12/14

Has developed a new glass "WAVETRAP" with shielding capability. A fine metallic mesh sandwiched between glass plates absorbs RF wave effectively.

6. Panasonic (Major electronics company in Japan) 12/15

Has rolled out a new connector series "R35K" for high density flex circuits. Height: 0.6 mm, Width: 1.3 mm. Panasonic expects major applications in wearable devices.

7. NIMS (R&D organization in Japan) 12/15

Has discovered a new trans element base semiconductor without toxic element for near infrared ray. The chemical composition is Ca_3SiO .

8. Xacty (Device manufacturer in Japan) 12/16

Has unveiled a new wearable camera "CX-WE300" for business use. The camera has a reliable correction function against vibrations.

9. JAE (Major device manufacturer in Japan) 12/16

Has commercialized a series of small size antenna “AN01” with a high radiation efficiency for 2.4 GHz, 5GHz and 920MHz bands of IoT equipment and automobile modules.

10. TDK (Major device supplier in Japan) 12/16

Has developed a new chip type noise control filter, “MDF1005,” for PoC (Power over Coaxial) of automobile applications. Size: 1.0 x 0.5mm.

11. NIMS (R&D organization in Japan) 12/16

Has developed a new heat-resistant vibration device built by GaN base MEMS process 5G device and automobiles. It works at 326°C. **DESIGN007**



Dominique K. Numakura is the managing director of DKN Research LLC. Contact haverhill@dknresearch.com for further information and news. To read past columns, [click here](#).

Geek+, Universal Logic Team Up to Explore Flexible Automation, Industry 4.0

Geek+, a global leader in autonomous mobile robots (AMRs) and warehouse automation, and Universal Logic, a world-leading pioneer of an AI/sensor/machine-control software “brain” for robots, announce the beginning of a new partnership. Together, the two technology leaders declare a joint commitment to support the manufacturing and logistics industry with a paradigm-shifting goods-to-robot solution, for automating supply chain operations and elevating industry 4.0.

The partnership will give Universal Logic access to Geek+’s wide range of robotics hardware for intelligent sorting and picking. Built on autonomous mobile robot technology and AI-driven software, Geek+ will provide Universal Logic with the flexibility to automate the entire chain from dynamic inventory control to pick & pack, expanding from goods-to-man to goods-to-robot solutions. Correspondingly, Geek+ will have access to Neo-cortex, Universal Logic’s AI platform featuring real-time and modular robot control for extended perception, direct grasping, and advanced robot guidance, enabling human-like flexible picking capabilities, to unleash the true potential of intelligent robotics for logistics.

Universal Logic CEO, David Peters, states: “The Geek+ mobile robot platform, dovetails perfectly with Universal’s dynamic robot control for picking and packing, providing our customers seamless automation capabilities, creating an end-to-end solution to meet current and future supply chain needs.”

Today, Geek+ and Universal Logic respectively serves a broad customer range including Fortune 500 Companies and regional businesses. The collaboration will enable them to strengthen their industry leadership and provide clients with flexible, adaptable, and efficient operations that can meet challenges associated with high mix/high volume applications in manufacturing, wholesale, and retail. By combining the efficiency and speed of robots with human-like precision and flexibility, it will allow businesses to realize stable and reliable supply chain operations and meet the challenges of tomorrow.

(Source: PRNewswire)



Advancements in Printed Circuit Manufacturing Equipment

Consider This

by John Talbot, TRAMONTO CIRCUITS

Computers, lasers, and artificial intelligence are infiltrating every area of the PCB manufacturing facility. Over the last few years, most printed circuit manufacturers have invested heavily in integration of the complete shop equipment, controlled from one central computer mainframe. The interconnecting intelligence allows for quicker file processing, higher accuracy, and vastly improved yields.

One of the most expensive machineries is the laser direct imaging (LDI) system. There has been significant improvement in the accuracy, speed, quality, and reduction in overall manufacturing rejects. The new machines feature numerous cameras to locate the alignment holes, comparing them to the original Gerber file, and then digitally scaling the image to fit the panel. The newer laser imaging machines

are capable of imaging down to 15-micron line widths and spaces.

From the beginning of a new PCB order, more powerful CAD/CAM manufacturing software is used to inspect the Gerber files, perform a design rule check, and identify any trace or hole violations that would result in shorts or opens later in the process. The new powerful software checks impedance throughout the circuit traces and layers. It adjusts for laminate shrinkage by calculating scaling and resizing each layer to compensate. The software will calculate etchback on traces and panelizes the job for maximum yield.

The software does not stop there. It coordinates feedback from post lamination alignment and X-ray drill, and adjusts each layer's scaling in a database to ensure tighter layer-to-layer



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alignment. The software sends all the required information to the drills, routers, testers, imaging and any other machines connected to the company's own internal network.

The biggest change has been the addition of lasers to many operations and machines—from laser drills that can sculpt through laminate to create blind microvias, to copper cutting/trimming lasers built into the automatic optical inspection units. These new lasers can easily remove small shorts. New technology even allows for 3D printing of copper to repair opens in a circuit, which greatly improves yields.

New technology even allows for 3D printing of copper to repair opens in a circuit, which greatly improves yields.

Computers are producing higher accuracy in alignment of inner layers by detecting errors in scaling of each layer with X-ray and then correcting the drilling files to correctly align the tooling holes for lamination and drilling.

Today's drilling machines, vastly superior to machines of only a few years ago, are equipped with laser drill size measurement, broken bit detection, and massive drill canisters which automatically change bits according to wear or hit counts. The drills feature controlled depth drilling for back drilling of vias to reduce capacitance and improve impedance. Newer drills feature up to 250,000 rpm air bearing heads, and very high-speed drilling and very accurate table servos. In addition to normal mechanical drilling, manufacturers have laser drills. Powerful UV lasers cut through the copper and FR-4 material to drill tiny microvias one or two layers down, and thicker copper stop pads are used to halt the laser. Laser drilling is essential for HDI or very fine micro-PCBs required for today's microelectronics.

To improve inner layer drilling registration, X-rays look inside for special alignment pads

and then find the best compromised location of the pads. The software then calculates for stretch or shrinkage in the panel's size after lamination. They automatically adjust the drill file size by using scaling and drill alignment holes so the drill will more accurately hit the center of all pads. The machine will communicate to the drill unit, giving it new X-Y and offset stretch coordinates so it can increase or decrease the data file position and size of the panel to more accurately hit the center of all the pads.

Inkjet solder mask units eliminate the old inaccurate silkscreen method. The machine has multiple ink jet heads that quickly spray accurate lines, letters and drawings in white ink onto the finished solder mask. A powerful UV lamp dries and cures the ink as it sprays on the PCB. This eliminates the messy manufacturing of the silkscreen, the flip table, and the squeegee-ing of ink onto the PCB.

Computers are now controlling the plating bath chemistry through constant monitoring and titrations. They sense a deficiency on one of the many chemicals and automatically add in the right amount to correct the bath during the run. The measuring and adjustment are all done in real-time. The chemical baths do not suddenly go out of specification, and important parameters such as copper ductility are well controlled.

Inkjet solder mask units have two different options. Older ones spray the entire board, which is then imaged with a laser direct imaging unit, developed, and then cured. Newer inkjet solder mask units apply and cure the solder mask ink with the openings for vias, directly onto the board. A powerful UV light then cures the solder mask right on the machine.

Computers in the lab allow for quicker cross-sections and easier spotting of potential problems before the boards are shipped. As well, the shop will have computerized tracking using bar codes or QR codes. The production manager can look at his computer identifying any job that is falling behind.

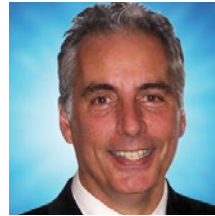
Newer flying probe electrical testing equipment is much faster. They feature many more little heads to probe each point on the printed

circuit to test for shorts or opens. The improved speed and accuracy eliminate the need for older, fixed bed probe units.

Laser cutters for flex circuits quickly and very accurately, shape, scallop and cut the flex circuits, eliminating the old kick press and steel rule die method.

Cost saving is the goal. Even though a single direct imaging laser can cost well over a million dollars, a PCB facility lives or dies based on yields. In the past, a 70% yield was considered doing very well. Today with all the computer and laser assistance in manufactur-

ing, most manufacturers are easily in the high 90% yield. This improvement goes directly to the bottom line. As well, it greatly reduces the dreaded re-run, which costs money and creates a delay in the delivery schedule to the customer. **DESIGN007**



John Talbot is president of Tramonto Circuits. To read past columns or contact Talbot, [click here](#).

Exium Debuts the World's First 5G Clean Network

The innovative tech startup Exium announced the premiere of its Secure 5G network as a service, based on the emerging Clean Network standards being promulgated by the US, EU and other freedom-loving nations.

Exium's 5G network service is built on an open, programmable, reliable, and software-driven Intelligent Cybersecurity Mesh™ that treats the internet itself as Zero Trust and relies heavily on strong encryption for all data transmitted, processed, or stored anywhere on it. This approach enables secure and private end-to-end connectivity and provides the ability to securely operate anywhere and anytime, regardless of the environment, even on underlying networks that may be compromised.

Exium's clean network is rooted in internationally accepted digital trust standards such as the Criteria for Security and Trust in Telecommunications Networks and Services developed by the Center for Strategic and International Studies (CSIS), the Prague Proposals, and the European Union's 5G Toolbox. The end-to-end clean network utilizes trusted hardware and software components, including the cloud-infrastructure and global backbone built and operated exclusively by US companies, such as Amazon, Google, and Microsoft.

Exium launched as a startup to serve businesses that are increasingly demanding the same end-to-end security standards that the US government requires for its communications.

"The only way to be sure a network is clean is architecting and building it from the bot-

tom up. The recent spate of cyberattacks were possible because outdated, proprietary systems are still being used across organizations," said Farooq Khan, founder, and CEO at Exium.

Exium's 5G clean network service is available globally on six continents. The service is device and network agnostic, and users can benefit from 5G clean network security and privacy on 4G, WiFi, Fiber, Cable or even Satellite networks. The service natively works with 5G devices without requiring any software updates. For non-5G devices, including Windows and Mac computers, a 5G software app, available on Exium's website, is required.

(Source: PRNewswire)





1 Mentor to Officially Change Name to Siemens EDA ►

Mentor, a Siemens business, will be known as Siemens EDA as of January 2021. The organization continues to operate as part of Siemens Digital Industries Software. Under this new banner, Siemens is bringing together the world's most comprehensive portfolio of EDA software, with Siemens technology for simulation, mechanical design, manufacturing, cloud, IoT and low-code.

3 Altium Divests Non-Core TASKING to Support, Enable Investment in Altium 365 ►

Electronic design software company Altium Limited has entered into a definitive agreement with FSN Capital to sell the assets of its TASKING business for US\$110 million. The transaction will be settled in cash with US\$100 million up front and \$10 million conditional upon achieving revenue targets in Fiscal 2021 post divestment.

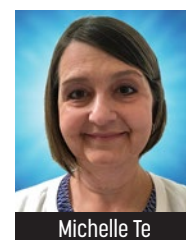
2 Cadence's Clarity: 'I Can See Clearly Now' ►

Do you recall the song "I Can See Clearly Now"? In this article, Clive "Max" Maxfield notes he had just been looking at the Clarity 3D Transient Solver from Cadence, so the lyrics he heard in his head were, "I can see clearly now the EMI is gone/I can see all EMC obstacles in my way..."



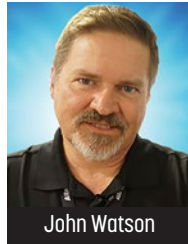
4 Oops, I Did It Again: Survey Details Most Common Design Errors ►

We hate to admit it, but even the best of us make mistakes. Such is true with PCB designers and design engineers. We wondered: What are the most common mistakes that PCB designers make? Michelle Te has more.



5 Elementary, Mr. Watson: Demystifying Bypass Capacitors ►

As PCB designers, we work under the simple rule of cause and effect, and a PCB design can quickly become a petri dish for the butterfly effect to flourish. One of those areas that can quickly snowball into major problems is your PCB power distribution structure. When it goes wrong, it usually goes very wrong and has significant issues throughout your design.



6 The Pulse: Don't Ignore DC Trace Resistance ►

Time flies! But the laws of physics don't. Martyn Gaudion focuses on how important it is becoming to take DC trace resistance into account when measuring and specifying thin copper traces.



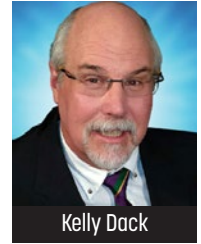
7 IPC Releases IPC-2581 Revision C for PCB Design ►

IPC-2581C Generic Requirement for Printed Board Assembly Product Manufacturing Description Data and Transfer Methodology is the eagerly anticipated update of IPC's widely adopted global standard for PCB design through manufacturing data flow.



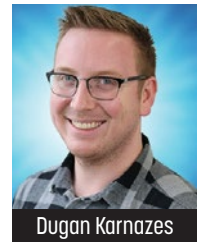
8 The Digital Layout: PCEA 2020—Small Rearview Mirror, Big Windshield ►

In this month's forward-driving column, Kelly Dack glances back at PCEA's year in "rearview," and PCEA Chairman Stephen Chavez focuses on what lies ahead. Dack also points out some interesting events for you to consider attending.



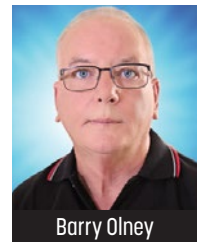
9 Figure It Out: Closing the Gap Between College and Industry with PCEA ►

What is the solution for the knowledge gap between industry requirements and college education? Dugan Karnazes explores what PCEA is doing to inspire, educate and unite PCB designers.



10 Beyond Design: Simulation Slashes Iterations ►

The majority of high-speed digital designs take at least two iterations to develop into a working product. However, multilayer boards can be designed to work right the first time with little additional effort. Barry Olney explains how design respins will continue to happen until designers make regular use of simulation software.



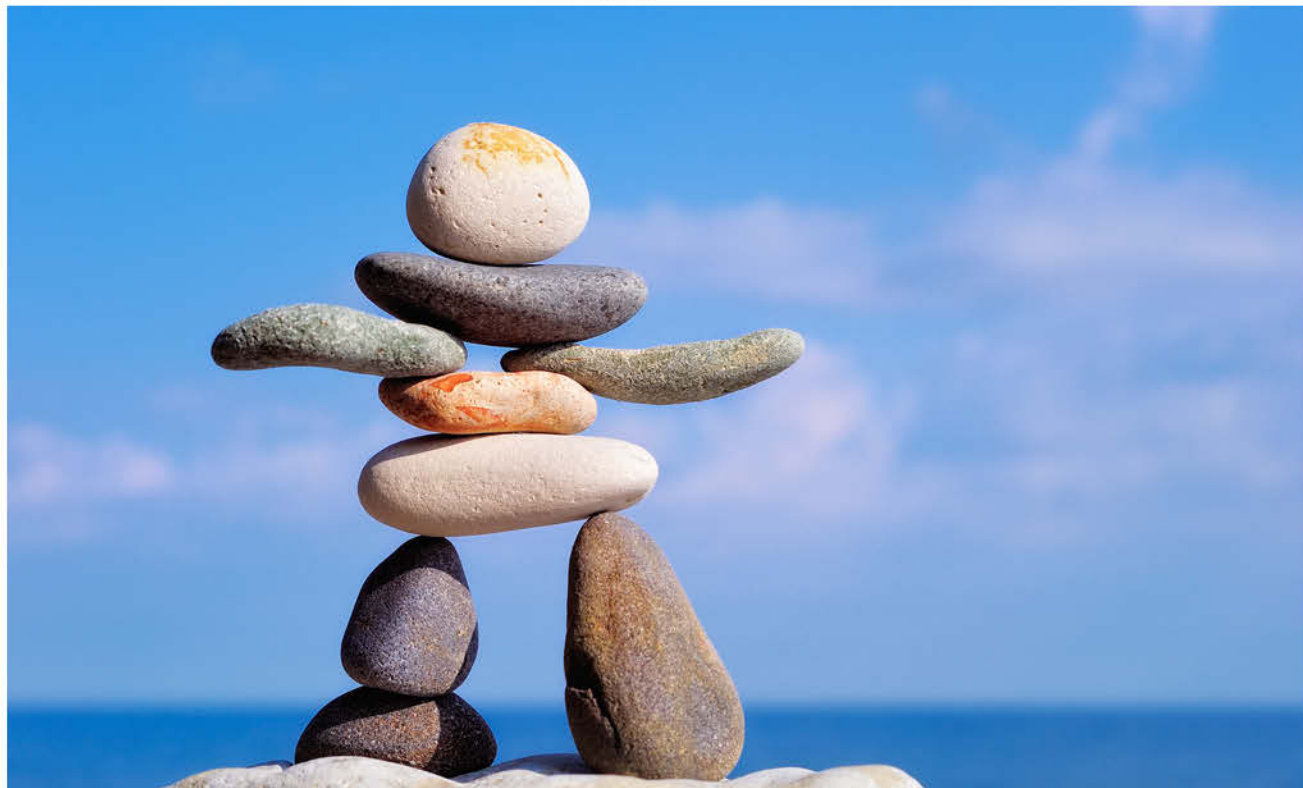
PCBDesign007.com

for the latest circuit design news and information.

Flex007.com

focuses on the rapidly growing flexible and rigid-flex circuit market.

Career Opportunities



How Do Your Team Members Stack Up?

Find industry-experienced candidates at I-Connect007.

For just \$750, your 200-word, full-column ad will appear in the "career opportunities" section of all three of our monthly magazines, reaching circuit board designers, fabricators, assemblers, OEMs, and suppliers.

In addition, your ad will be featured in at least one of our newsletters, and your posting will appear on our jobConnect007.com board, which is also promoted in every newsletter.

Potential candidates can click on your ad and submit a resume directly to the email address you provide or be directed to the URL of your choice. If you wish to continue beyond the first month, the price is the same per month.

No contract required. We even include your logo in the ad, which is great branding!

To get your ad into the next issue, contact:

Barb Hockaday at barb@iconnect007.com or +1 916.365.1727 (-8 GMT PST)

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GOOD FOR THE INDUSTRY



Career Opportunities



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INTERNATIONAL GROUP
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Sales Desk & Supply Chain Manager, Leamington Spa, UK

Want to advance your career by joining a globally successful and growing world class CCL manufacturing company and help drive that success? As sales desk & supply chain manager you will work towards maximizing the efficiency and effectiveness of controlling stock levels and sales interactions with the customers and ensuring that the requirement of the business for fast turn delivery of quality products is met in the most cost effective and efficient way. Your tasks will include sales desk & stock management, implementing performance improvement measures, procuring materials and resources and assuring compliance. You will be a mentor to your team members and implement best practices across all levels.

Skills and abilities required:

- Proven commercial experience in similar role for minimum 5 years
- Knowledge of organizational effectiveness and operations management
- Experience with ISO9001 or similar QMS required
- Experience with Lean Six Sigma a plus
- Excellent leadership ability and communication skills (English)
- Computer literate (Microsoft Suite)
- Experience with ERP-systems

What's on offer:

- Excellent salary and benefits commensurate with experience

This is a fantastic opportunity to become part of a successful brand and leading team.

Please apply in the strictest confidence, enclosing your CV to humanresource@ventec-europe.com.

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ventec
INTERNATIONAL GROUP
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Operations Manager, Elk Grove Village IL, USA

Want to advance your career by joining a globally successful and growing world class CCL manufacturing company and help drive that success? As operations manager at Ventec USA LLC, a wholly owned subsidiary of Ventec International Group, you will coordinate and oversee our organization's operations in Elk Grove Village, IL, and Fullerton, CA. Your tasks will include formulating strategy, implementing performance improvement measures, procuring materials and resources and assuring compliance. You will be a mentor to your team members, find ways to maintain and improve the highest quality of customer service and implement best practices across all levels.

Skills and abilities required for the role:

- Proven commercial experience as operations manager or similar role for minimum 5 years
- Knowledge of organizational effectiveness and operations management
- Experience with ISO9001 or similar QMS required
- Experience in budgeting and forecasting & familiarity with business and financial principles
- Excellent leadership ability and communication skills (English)
- Outstanding organizational skills
- Degree in Business, Operations Management, or related field preferred but not required

What's on offer:

- Excellent salary and benefits commensurate with experience

This is a fantastic opportunity to become part of a successful brand and leading team with excellent benefits.

Please forward your resume to jpattie@ventec-usa.com and mention "Operations Manager—Elk Grove Village" in the subject line.

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Career Opportunities

Now Hiring

Director of Process Engineering

A successful and growing printed circuit board manufacturer in Orange County, CA, has an opening for a director of process engineering.

Job Summary:

The director of process engineering leads all engineering activities to produce quality products and meet cost objectives. Responsible for the overall management, direction, and coordination of the engineering processes within the plant.

Duties and Responsibilities:

- Ensures that process engineering meets the business needs of the company as they relate to capabilities, processes, technologies, and capacity.
- Stays current with related manufacturing trends. Develops and enforces a culture of strong engineering discipline, including robust process definition, testing prior to production implementation, change management processes, clear manufacturing instructions, statistical process monitoring and control, proactive error proofing, etc.
- Provides guidance to process engineers in the development of process control plans and the application of advanced quality tools.
- Ensures metrics are in place to monitor performance against the goals and takes appropriate corrective actions as required. Ensures that structured problem-solving techniques are used and that adequate validation is performed for any issues being address or changes being made. Develops and validates new processes prior to incorporating them into the manufacturing operations.
- Strong communication skills to establish priorities, work schedules, allocate resources, complete required information to customers, support quality system, enforce company policies and procedures, and utilize resources to provide the greatest efficiency to meet production objectives.

Education and Experience:

- Master's degree in chemical engineering or engineering is preferred.
- 10+ years process engineering experience in an electronics manufacturing environment, including 5 years in the PCB or similar manufacturing environment.
- 7+ years of process engineering management experience, including 5 years of experience with direct responsibility for meeting production throughput and quality goals.

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Now Hiring

Process Engineering Manager

A successful and growing printed circuit board manufacturer in Orange County, CA, has an opening for a process engineering manager.

Job Summary:

The process engineering manager coordinates all engineering activities to produce quality products and meet cost objectives. Responsible for the overall management, direction, and coordination of the engineering team and leading this team to meet product requirements in support of the production plan.

Duties and Responsibilities:

- Ensures that process engineering meets the business needs of the company as they relate to capabilities, processes, technologies, and capacity.
- Stays current with related manufacturing trends. Develops and enforces a culture of strong engineering discipline, including robust process definition, testing prior to production implementation, change management processes, clear manufacturing instructions, statistical process monitoring and control, proactive error proofing, etc.
- Ensures metrics are in place to monitor performance against the goals and takes appropriate corrective actions as required. Ensures that structured problem-solving techniques are used and that adequate validation is performed for any issues being address or changes being made. Develops and validates new processes prior to incorporating into the manufacturing operations

Education and Experience:

- Bachelor's degree in chemical engineering or engineering is preferred.
- 7+ years process engineering experience in an electronics manufacturing environment, including 3 years in the PCB or similar manufacturing environment.
- 5+ years of process engineering management experience, including 3 years of experience with direct responsibility for meeting production throughput and quality goals.

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Career Opportunities



IPC Instructor Longmont, CO; Phoenix, AZ; U.S.-based remote

*Independent contractor,
possible full-time employment*

Job Description

This position is responsible for delivering effective electronics manufacturing training, including IPC Certification, to students from the electronics manufacturing industry. IPC instructors primarily train and certify operators, inspectors, engineers, and other trainers to one of six IPC Certification Programs: IPC-A-600, IPC-A-610, IPC/WHMA-A-620, IPC J-STD-001, IPC 7711/7721, and IPC-6012.

IPC instructors will conduct training at one of our public training centers or will travel directly to the customer's facility. A candidate's close proximity to Longmont, CO, or Phoenix, AZ, is a plus. Several IPC Certification Courses can be taught remotely and require no travel.

Qualifications

Candidates must have a minimum of five years of electronics manufacturing experience. This experience can include printed circuit board fabrication, circuit board assembly, and/or wire and cable harness assembly. Soldering experience of through-hole and/or surface-mount components is highly preferred.

Candidate must have IPC training experience, either currently or in the past. A current and valid certified IPC trainer certificate holder is highly preferred.

Applicants must have the ability to work with little to no supervision and make appropriate and professional decisions.

Send resumes to Sharon Montana-Beard at
sharonm@blackfox.com.

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**Our Summit Anaheim, CA, division
currently has multiple open positions
for planning engineers.**

The planner is responsible for creating and verifying manufacturing documentation, including work instructions and shop floor travelers. Review lay-ups, details, and designs according to engineering and customer specifications through the use of computer and applications software. May specify required manufacturing machinery and test equipment based on manufacturing and/or customer requirements. Guides manufacturing process development for all products.

Responsibilities:

1. Accurately plan jobs and create shop floor travelers.
2. Create documentation packages.
3. Use company software for planning and issuing jobs.
4. Contact customers to resolve open issues.
5. Create TDR calculations.
6. Assist in the training of new planning engineers.
7. Review prints and purchase orders.
8. Create stackups and order materials per print/spec.
9. Plan jobs manufacturing process.
10. Institute new manufacturing processes and or changes.

Education/Experience:

1. High school diploma or equivalent
2. Minimum five (5) years' experience in the printed circuit board industry with three (3) years as a planning engineer.
3. Must be able to cooperate and communicate effectively with customers, management, and supervisory staff.
4. Must be proficient in rigid, flex, rigid/flex, and sequential lam designs.

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Career Opportunities



We're Hiring! Connecticut Locations

Senior Research Chemist: **Waterbury, CT, USA**

Research, develop, and formulate new surface treatment products for the printed circuit board, molded interconnect, IC substrate, and LED manufacturing industries. Identify, develop, and execute strategic research project activities as delegated to them by the senior research projects manager. Observe, analyze, and interpret the results from these activities and make recommendations for the direction and preferred route forward for research projects.

Quality Engineer: **West Haven, CT, USA**

Support the West Haven facility in ensuring that the quality management system is properly utilized and maintained while working to fulfill customer-specific requirements and fostering continuous improvement.

For a complete listing of career opportunities or to apply for one of the positions listed above, please visit us here.

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We're Hiring! Illinois / New Jersey

Technical Service Rep: **Chicago, IL, USA**

The technical service rep will be responsible for day-to-day engineering support for fabricators using our chemical products. The successful candidate will help our customer base take full advantage of the benefits that are available through the proper application of our chemistries.

Applications Engineer: **South Plainfield, NJ, USA**

As a key member of the Flexible, Formable, and Printed Electronics (FFPE) Team, the applications engineer will be responsible for developing applications know-how for product evaluation, material testing and characterization, and prototyping. In addition, this applications engineer will provide applications and technical support to global customers for the FFPE Segment.

For a complete listing of career opportunities or to apply for one of the positions listed above, please visit us here.

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Career Opportunities



SMT Operator Hatboro, PA

Manncorp, a leader in the electronics assembly industry, is looking for a **surface-mount technology (SMT) operator** to join their growing team in Hatboro, PA!

The **SMT operator** will be part of a collaborative team and operate the latest Manncorp equipment in our brand-new demonstration center.

Duties and Responsibilities:

- Set up and operate automated SMT assembly equipment
- Prepare component kits for manufacturing
- Perform visual inspection of SMT assembly
- Participate in directing the expansion and further development of our SMT capabilities
- Some mechanical assembly of lighting fixtures
- Assist Manncorp sales with customer demos

Requirements and Qualifications:

- Prior experience with SMT equipment or equivalent technical degree preferred; will consider recent graduates or those new to the industry
- Windows computer knowledge required
- Strong mechanical and electrical troubleshooting skills
- Experience programming machinery or demonstrated willingness to learn
- Positive self-starter attitude with a good work ethic
- Ability to work with minimal supervision
- Ability to lift up to 50 lbs. repetitively

We Offer:

- Competitive pay
- Medical and dental insurance
- Retirement fund matching
- Continued training as the industry develops

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SMT Field Technician Hatboro, PA

Manncorp, a leader in the electronics assembly industry, is looking for an additional SMT Field Technician to join our existing East Coast team and install and support our wide array of SMT equipment.

Duties and Responsibilities:

- Manage on-site equipment installation and customer training
- Provide post-installation service and support, including troubleshooting and diagnosing technical problems by phone, email, or on-site visit
- Assist with demonstrations of equipment to potential customers
- Build and maintain positive relationships with customers
- Participate in the ongoing development and improvement of both our machines and the customer experience we offer

Requirements and Qualifications:

- Prior experience with SMT equipment, or equivalent technical degree
- Proven strong mechanical and electrical troubleshooting skills
- Proficiency in reading and verifying electrical, pneumatic, and mechanical schematics/drawings
- Travel and overnight stays
- Ability to arrange and schedule service trips

We Offer:

- Health and dental insurance
- Retirement fund matching
- Continuing training as the industry develops

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Career Opportunities



Sales Account Manager

Sales Account Management at Lenthor Engineering is a direct sales position responsible for creating and growing a base of customers that purchase flexible and rigid flexible printed circuits. The account manager is in charge of finding customers, qualifying the customer to Lenthor Engineering and promoting Lenthor Engineering's capabilities to the customer. Leads are sometimes referred to the account manager from marketing resources including trade shows, advertising, industry referrals and website hits. Experience with military printed circuit boards (PCBs) is a definite plus.

Responsibilities

- Marketing research to identify target customers
- Identifying the person(s) responsible for purchasing flexible circuits
- Exploring the customer's needs that fit our capabilities in terms of:
 - Market and product
 - Circuit types used
 - Competitive influences
 - Philosophies and finance
 - Quoting and closing orders
 - Providing ongoing service to the customer
 - Develop long-term customer strategies to increase business

Qualifications

- 5-10 years of proven work experience
- Excellent technical skills

Salary negotiable and dependent on experience. Full range of benefits.

Lenthor Engineering, Inc. is a leader in flex and rigid-flex PWB design, fabrication and assembly with over 30 years of experience meeting and exceeding our customers' expectations.

Contact Oscar Akbar at: hr@lenthor.com

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Senior Process Engineer

Job Description

Responsible for developing and optimizing Lenthor's manufacturing processes from start up to implementation, reducing cost, improving sustainability and continuous improvement.

Position Duties

- Senior process engineer's role is to monitor process performance through tracking and enhance through continuous improvement initiatives. Process engineer implements continuous improvement programs to drive up yields.
- Participate in the evaluation of processes, new equipment, facility improvements and procedures.
- Improve process capability, yields, costs and production volume while maintaining safety and improving quality standards.
- Work with customers in developing cost-effective production processes.
- Engage suppliers in quality improvements and process control issues as required.
- Generate process control plan for manufacturing processes, and identify opportunities for capability or process improvement.
- Participate in FMEA activities as required.
- Create detailed plans for IQ, OQ, PQ and maintain validated status as required.
- Participate in existing change control mechanisms such as ECOs and PCRs.
- Perform defect reduction analysis and activities.

Qualifications

- BS degree in engineering
- 5-10 years of proven work experience
- Excellent technical skills

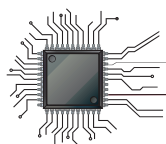
Salary negotiable and dependent on experience. Full range of benefits.

Lenthor Engineering, Inc. is the leader in Flex and Rigid-Flex PWB design, fabrication and assembly with over 30 years of experience meeting and exceeding our customers' expectations.

Contact Oscar Akbar at: hr@lenthor.com

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Career Opportunities



MivaTek

Global

MivaTek Global: We Are Growing!

MivaTek Global is adding sales, technical support and application engineers.

Join a team that brings new imaging technologies to circuit fabrication and microelectronics. Applicants should have direct experience in direct imaging applications, complex machine repair and/or customer support for the printed circuit board or microelectronic markets.

Positions typically require regional and/or air travel. Full time and/or contractor positions are available.

Contact HR@MivaTek.Global
for additional information.

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Become a Certified IPC Master Instructor

Opportunities are available in Canada, New England, California, and Chicago. If you love teaching people, choosing the classes and times you want to work, and basically being your own boss, this may be the career for you. EPTAC Corporation is the leading provider of electronics training and IPC certification and we are looking for instructors that have a passion for working with people to develop their skills and knowledge. If you have a background in electronics manufacturing and enthusiasm for education, drop us a line or send us your resume. We would love to chat with you. Ability to travel required. IPC-7711/7721 or IPC-A-620 CIT certification a big plus.

Qualifications and skills

- A love of teaching and enthusiasm to help others learn
- Background in electronics manufacturing
- Soldering and/or electronics/cable assembly experience
- IPC certification a plus, but will certify the right candidate

Benefits

- Ability to operate from home. No required in-office schedule
- Flexible schedule. Control your own schedule
- IRA retirement matching contributions after one year of service
- Training and certifications provided and maintained by EPTAC

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Career Opportunities



APCT, Printed Circuit Board Solutions: Opportunities Await

APCT, a leading manufacturer of printed circuit boards, has experienced rapid growth over the past year and has multiple opportunities for highly skilled individuals looking to join a progressive and growing company. APCT is always eager to speak with professionals who understand the value of hard work, quality craftsmanship, and being part of a culture that not only serves the customer but one another.

APCT currently has opportunities in Santa Clara, CA; Orange County, CA; Anaheim, CA; Wallingford, CT; and Austin, TX. Positions available range from manufacturing to quality control, sales, and finance.

We invite you to read about APCT at APCT.com and encourage you to understand our core values of passion, commitment, and trust. If you can embrace these principles and what they entail, then you may be a great match to join our team! Peruse the opportunities by clicking the link below.

Thank you, and we look forward to hearing from you soon.

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U.S. CIRCUIT

Sales Representatives (Specific Territories)

Escondido-based printed circuit fabricator U.S. Circuit is looking to hire sales representatives in the following territories:

- Florida
- Denver
- Washington
- Los Angeles

Experience:

- Candidates must have previous PCB sales experience.

Compensation:

- 7% commission

Contact Mike Fariba for more information.

mfariba@uscircuit.com

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- Get instant access to premium 'members-only' eBooks, webinars and more



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Learn from the Experts in Our On-demand Video Series

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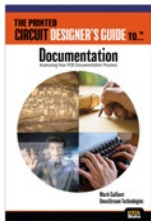
Implementing “Digital Twin” Best Practices From Design Through Manufacturing with Expert Jay Gorajia, a 12-part micro webinar series.



I-007eBooks The Printed Circuit Designer's Guide to...



Thermal Management: A Fabricator's Perspective, by Anaya Vardya, American Standard Circuits
Beat the heat in your designs through thermal management design processes. This book serves as a desk reference on the most current techniques and methods from a PCB fabricator's perspective.



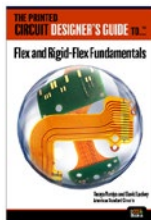
Documentation, by Mark Gallant, Downstream Technologies
When the PCB layout is finished, the designer is still not quite done. The designer's intent must still be communicated to the fabricator through accurate PCB documentation.



Thermal Management with Insulated Metal Substrates, by Didier Mauve and Ian Mayoh, Ventec International Group
Considering thermal issues in the earliest stages of the design process is critical. This book highlights the need to dissipate heat from electronic devices.



Fundamentals of RF/Microwave PCBs, by John Bushie and Anaya Vardya, American Standard Circuits
Today's designers are challenged more than ever with the task of finding the optimal balance between cost and performance when designing radio frequency/microwave PCBs. This micro eBook provides information needed to understand the unique challenges of RF PCBs.



Flex and Rigid-Flex Fundamentals, by Anaya Vardya and David Lackey, American Standard Circuits
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MANAGING EDITOR: **ANDY SHAUGHNESSY**
(404) 806-0508; andy@iconnect007.com

PUBLISHER: **BARRY MATTIES**
barry@iconnect007.com

SALES MANAGER: **BARB HOCKADAY**
(916) 608-0660; barb@iconnect007.com

MARKETING SERVICES: **TOBEY MARSICOVETERE**
(916) 266-9160; tobey@iconnect007.com

TECHNICAL EDITOR: **PETE STARKEY**
+44 (0) 1455 293333; pete@iconnect007.com

CONTRIBUTING TECHNICAL EDITOR: **DAN FEINBERG**
baer@iconnect007.com

CONTRIBUTING TECHNICAL EDITOR: **HAPPY HOLDEN**
(616) 741-9213; happy@iconnect007.com

ASSOCIATE EDITOR: **MICHELLE TE**
michelle@iconnect007.com

PRODUCTION MANAGER: **SHELLY STEIN**
shelly@iconnect007.com

MAGAZINE LAYOUT: **RON MEOGROSSI**

AD DESIGN: **SHELLY STEIN, MIKE RADOGNA ,**
TOBEY MARSICOVETERE

TECHNOLOGY SPECIALIST: **BRYSON MATTIES**

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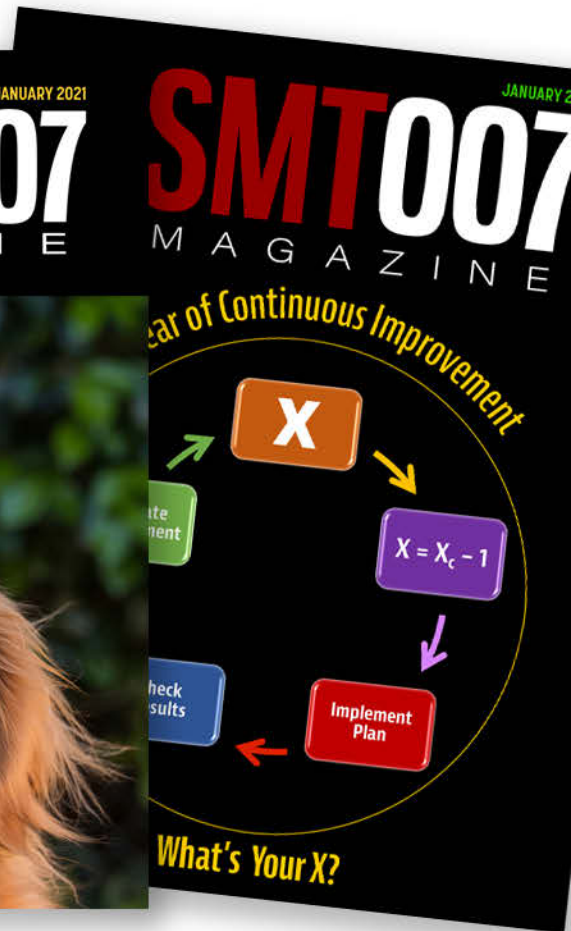
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EDITORIAL CONTACT

Andy Shaughnessy

andy@iconnect007.com

+1 404.806.0508 GMT-5



mediakit.iconnect007.com

SALES CONTACT

Barb Hockaday

barb@iconnect007.com

+1 916 365-1727 GMT-7



www.iconnect007.com