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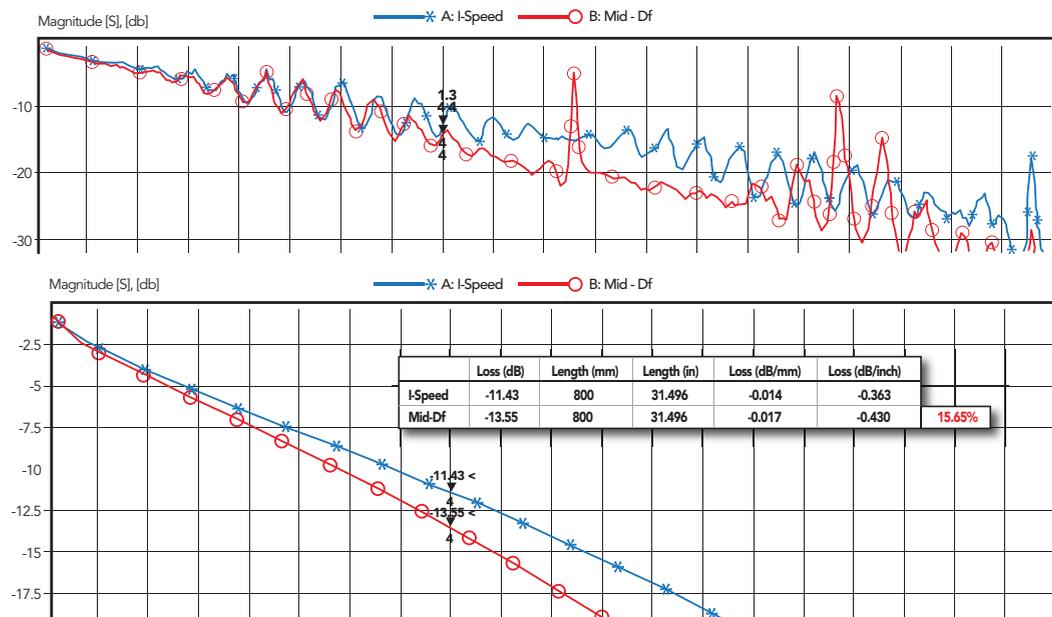
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This Issue: FLEX DESIGN

FEATURED CONTENT

Flexible circuits have come a long way in the past decade. Once considered too costly for most applications, flex circuits can now be found in everything from printers to digital cameras. But designing “flexitos” is quite different than designing rigid boards. In this issue of *The PCB Design Magazine*, our flex contributors offer a variety of flex design tips and techniques.

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by Glenn Oliver, Matt Doyle, John Dangler, Rick Brandwein and Paul Abrahamson



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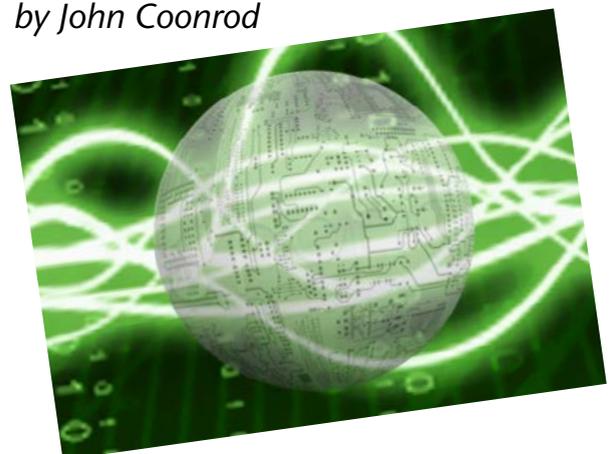
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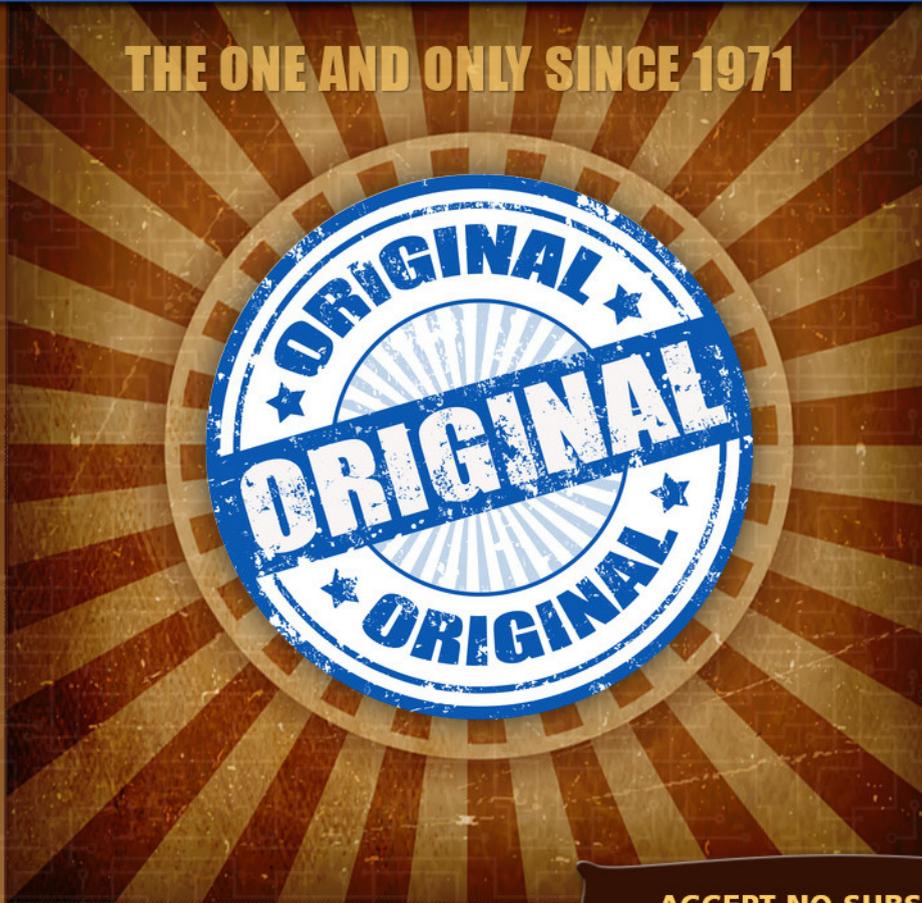




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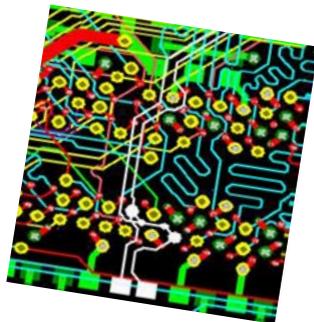


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Zen and the Collaborative Art of Designing, Manufacturing and Implementing Low-Loss, High-Speed Flex Interconnects, Part 1



by **Glenn Oliver**, DUPONT
Matt Doyle and John Dangler, IBM
Rick Brandwein and Paul Abrahamson, MOLEX

SUMMARY: *To maximize performance improvements and ensure the success of advanced flex materials, new design and fabrication trade-offs must be understood by material suppliers, OEM and fabricators. This article represents collaboration between an OEM, a fabricator, and a material supplier with the goal of broadening flex circuits in higher-speed applications.*

Abstract

Increasing data speeds, decreasing edge rates, and intricate form factors challenge our ability to meet electrical and mechanical performance requirements of flexible printed circuits. This paper demonstrates that a focus on advanced flex circuit materials will enable flex circuits to remain a valid interconnect. To maximize per-

formance improvements and ensure the success of advanced flex materials, new design and fabrication trade-offs must be understood by material suppliers, OEM and fabricators. This article represents collaboration between an OEM, a fabricator, and a material supplier with the goal of broadening flex circuits in higher-speed applications. Modeled and measured data will characterize construct performance. In addition, lessons learned will be presented that detail engineering trade-offs required to maximize performance and manufacturability of new flex materials.

Motivation

Conversion from an old, established technology to new innovations often requires fundamental changes at every level, from raw materials all the way to the performance of the ultimate system. For example, automobile bodies have long been made from metal. However, high fuel costs are motivating a significant tech-

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ZEN AND THE COLLABORATIVE ART OF DESIGNING FLEX INTERCONNECTS, PART 1 *continues*

nology shift to utilizing carbon fiber composites as a raw material. While the advantages of this new technology are clear, the technology conversion is far from trivial because the new technology impacts every level of the automobile design, manufacturing and certification process.

For instance, a car body designer has a material that is both lighter and stronger than metal, but there are trade-offs (such as the ability to protect a passenger in a crash) that must be considered, which requires a completely different approach than when designing a car body made of metal. The manufacturer of the vehicle has to re-tool their production line. Processes like welding and assembly have to be optimized for the new material. Finally, the supplier of the raw material has to work with both the designer and the fabricator to supply carbon fibers that are lightweight, strong and meet the cost targets¹. While all of these new implementation tasks inject new risks which must be understood, that risk is balanced by enabling automobile manufacturers to meet more stringent fuel efficiency standards.

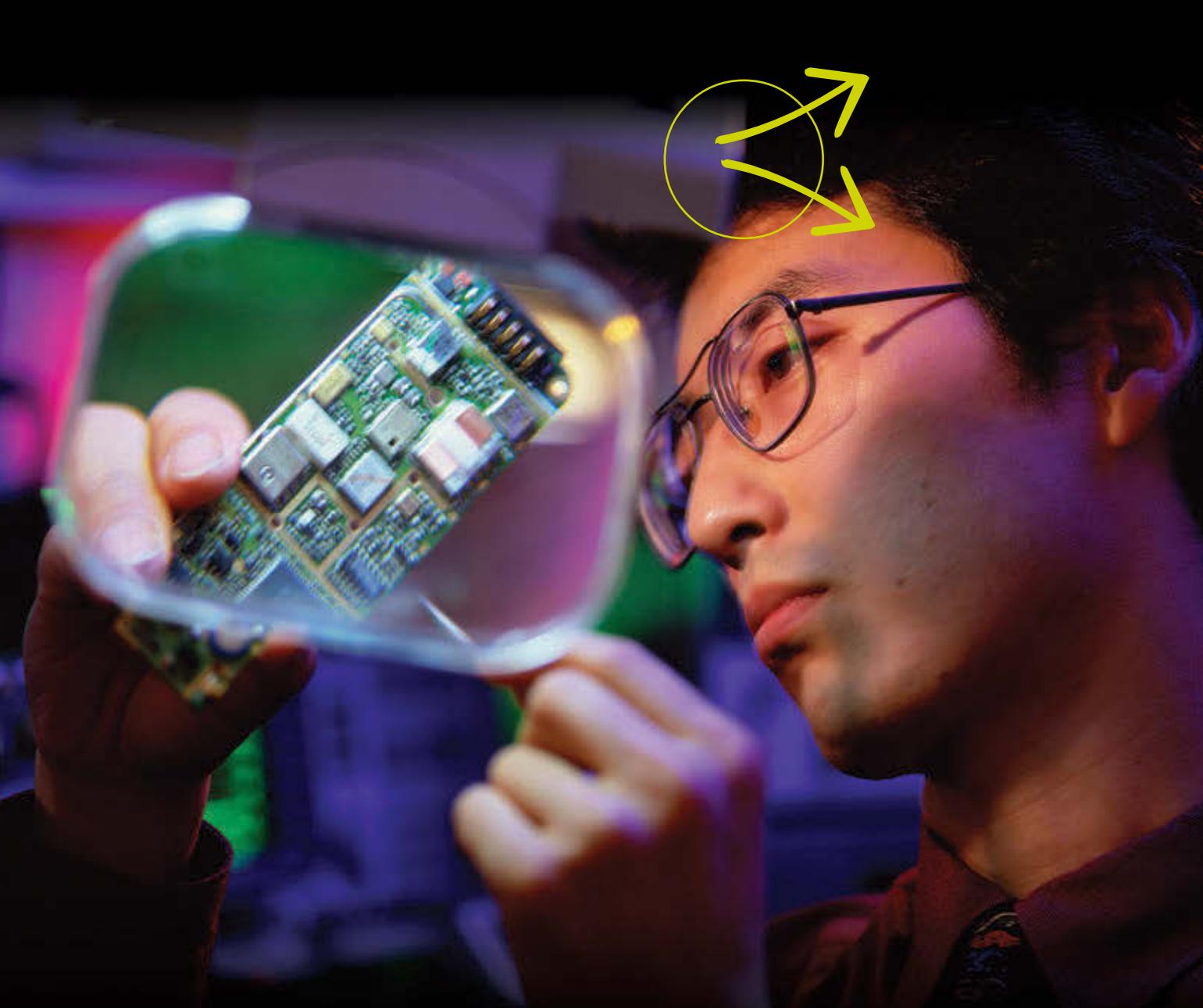
In a similar fashion, performance requirements placed upon the electronics industry force development of high-speed interconnect to consider a vast array of new materials. More specifically, ever-increasing data-rate, bandwidth, and density within smaller form factors with less energy loss force interconnect solutions to reconsider how each material and phys-

ical feature contributes to the end goal. Flexible printed circuits are not immune to these demands and this paper will describe collaboration of an OEM, a fabricator, and a materials supplier to scrutinize existing materials, optimize alterations to those materials, and make necessary trade-offs required to inject new materials into high-speed flexible channels.

Before we begin, it is valuable to briefly discuss why a company or collaboration of companies chooses to invest time into the arena of flexible printed circuits. Given recent rise of personal consumer electronics, it may be obvious that one of the reasons one may consider flexible circuits is interconnect density. Figure 1 depicts one of the most appealing advantages of flex interconnect over alternate methods such as coax². Flex interconnect realizes as good, if not better, mechanical flexibility as coaxial or ribbonized coaxial channels, while yielding far greater IO density given identical volumes. Figure 1 illustrates that given identical physical width and Z-axis height values, a flex circuit can offer as much as five times the IO density than a typical coaxial solution. The potential disadvantage, of course, is that conventional flex presents notably higher insertion loss than conventional coax. However, if the insertion loss disadvantage can be overcome, combined with attractive IO density, the resulting flex structure could be very advantageous. It is for this reason the investigation within this paper proceeded.

Conventional Flex Construct: 500 Signals/SQ*IN**Ribbonized Coaxial Construct: 100 Signals/SQ*IN**

Figure 1: Illustration of the density advantage provided by flexible circuits.



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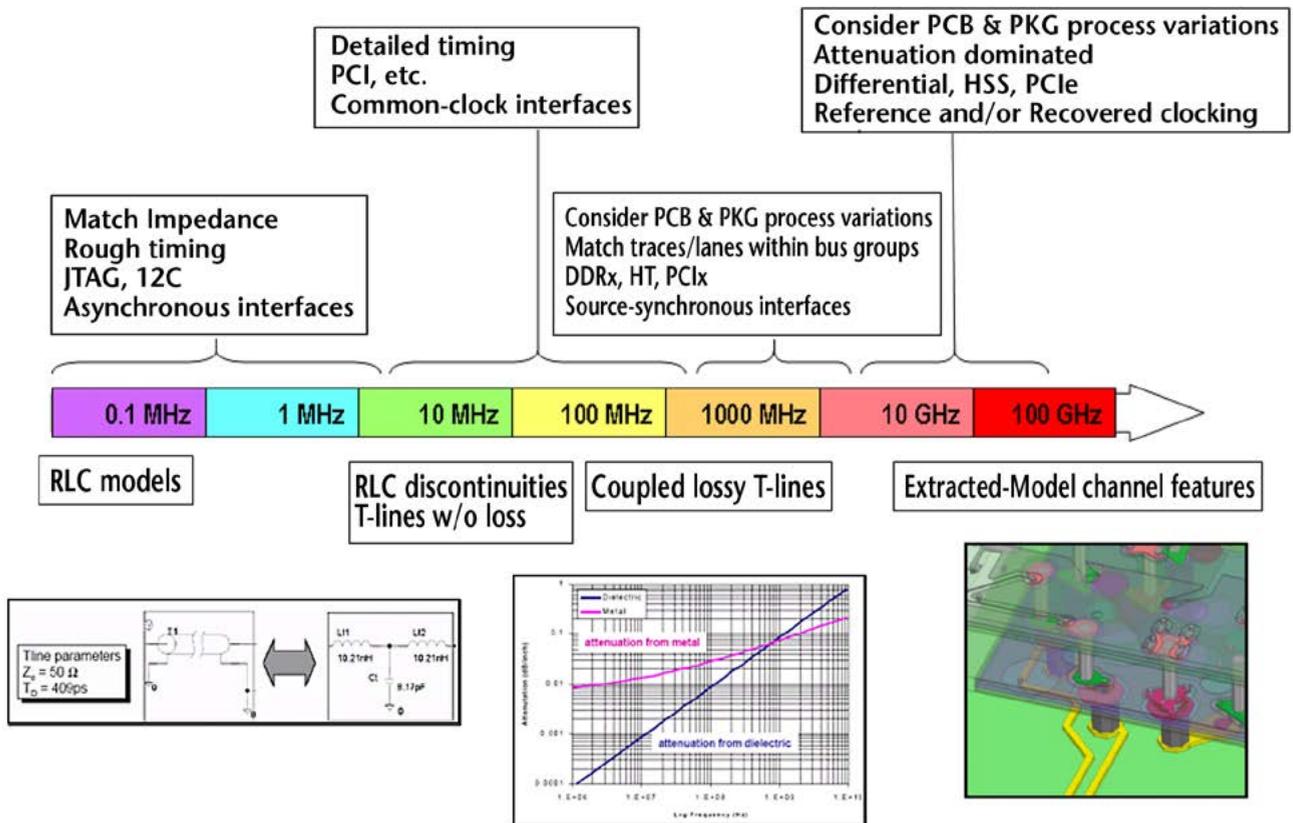
ZEN AND THE COLLABORATIVE ART OF DESIGNING FLEX INTERCONNECTS, PART 1 *continues*

Figure 2: Progression of channel model development.

Problem Statement

As data rates increase and slew rates decrease, the approach to model development and channel characterization must be altered to ensure the channel model response sufficiently mimics the physical structure of the topology in question and, further, that response remains causal. This is critical since accurately depicting the discontinuities realized by the propagating signal becomes increasingly important with faster signaling rates (decreased slew rates) where causal responses may be more difficult to achieve yet critically required for simulation and margin assessment accuracy. As Figure 2 depicts, time and technology have required the channel model developer to change his/her focus from that of RLC, to loss-less and lossy transmission lines and ultimately fully extracted channel models³.

As a consequence of higher frequency content and the need for fully extracted channel models, transmission loss from individual chan-

nel building blocks (materials) weigh heavily on over channel loss budgets. Specifically, individual materials comprising a given channel become important in and of themselves, whereas previously some building block details may have been overlooked or lumped together into an averaged model segment. Therefore, lossy portions of channel material materials and fine details of any given physical structure must not be overlooked, rather must be obtained and scrutinized through extracted channel (3D) analysis. This puts further emphasis not only on the structure of individual channel segments, but on the materials and processes used to manufacture those structures. For example, for flex structures containing conventional adhesive-based bonding films, it is no longer acceptable to approximate the dielectric constant and loss tangent associated with the bonding film structure. Rather, the model developer must accurately depict both the adhesive and polyimide (for example)



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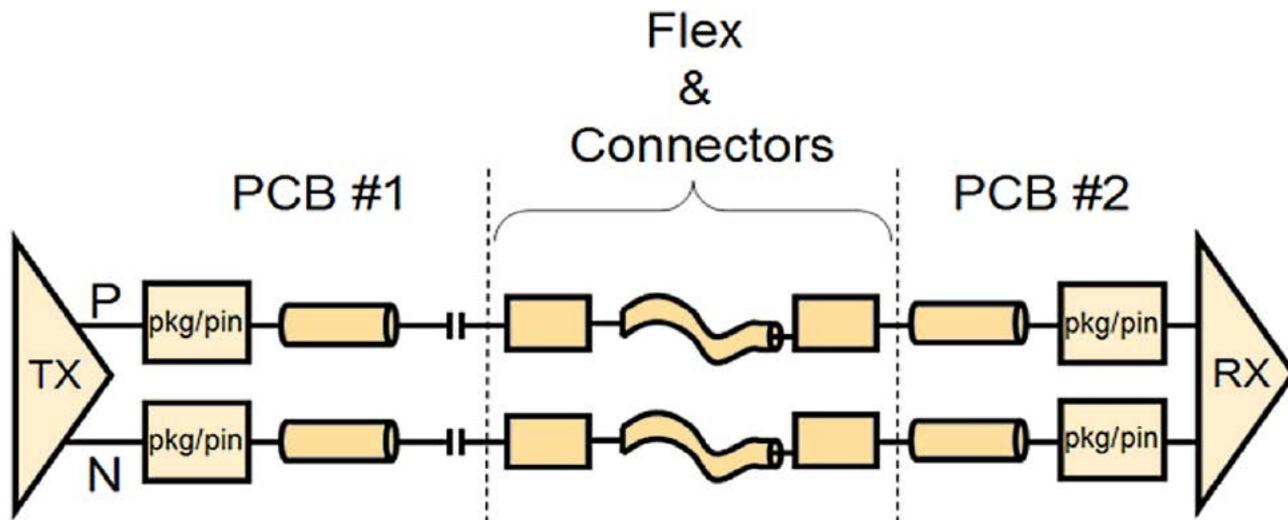


Figure 3: Example of a PCIe channel.

portions comprising the bonding film which is laminated to the signal layer.

Similar to the importance of modeling finite channel details, the progression of Figure 2 demands improved modeling and implementation of lower-loss interconnect materials.

Channels comprised of standard FR-4 PCBs and polyimide flexible circuits may be acceptable with data rates at 2Gbps using 100ps edges, for example. However, an attempt to reuse the same channel (and materials) at 6Gbps and 50ps edges may not realize sufficient margin at the receiver's input. For this reason, material improvements are just as important as reducing discontinuities within the frequency band of interest.

Flexible Interconnects: Typical Performance

Before discussing the details associated with enhancement of flex material performance, consider the following example PCIe channel containing two rigid PCBs (backplane and daughter cards) connected via a cabled interconnect solution (in this case a flex circuit).

The example PCIe channel of Figure 3 has been assessed in two fashions, first utilizing conventional flexible circuit channel materials and second, using low-loss flex materials, both of which are then compared against the PCIe external cabling specification⁴ shown in Figure 4.

The example PCIe channel assessment provides some initial insight into the electrical margin improvements available through the use of lower-loss flexible circuit dielectric materials. Channel insertion loss estimates, rendered from HSSCDR simulations (internally-developed IBM simulator), indicate that use of standard flexible circuit material enables specification compliancy under nominal conditions (temperature, voltage, impedance) through a flex length of 18 inches (all else held equal) but fails to meet interface specifications under all worst-case specifications. However, the same HSSCDR simulations provided evidence that utilization a new dielectric material (all else held equal) yielded spec-compliancy through all nominal and worst-case conditions through not only 18 inches of flex, but 20 inches of flex length.

Background and Fundamentals

Dielectric properties like permittivity and loss tangent have not been a large concern for designers of flex materials until recently. This is due to the fact that due to the nature of flex circuit applications, the primary way they are specified is using mechanical properties. Properties like elastic modulus and copper adhesion under flex loads have long been well understood figures of merit and differentiators between various product offerings. However, shrinking form factors and the need for three dimensional rout-

ZEN AND THE COLLABORATIVE ART OF DESIGNING FLEX INTERCONNECTS, PART 1 *continues*

Standard Flex Material; Nominal Conditions					Total Channel Loss (dB)	Budget (dB)	Margin (dB)
Flex Length (inches)	PCB #1	Flex	Connectors	PCB #2			
12.00	2.49	3.46	1.60	1.20	8.75	10.75	2.00
14.00	2.49	4.03	1.60	1.20	9.32	10.75	1.43
16.00	2.49	4.61	1.60	1.20	9.90	10.75	0.85
18.00	2.49	5.18	1.60	1.20	10.48	10.75	0.28
20.00	2.49	5.76	1.60	1.20	11.05	10.75	-0.30
Standard Flex Material; Worst-Case Conditions					Total Channel Loss (dB)	Budget (dB)	Margin (dB)
Flex Length (inches)	PCB #1	Flex	Connectors	PCB #2			
12.00	3.26	3.46	2.50	1.56	10.78	10.75	-0.03
14.00	3.26	4.03	2.50	1.56	11.35	10.75	-0.60
16.00	3.26	4.61	2.50	1.56	11.93	10.75	-1.18
18.00	3.26	5.18	2.50	1.56	12.50	10.75	-1.75
20.00	3.26	5.76	2.50	1.56	13.08	10.75	-2.33
Low-Loss Flex Material; Nominal Conditions					Total Channel Loss (dB)	Budget (dB)	Margin (dB)
Flex Length (inches)	PCB #1	Flex	Connectors	PCB #2			
12.00	2.49	1.52	1.60	1.20	6.82	10.75	3.94
14.00	2.49	1.78	1.60	1.20	7.07	10.75	3.68
16.00	2.49	2.03	1.60	1.20	7.32	10.75	3.43
18.00	2.49	2.29	1.60	1.20	7.58	10.75	3.17
20.00	2.49	2.54	1.60	1.20	7.83	10.75	2.92
Low-Loss Flex Material; Worst-Case Conditions					Total Channel Loss (dB)	Budget (dB)	Margin (dB)
Flex Length (inches)	PCB #1	Flex	Connectors	PCB #2			
12.00	3.26	1.52	2.50	1.56	8.84	10.75	1.91
14.00	3.26	1.78	2.50	1.56	9.10	10.75	1.65
16.00	3.26	2.03	2.50	1.56	9.35	10.75	1.40
18.00	3.26	2.29	2.50	1.56	9.61	10.75	1.14
20.00	3.26	2.54	2.50	1.56	9.86	10.75	0.89

Figure 4: Loss budget comparison.

ing have pushed flex circuits into a significant number of digital applications. The unavoidable trend caused by bandwidth demands pushes data rates higher.

Flex Circuit Copper Clad Laminates

Since most conventional flex designers are not well versed in high-speed material charac-

teristics, significant misunderstandings about the properties of flex materials have evolved (or devolved) over time. One of these unfortunate false conclusions is “Polyimide is a lossy material.” This would be akin to making the statement “All rigid materials are lossy.” It would be self-evident to any flex designer that a wide variety of adhesive systems can be used to make

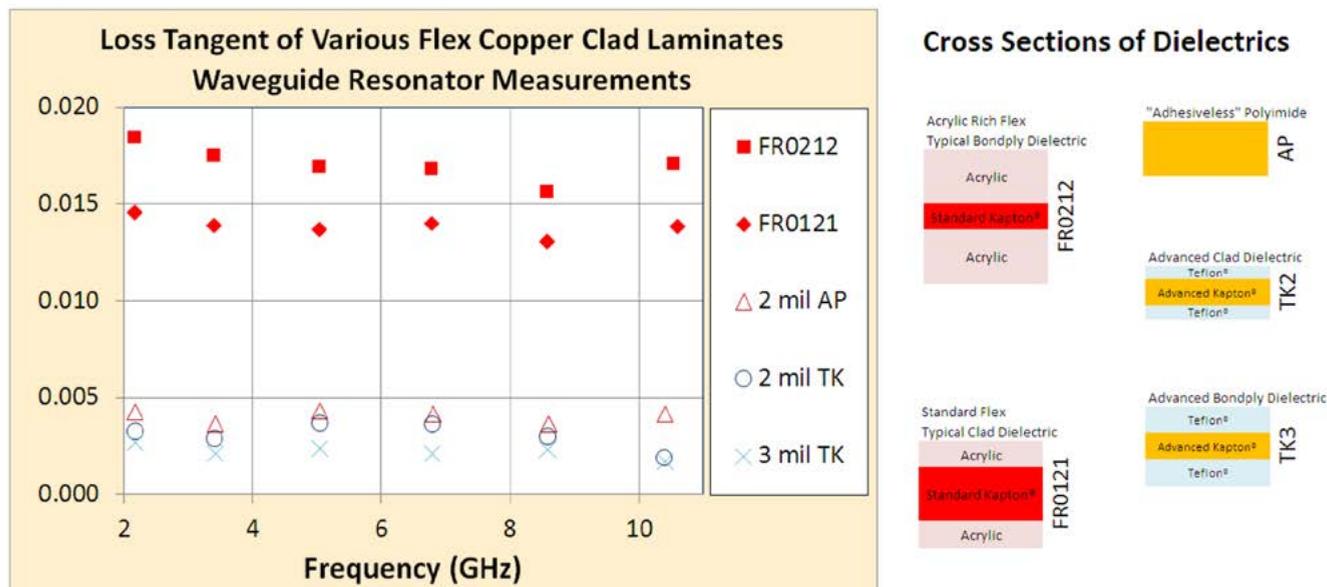


Figure 5: Summary of loss tangent measurements of flex laminates.

rigid laminates and therefore a wide variety of electrical properties. Likewise, there are a wide variety of flex materials available.

Previous work has shown that the core and bonding materials used to make flex copper clad laminates vary widely in dielectric loss^{4,5}. Figure 5 shows a range of commercially available materials containing polyimide. Notice that the conventional flex materials shown in red and pink have significantly higher loss tangent values than products free of acrylic adhesive. Polyimides optimized for high speed applications have significantly lower loss tangent values than products containing acrylic adhesives. Advanced flex materials have been developed that utilize Teflon® thermoplastic to further decrease the dielectric loss⁶.

The behavior of “standard” versus “advanced” flex materials is similar to that demonstrated by similar categories for rigid materials. Previous measurements of the impedance of signal lines has shown that flex materials behave in a similar way to rigid materials for basic microstrip structures. Just like for advanced rigid materials, advanced flex materials demonstrate lower permittivity, which is advantageous for signal integrity. Figure 6 summarizes the difference between 2 and 4 mil thick dielectrics of standard FR-4 (FR), Megtron 4 (M4), Megtron

6 (M6), Adhesiveless Flex (AP), and Advanced Flex (TK)⁶. The numbers behind each clad identifier are the dielectric thickness in μm .

Properties of Flex Materials

Dielectrics used to make flexible circuit clad and bondply are manufactured in a fundamentally different way as are rigid materials. Flex materials do not use woven or random glass as reinforcement. Instead, dielectrics obtain their strength from polyimide (or Kapton®) films⁸. This has significant implications for signal integrity. There is no “fiber weave” effect resulting from the fiberglass reinforcing material content found in conventional rigid card materials. This of course provides both electrical advantages because high-frequency electrical discontinuities are reduced while at the same time greater mechanical flexibility is enabled. However, flex designers often utilize non-solid or “meshed” ground planes like that shown in Figure 7 to enhance mechanical flexibility. These hatched ground planes significantly enhance mechanical flexibility, but introduce several parasitic electrical elements. These include potential Z-axis crosstalk, non-TEM wave propagation, increased insertion loss, opportunity for EMC concerns and depending upon percent copper-fill, potential for decreased ESD immunity.



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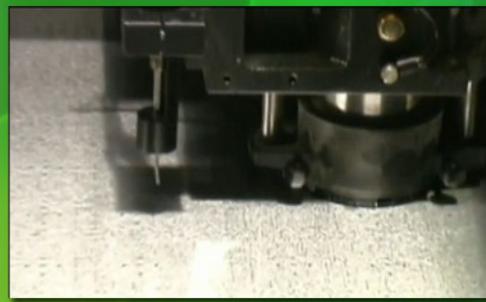
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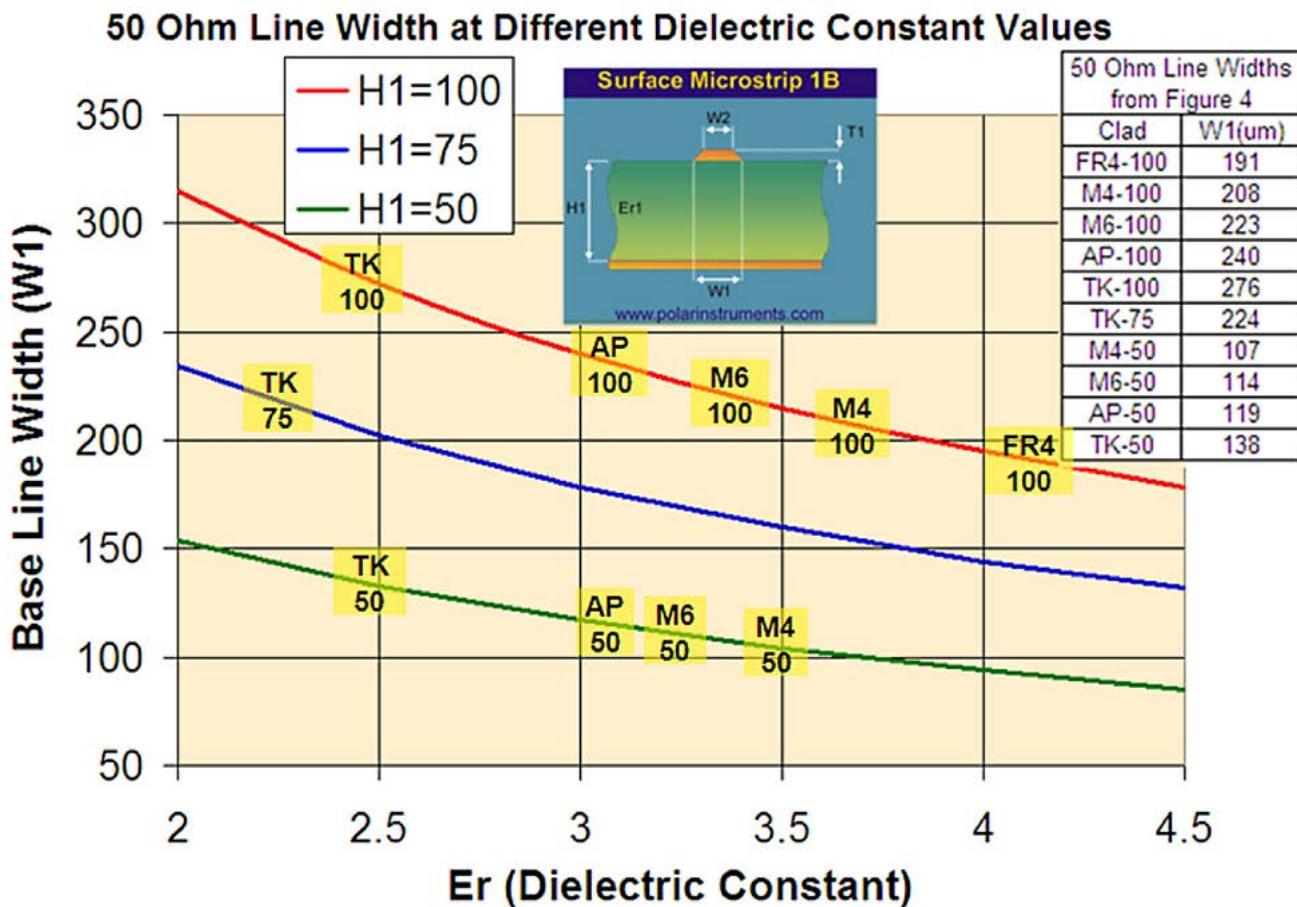
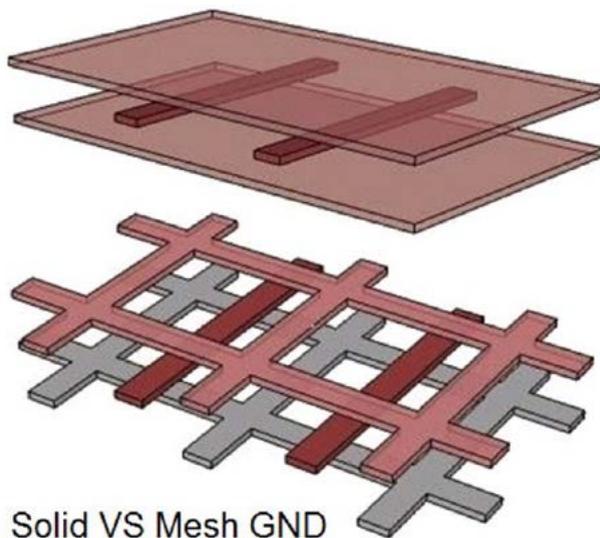


Figure 6: Comparison of flex to rigid copper clad laminates⁷.

Since flex materials obtain their mechanical reinforcement from Kapton® instead of glass, the grade of Kapton® and associated adhesives must be chosen carefully with respect to the target application. Standard grades of Kapton® used acrylic based flex materials have higher dielectric loss and are more absorb more moisture. This can be quite significant factors in high-speed or high-frequency designs.

Stripline constructions are generally preferred over microstrip to maximize signal integrity. When utilizing this structure it is implicit that more materials are involved than a copper clad laminate. Adhesives are required to bond copper clads together. Standard flexible adhesives are generally very lossy. Figure 8 summarizes the loss tangent of some of the materials used to make flexible copper clads and bonding/cover



Solid VS Mesh GND

Figure 7: Solid versus meshed ground plane.

Loss Tangent of Component Flex Materials: Waveguide Resonator Measurements

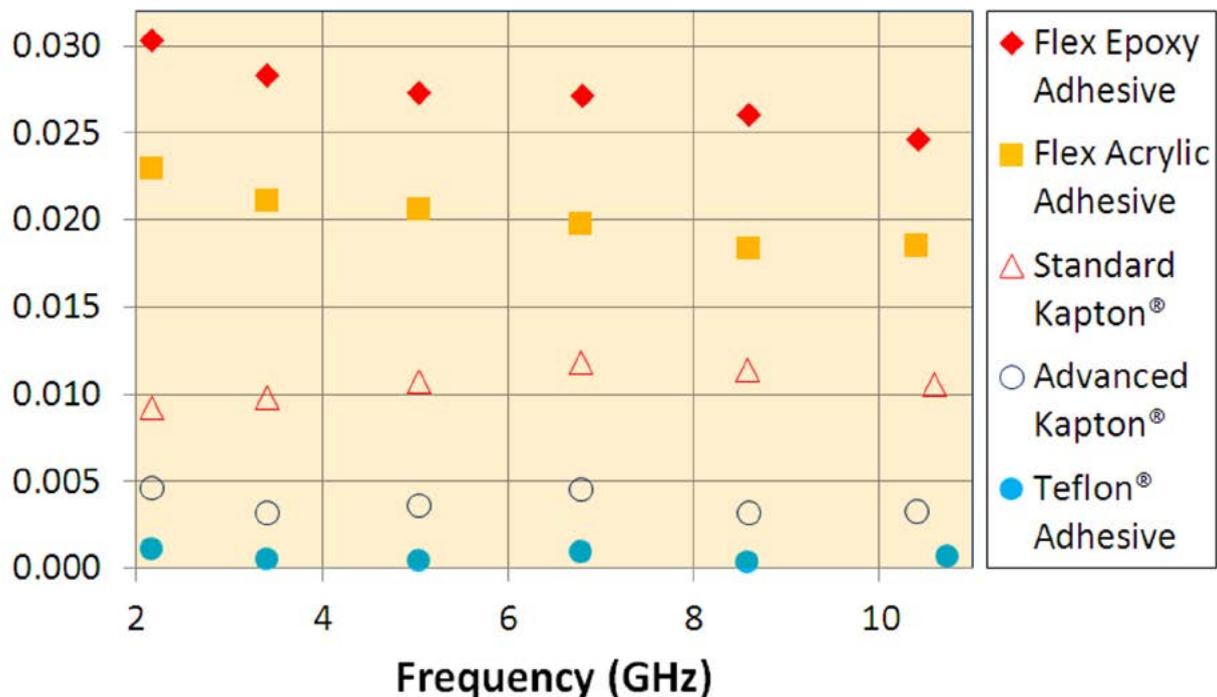


Figure 8: Loss tangent measurements of dielectrics used in flex circuits.

films. First note that the difference between Standard Kapton® and Advanced Kapton® is significant. There are specific polyimide formulations that have minimal loss and moisture absorption that are utilized for high-speed products like Pyralux® AP and Pyralux® TK. While the benefit of these improved polyimide formulations is significant, the largest source of loss in a flexible circuit stackup is the acrylic adhesive. Both acrylic adhesives (popular in North America) and epoxy adhesives (popular in Asia) have much higher dielectric loss. Since the acrylic is usually in contact with ground and signal lines, the relative effect of this high dielectric loss is magnified. The degradation of signal due to acrylic significantly limits the utility of flex circuits at high speeds.

Design of Test Vehicles

A well designed test vehicle panel can provide a broad range of samples and coupons to gather key data on potential new materials and

conventional materials for comparison such as manufacturability, yield, dimensional stability, impedance, other signal integrity properties, and reliability. The panel size chosen for our test vehicles was 18" x 24". This was chosen as it is a common panel size used in multilayer flex production. Our panelization contained single ended impedance/insertion loss coupons across a broad range of line width ranging from 2 to 9 mils. Specific line widths for which we had significant historical data from standard materials on production parts were included. Three pair NEXT/FEXT differential coupons at target line widths/spaces were included to provide loss and crosstalk data. To obtain differential impedances across a range of line widths and spaces, stair-stepped differential coupons with various line width/spaces were created. Short pulse propagation coupons were added.

Via arrays were added to provide samples for in process cross sectioning. These were used,

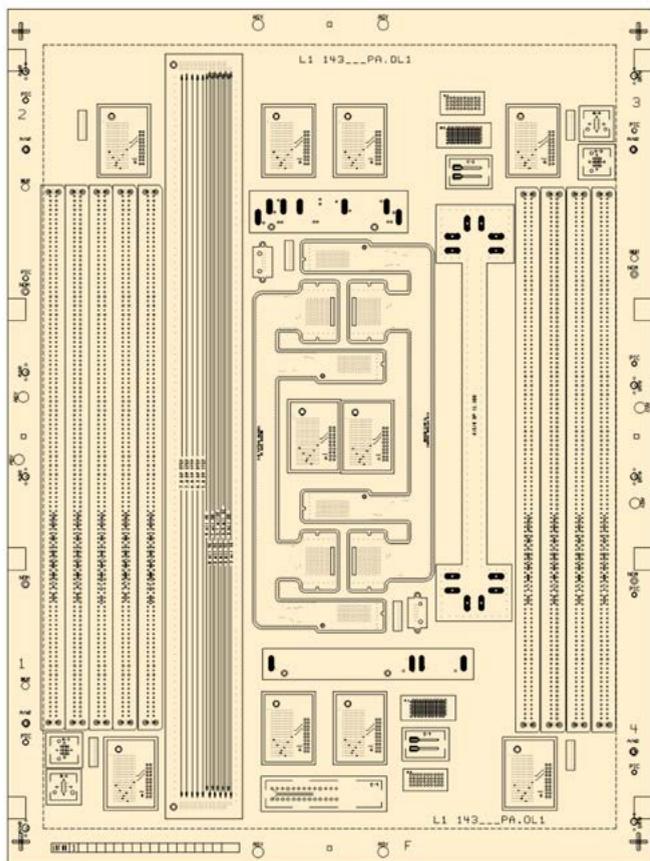


Figure 9: Panelization of test vehicles.

for example, to check hole quality after copper plate. Registration ladder coupons were included on the four corners of the panel and near the center to evaluate dimensional stability of material sets. IPC solder float coupons were added to provide cross-section compatibility data with ECAT processing.

Connector footprints including single-ended VHDM® and differential Impact™ connectors were included to get build experience with various connector footprints and wiring design rules^{9,10}. These coupons were also used for in process monitoring and solder float evaluations. Although the flex materials used in our evaluations lack glass weave which is a key driver of IR issues in rigid boards, IR coupons were added to confirm the new materials do not have IR issues.

Coupons for via reliability testing by accelerated thermal cycling (ATC) were added to the panel. A coupon that tests through-hole reli-



Figure 10: ATC construction.

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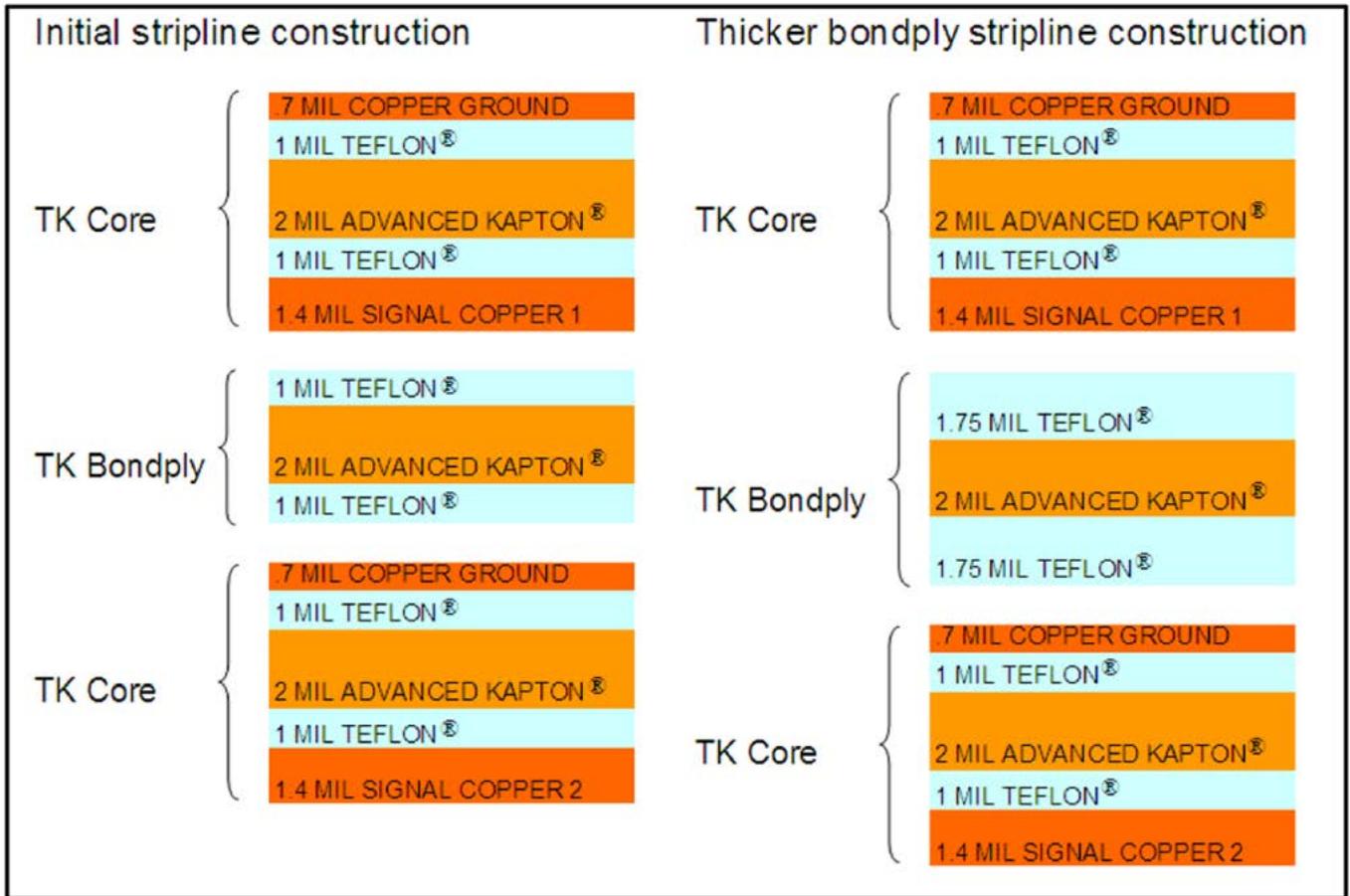


Figure 11: TK stripline constructions.

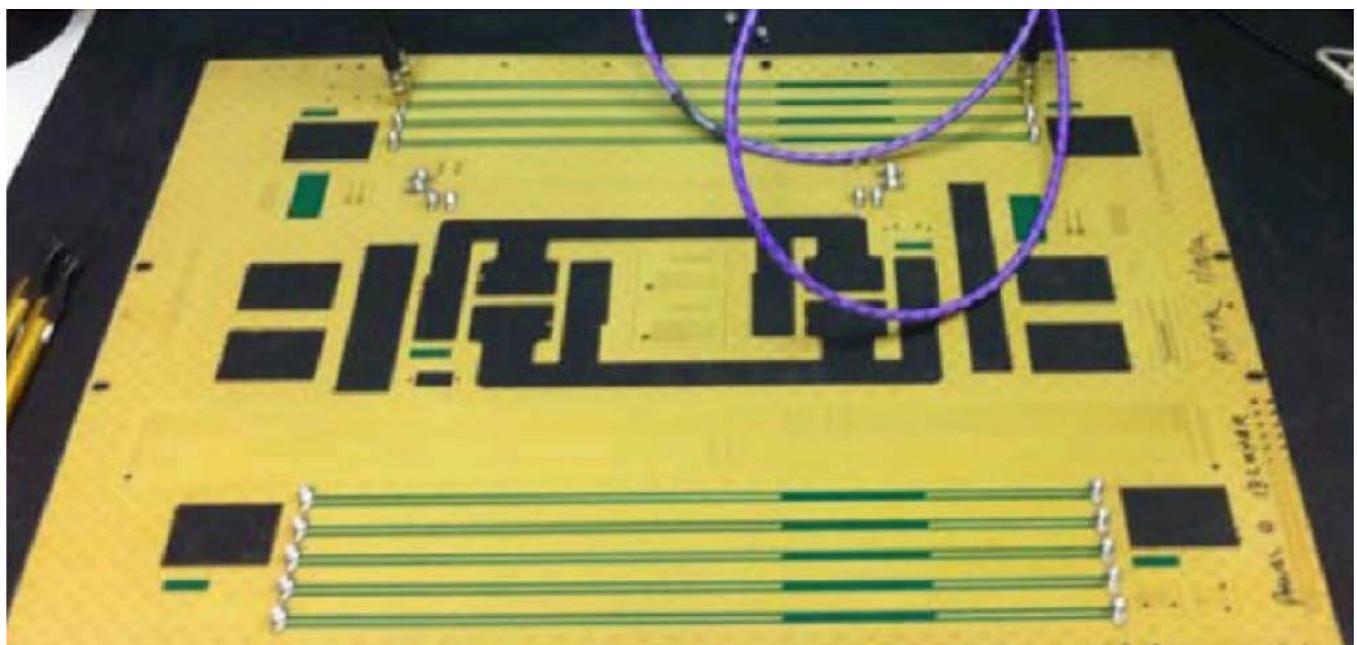


Figure 12: 13-layer panel with 8 ATC and other coupons removed.

ability (top to bottom layer) and interconnect reliability (signal to via) was included. Each ATC coupon tests 160 vias or part of vias for through-hole reliability and 316 interconnects. Coupon hole size is 16.6 mils finished.

Finally functional versions of current production parts were included in the panelization to provide samples for mechanical and system performance comparison to existing standard production multilayer flex assemblies. The resulting test panelization used is shown in Figure 9.

Initial builds for lamination evaluations and SI coupons used the core stripline construction shown in the left side of Figure 11. Builds were migrated to the thicker bondply shown in the right side of this figure to improve SI properties and reduce propensity for air entrapment. One to five signal layer constructions were built.

ATC coupons were built on a 5 signal layer-thick bondply stackup as shown in Figure 10 and Figure 12.

Part 2 of this article will appear in the July 2013 issue of The PCB Design Magazine.

This paper was presented at DesignCon 2013. **PCBDESIGN**

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10. Impact is a trademark of Molex.

Glenn Oliver is currently the principal engineer responsible for characterization of electrical properties of materials for high-frequency applications. His work background includes eight years in photonics research and development followed by nine years in RF/microwave development and applications. He can be reached at glenn.e.oliver@dupont.com.

Matt Doyle has 13 years of experience in 2D & 3D modeling and signal integrity working within IBM's Systems & Technology Group. One of his specialties is designing high-speed, flexible interconnect solutions for IBM Power systems, as well as for supercomputer, consumer-electronics, medical, and aerospace & defense applications. He can be reached at doylem@us.ibm.com.

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John Dangler is a development engineer at IBM with extensive experience in flex cables. He is responsible for design, qualification, sourcing and quality engineering for flex and rigid-flex implementations. John has 18 patents issued or filed related to electronic packaging. He can be reached at jdangler@us.ibm.com.

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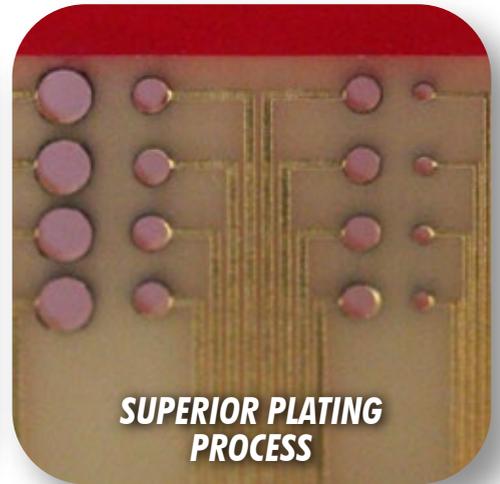


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Solid Rigid-Flex Design Eases System Assembly

by **Amit Bahl**
SIERRA CIRCUITS

A straight line is not always the shortest route between two points in electronic products: Thanks to rigid-flex PCB architecture, circuits can be folded onto themselves with 180° bends—superimposed at minimum height—thereby shrinking product dimensions. Moreover, rigid-flex construction conserves the board territory that cable connectors would otherwise consume, improves system reliability by eliminating connector solder junctions, tightens impedance control, and greatly increases the number of potential paths for board I/O compared to coaxial flat cables. Furthermore, if a product has moving sections with electronics embedded, rigid-flex construction is the ticket.

Credit rigid-flex architecture for the existence of smartphones and other pocket-size electronic wonders. There's simply no alternative for stuffing that much functionality into such a small space. However, to realize the advantages of rigid-flex construction (including lightweight assemblies) certain design constraints apply specifically to the flex layers in a stackup. Do not attempt your first (or second, or third) rigid-flex design before you consult your prototype manufacturer.

Unlike a conventional PCB stackup, foil construction cannot be used for flex layers. The flex

layers in a rigid-flex assembly are built from unreinforced base substrates typically consisting of polyimide dielectric film, clad with rolled annealed copper. The rolled copper is much more flexible than the copper used for rigid boards, but it cannot be plated without becoming brittle. Therefore, the clad base material is first drilled, holes are selectively plated, then the traces and pads are etched. Bondply, a layer of polyimide film with adhesive coating on both sides, isolates that conductor layer from the next, and so forth. A cover layer of adhesive polyimide film insulates and protects the top and bottom surfaces of the flex stack along the ribbon that extends between rigid board sections.

Flex materials are elastic under all circumstances, including processing. During the final lamination of the rigid-flex stack, they are less dimensionally stable than the rigid core and prepreg materials that sandwich them. Hole-to-copper clearance must be greater than the minimum possible with a rigid-only stackup, ideally at least 10 mils. Vias must be farther from the edge of the rigid area adjoining the flex ribbon than the minimum distance in rigid-only stacks, preferably at least 50 mils from the edge, but certainly no less than 30 mils. This rule is the one most violated in rigid-flex designs.





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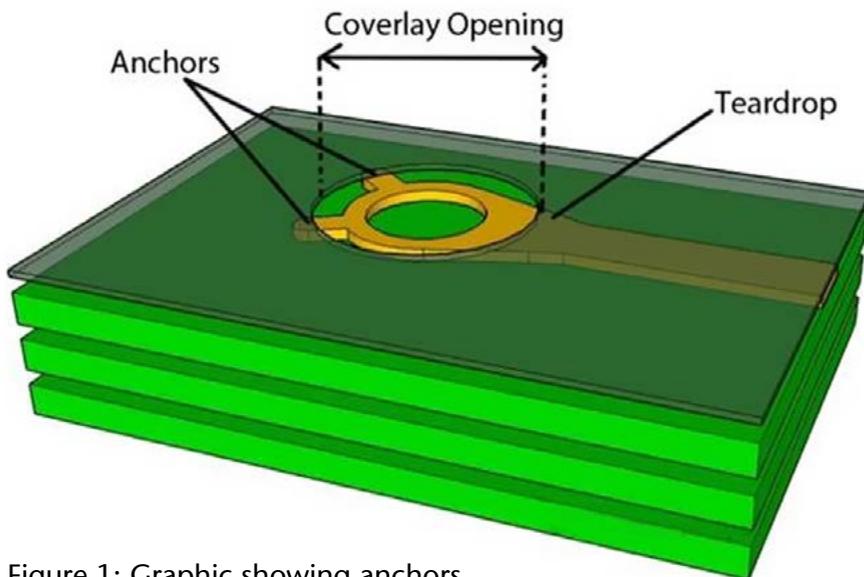
SOLID RIGID-FLEX DESIGN EASES SYSTEM ASSEMBLY *continues*

Figure 1: Graphic showing anchors, coverlay opening and teardrop-shaped transition from annular ring to trace.

Seek guidance to develop your stackup and design rules. Differing coefficients of thermal expansion among the flex base material, adhesives, prepreg, and rigid cores requires a very careful balance of thicknesses, especially for impedance-controlled designs. There can be many layers of flex in a rigid-flex design, depending on the bend radius of the ribbon portion and whether it will remain stationary after assembly. Flex layer count must be limited in dynamic applications. Consult your manufacturer. If more than four flex layers are required, bonding adhesive must be absent in the sections that are designed to bend. The bend radius should be no less than 12 times greater than the circuit thickness.

Trace routing in the ribbon area should be curved, not angled, to increase peel strength. This recommendation is opposite the routing practice for rigid boards. To increase ribbon flexibility, planes should be cross-hatched; however, the cross-hatch complicates impedance control. Again, a careful balance is required. In some applications, a wide, solid strip under critical traces suffices. Traces on different layers should be staggered vertically, not placed atop each other, to increase ribbon flexibility.

Annular rings should be as large as possible in flex-only regions to reduce the risk of peel-

ing, and the transition from the annular ring to the trace should be teardrop-shaped for the same reason. Adding tabs or anchors (Figure 1) also helps to prevent peeling.

Traces should always be perpendicular to the fold in the flex areas that will be bending. Where flex ribbons have sharp interior corners, tear stops should be added. Copper can be incorporated during layout at the elbow of those corners for reinforcement or polyimide stiffeners can be specified for the inside corner radii. The stiffeners can be laminated when the covercoat is bonded and are the preferred method to prevent tears. The best strategy is to avoid using

sharp corners in a flex design.

A very basic checklist for rigid-flex designs includes these routing considerations:

- Stagger flex traces vertically layer to layer
- Turns should be gradual
- Vias should be no closer to the edge of the rigid board than 30 mils at the flex transition
- Minimize flex layers

Remember, rigid-flex PCB designs may be expensive to fabricate, but they can save costs during system assembly. Such architecture often is the only way to squeeze the required product functions within the target package volume. The earlier you consult a PCB manufacturer during product definition, the better your results. **PCBDESIGN**



Amit Bahl directs sales and marketing at Sierra Circuits, a PCB manufacturer in Sunnyvale, CA. He can be reached by [clicking here](#).

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High-Frequency Flexible Circuits

by John Coonrod

ROGERS CORPORATION, ADVANCED CIRCUIT MATERIALS DIVISION

Flexible circuits, as a family of products, come in many variations. There are the more traditional flex circuits that are low layer-count, very flexible, used in dynamic motion applications and static scenarios. The static case is generally an application of a one-time bend, where the circuit is formed to a shape in the assembly and then it never has to flex again. In dynamic applications, the circuit must continually flex during the product's lifecycle, such as a read-write flex circuit inside of a hard disk drive.

Rigid-flex circuits have the ability to join multilayer rigid PCB technology with flexible circuits. Think of this concept as having flex circuit layers built into a multilayer PCB. The rigid areas are typically a FR-4 type material and the flex layers are polyimide-based materials. Rigid-flex offers the best of both worlds but can be problematic for manufacturing and reliability issues. Over the years, manufacturers of rigid-flex have fine-tuned the technology to where the manufacturing and reliability issues are well understood. Now, rigid-flex can be made effectively and with very good reliability.

Flexible circuit materials offer great properties for the typical end-use application. However, they do have natural limits, as all materials do. A few potentially limiting properties, at least for some applications: relatively high moisture absorption, poor thermal conductivity, high CTE (coefficient of thermal expansion),

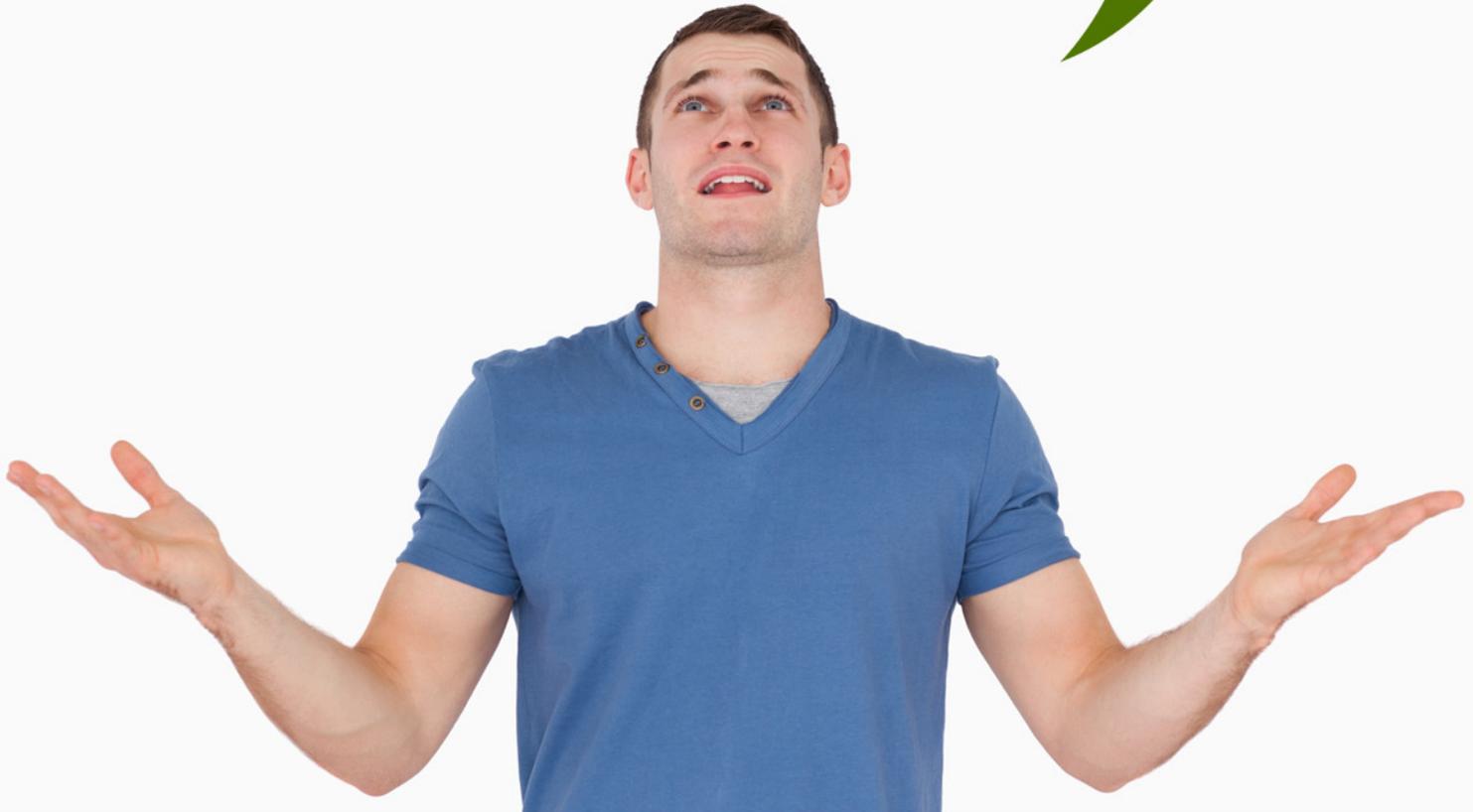
low T_g , and poor dissipation factor. But with a wide range of polyimide films and adhesives now available, many of these issues can be addressed through a thoughtful combination of materials for the flex circuit construction.

Even with the most innovative selection of customary flexible circuit materials, one issue stands alone and that is poor performance with high-frequency applications. There are applications where flex circuit technology could offer a major advantage if the circuit had good electrical performance at high frequencies. What is meant by high frequencies? Well, the answer to that question is a bit subjective depending on your reference frame, but at 2.5 GHz, 5.8 GHz, 18 GHz, 24 GHz, 60 GHz and 77 GHz, flex circuits could be beneficial. Traditional flex materials have been used in the frequency range of hundreds of megahertz and even stretching beyond one gigahertz. Typically, traditional flex circuits struggle to have good electrical performance above 1 or 2 GHz due to high dissipation factor and the associated losses. There are some exceptions that may allow flex circuits to extend to the 2.5 or possibly 5.8 GHz, but there is no hope for 24 GHz using traditional flex materials.

Some materials are formulated for high-frequency applications, where the frequencies mentioned are not a concern and some of these materials have flexible properties. In general,



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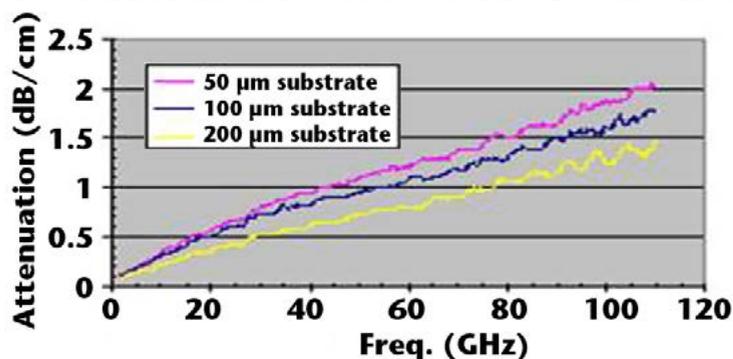


Figure 1: LCP loss performance over an extremely wide range of frequencies from a study^[1] done by the Georgia Institute of Technology.

a material can be used for flexible circuit applications when the material is thin, modulus is relatively low, there is no woven glass reinforcement and the copper type used has good flexibility. Some of the thin PTFE-based circuit materials can and have been used in flexible high-frequency circuit applications.

One application was the 5 mil thick RT/duroid 5880® laminate used in a positioning arm, with high-frequency circuitry at the end of the arm. This was a dynamic application, and given the large bend radius, there was less strain on the circuit during the flexing motion, which allowed better flex life. The RT/duroid 5880 substrate is a nearly pure PTFE laminate with a small percentage of filler, which helps to reduce the CTE and there are no woven glass layers. The rolled annealed copper has been proven in innumerable flex circuit applications to be the copper type of choice for flexibility. An additional benefit of the rolled copper is the very smooth surface that helps to minimize conductor loss. This type of loss will be a major contributing factor for overall insertion loss, given a thin circuit that is operating at high frequency.

There are other materials to consider as well. Liquid crystalline polymer (LCP) has been known for decades to be an extremely good material at the highest RF frequencies and it is flexible. The ULTRALAM 3850® laminate is based on thin film technology, with no woven glass, and low modulus. This is available with a cop-

per that is very flexible. This material is being used in many high-frequency applications and the graph shown in Figure 1 demonstrates very low loss (low attenuation) at high frequencies.

There have been rigid-flex circuits made using LCP flexible circuit layers combined with rigid high-frequency laminate layers. This is an excellent combination for a circuit with high utility, excellent high-frequency performance, flexibility and the ability to minimize the electrical transitions from the rigid circuit to the flex. If the rigid-flex was made as a separate rigid board and flex circuit, the connectors between these circuits can alter the electrical performance significantly.

Rigid-flex design has more freedom to adjust the electrical transition from the rigid portion of the circuit to the flex portion, and this allows a better signal propagation, less EMI issues and overall improved performance.

When considering a flexible circuit application which needs good high-frequency performance, there are many more material choices than the traditional flexible circuit material. These other materials are often not considered for flex applications because of a mindset and not necessarily due to flexible performance issues. It is always recommended that the circuit designer consult their materials supplier when considering a new application and explore many options that may not be apparent. **PCBDESIGN**

References

1. Thompson, Kirby, Papapolymerou, Tentzeris, "W-Band Characterization of Finite Ground Coplanar Transmission Line on Liquid Crystal (LCP) Substrates", IEEE Polytronic Conference 2003.



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Cohesive Failures

by Paul Reid

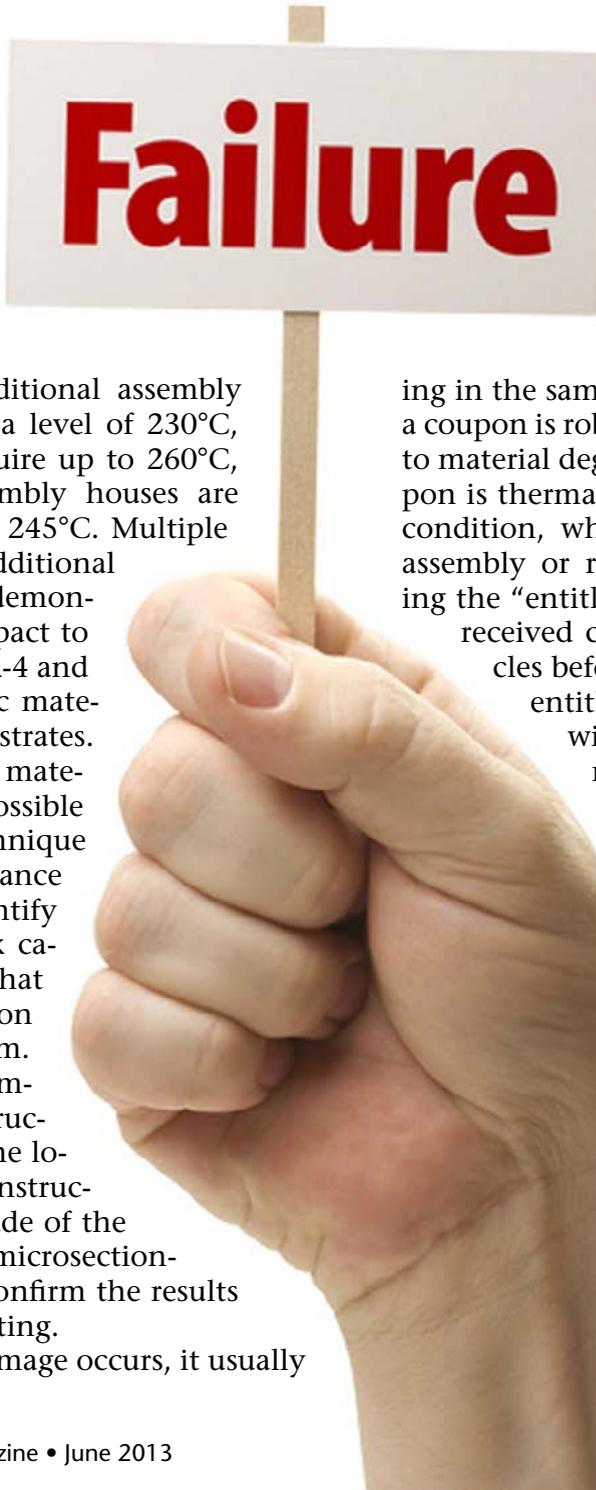
Since the advent of the European Union's legislation for Restriction on Hazardous Substances (RoHS), lead has been banned from use in solder in surface finishes and pastes used in the PWB assembly process. The alternative metals and alloys to traditional tin/lead (Sn/Pb) solder required that the assembly temperatures be increased to achieve the higher melting point of the lead-free solders. The traditional assembly temperature reached a level of 230°C, but lead-free can require up to 260°C, although many assembly houses are using a more modest 245°C. Multiple exposures to the additional 15°C to 30°C has demonstrated a negative impact to the integrity of the FR-4 and halogen-free dielectric material used in PWB substrates. Quantification of material damage is now possible through a new technique that utilizes capacitance measurements to identify specific levels of bulk capacitance change that signify degradation within the resin system. This technique was employed to non-destructively identify both the locations within the construction and the magnitude of the change. Traditional microsectioning is completed to confirm the results of the capacitance testing.

When material damage occurs, it usually

extends thermal cycles to failure, frequently giving false positive artifact results. Adhesive delamination and cohesive failures, however, can reduce the thermal cycles to failure. The crack may propagate starting in the epoxy and go through the copper in the barrels of the PTH, reducing the thermal cycle to failure, but this is a rare condition.

Most of the time, the crack stops when it gets to the copper of the PTH. If one does thermal cycle testing and does not include material testing in the same coupon, it is easy to deem that a coupon is robust when in fact it has failed due to material degradation. Consider that the coupon is thermal cycle tested in an "as-received" condition, which is without a simulation of assembly or rework (preconditioning), as being the "entitlement" of the coupon. If the as-received coupons achieve 500 average cycles before failure, then 500 cycles is the entitlement that this coupon design, with that specific construction and material, achieves. The cycles to failure of the coupons that are tested as-received are as good as can be expected and as a simulation of assembly and rework becomes more aggressive, there is an increasing reduction of the cycles to failure.

Consider the data given in Figure 1. Exposing coupons to a simulation of assembly (3x) or assembly and rework (6x) preconditioning degrades the entitlement as the tem-





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COHESIVE FAILURES *continues*

	Control	Sn/Pb Reflow		Low Temp Pb/Free		High Temp Pd/Free	
Precon	As Rec	3X230°C	6X230°C	3X245°C	6X245°C	3X260°C	6X260°C
Cycles of Failure without Material Damage							
Percent of Entitlement	100%	80%	60%	75%	55%	70%	50%
No Material Damage – Average Cycles to Failure	500	400	300	375	275	350	250
Cycles of Failure with Material Damage							
Percent of Entitlement	100%	80%	60%	80%	85%	90%	100%
Material Damage – Average Cycles to Failure	500	400	300	400	425	450	500

Figure 1: Cycles to failure with and without material damage.

perature or the number of cycle is increased. In this example, coupons exposed to 3x230°C preconditioning typically degrades the entitlement by 20% so we expect the cycles to failure to drop to 400. If we drop below 400 cycles to failure, for example, to 350, then we become concerned that there is a processing problem like thin copper or interconnection smear. What we expect is a reduction of 45% of the entitlement for coupons that are preconditioned 6x245°C and 50% for coupons preconditioned 6x260°C. This works when there is no material damage occurring in the coupon. Without material damage, we see that the higher the preconditioning the less thermal cycles to failure that a coupon achieves.

With material damage, the coupons that survived 6x260°C preconditioning may survive to the same numbers of cycle to failure (or a higher number) as the coupons that were tested as received. That a coupon could become stronger as it is preconditioned with a higher temperatures and number of cycles is counterintuitive. We find is stress-relieving material damage, artificially extending cycles to failure, is a common occurrence.

Back in 2004, when we started to test coupons with 6x260°C preconditioning, we were finding extended cycles to failure. This is why we had to find a way to determine if there was material damage in the coupons independent of the cycles to failure data. We decided to

measure capacitance changes in the coupons between ground planes. After a significant amount of testing, we found that a 4% reduction in capacitance in our IST test coupons usually reflects material damage. What we currently do is a cross-section of the coupons that show a 4% reduction in capacitance to confirm or refute material damage.

The method was time-consuming, as we had to probe two adjacent ground planes by hand

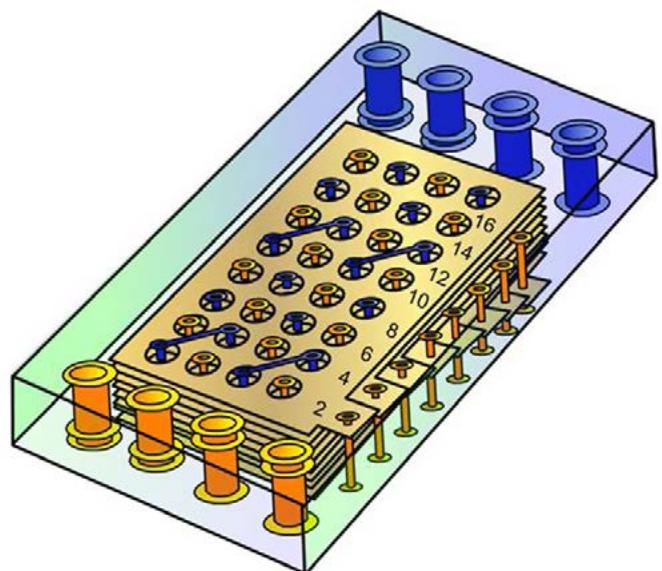


Figure 2: The capacitance layers in an 18-layer IST coupon.



Figure 3: A DELAM tester.

and record that data in a spreadsheet. In a six-layer board we have three ground planes (2, 4, and 5) which requires only two readings. Figure 2 shows the capacitance layers in an 18-layer coupon at layers 2, 4, 6, 8, 10, 12, 14, and 16. This coupon requires seven measurements. In one 52-layer design we have 28 holes that require manual probing of 27 pairs of holes. This could take up to 10 minutes to measure and record the 52 layer coupon manually. What we do is measure the capacitance on the coupon as received and then compare those readings to readings measured after preconditioning and at end of test. We test hundreds of coupons per month and this manual effort is significant.

In order to relieve this burden what we did was develop the dielectric estimation laminate assessment method (DELAM). This bed of nails

tester measures the capacitance between adjacent layers. The coupon slips on to alignment pins then you close the “clam shell” fixture and the tester measures and records the capacitances automatically. What this equipment does is measure capacitance between two holes at the rate of 63 pairs of holes in 30 seconds with a greater accuracy than the hand method.

Measured manually or automatically, we find is that frequently lead-free preconditioning causes material damage. We see that, if the material is weak, two or three coupons (sometimes every coupon) will fail in a group of eight. If the material is robust there will be no failures in a group of eight coupons. We then select the coupon that shows the most damage and cross-section it to confirm or refute the presence of material damage. If we find material damage in the cross-section, then we keep the -4% threshold. If we do not find material damage we increase the threshold of -6% or -8% change. Using these techniques, we are able to accurately find and understand material damage.

Cohesive fractures are cracks that occur in the dielectric, not at the laminated interface like we see in adhesive delamination. The crack may propagate through the B-stage, C-stage and glass bundles and possibly go around copper pads. In cohesive failure the cracks may propagate vertically and are not limited to laminated surfaces. This crack occurs within the epoxy substrate. This fracture may initiate during the heating of the coupons but it appears to expand



Figure 4: Close up of the bed of nails in the DELAM tester.



Figure 5: Cohesive crack.

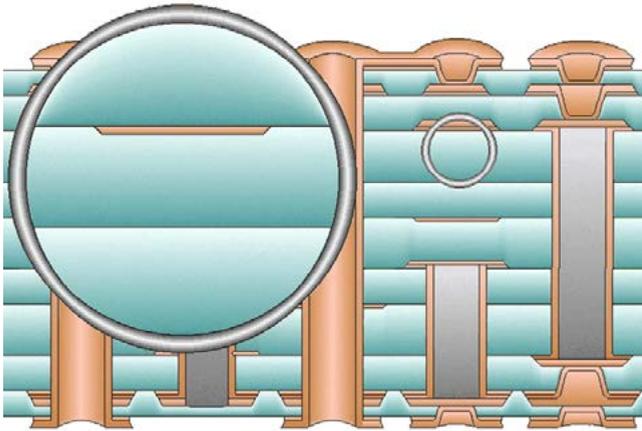
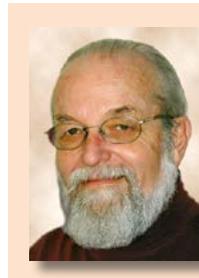
COHESIVE FAILURES *continues*

Figure 6: Animation of cohesive failure [click here](#).

during the cooling cycle. In a cohesive failure, the cracks may bifurcate and branch ending number of points.

Notice in the animation that the crack occurs during the heating cycle but expands at the beginning of the cooling cycle. It appears

that this type of crack occurs due to an aging of the dielectric system. What is thought to happen is that the epoxy is cross-linking to a greater degree due to the elevated temperature of the preconditioning. This increase in cross-linking increase the strain of the epoxy system until the strain is greater than the mechanical strength of the epoxy crosses links. Unlike adhesive failure which tends to be a delamination where volatiles tend to increase in pressure causing the failure to be “blown apart,” it appears that with a cohesive crack the epoxy literally pulls itself apart. Watch the animation of a typical cohesive failure in Figure 6. **PCBDESIGN**



Paul Reid is program coordinator at PWB Interconnect Solutions, where his duties include reliability testing, failure analysis, material analysis, and PWB reliability consulting. To contact Reid, [click here](#).

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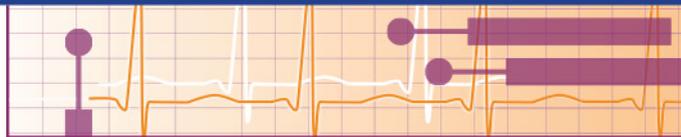
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News Highlights



Board Bookings in North America Up 22% in March

Compared to the previous month, shipments in March increased 20%, and bookings grew 22.2%. The book-to-bill ratio for the North American board industry continued to strengthen in March, reaching 1.08.

Viasystems' Sales Up 4.1%; Still Feeling Effects of Fire

"While resulting net sales and earnings for our first quarter were in line with stated expectations, our Guangzhou, China operations struggled to recover from last year's fire as quickly as we had planned. The shortfall in earnings from the Guangzhou operations was offset by reduced variable expenses such as travel and incentive compensation in the quarter," said company CEO David M. Sindelar.

TTM's Q1 Sales Down 14.8% On-Quarter

"Our results for the first quarter for both Asia Pacific and North America were in line with our expectations," said Kent Alder, CEO. "While we experienced normal seasonality during the quarter, we were pleased to realize a year-over-year increase in revenue due to increased sales in our cellular phone and networking end markets."

Automotive, Industrial Sectors Drive PCB Industry Growth

Increased consumer demand will aid the PCB and electronic component manufacturing industry in a big way. "Due to a mounting need for energy savings, the automotive and industrial sectors are increasingly using electronics, which is driving growth in demand for this industry's products," says IBISWorld Analyst Andrew Krabepetcharat.

Endicott Interconnect CEO Jay McNamara Steps Down

Endicott Interconnect Technologies, Inc. (EI) has announced that CEO Jay McNamara retired as of Friday April 12, 2013. He had been the president and CEO of Endicott Interconnect since its inception in 2002 as a divestiture of IBM's Microelectronics Division.

Invotec Expands Technical Team

As part of the continuous improvement process, Invotec Group is adding to its technical team at their Tamworth facility. "Responsibility for product and process is being split, which will provide a greater focus to ensure we continue to deliver the highest levels of customer satisfaction through exceptional service, technology, performance and reliability," commented Chris Haley, operations manager.

New IPC Certification Program Protects Intellectual Property

"The protection of intellectual property is very important to our industry, but until now wasn't uniformly defined," said Michael Moisan, VP of global technology, TTM Technologies. "IPC's new Intellectual Property Protection Certification Program is designed to help improve facilities' programs and ultimately get them certified to a universally-recognized standard."

China Drives Development of Global PCB Industry

China has become the country that enjoys the largest PCB output value and the fastest growth speed, and also the main driving force to promote the development of the global PCB industry. In 2012, there were 791 PCB enterprises with above designated scale in China with the market scale exceeding CNY 250 billion.

Hop on the Embedded Components Bandwagon

The complexity of PCBs is poised for a significant change as embedded components become more common. But developers who want to gain the benefits in size and performance of embedded components need to understand several critical points before joining in this new trend.

Aspocomp Reports 23% Sales Drop in Q1

Sami Holopainen, CEO, said, "At the beginning of 2013, demand remained as weak as it had been throughout the second half of 2012. There were, however, cautious signs of recovery to be seen, with the exception of the telecommunications sector. Our net sales decreased clearly from the comparison period, but remained on a par with the previous quarter at EUR 4.9 million."

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Right-Angle Bends in PCB Traces

by Jack Olson, CID+

Sooner or later in your career as a circuit board designer, the subject of right-angle bends in trace routes will come up. This discussion has a long history, because the best solution for a 90-degree bend is a “mitered” corner. This removes the impedance discontinuity, but is difficult to accomplish in most PCB layout software. So, how important is it?

I decided to ask the members of the long-running Signal Integrity Listserv (SI-LIST) about right-angle (90 degree) routing, and received some valuable responses. Here is an excerpt from the edited-for-clarity thread on right-angle bends:

Original question posed by columnist and board designer Jack Olson:

I may never understand why people use square corners in their models when they want to experiment with this subject. Are we talking about 90 degree bends or drawing traces with square corners? Maybe it is interesting from a mathematical point of view, but I’ve never met a board designer who used square apertures to draw traces. Every modern board design I’ve ever seen (by modern, I mean designed in a CAD system, not the old manual tape layouts) uses round apertures, and when using a round

aperture the width is always constant, no matter how you “bend” the trace.

Response from Lee Ritchey, Speeding Edge:

That is another urban legend and has never been true. I’ve seen fabricators say this and then etch outer layers with all sorts of surface mount pads that have traces entering them that result in right-angle corners and never complain!

We’ll probably all go to our graves before we flush out all this misinformation!

Response from Scott McMorrow, TerraSpeed Consulting Group:

It’s not so much “misinformation” but “misapplication” of information. The “no right-angle bend rule” makes perfect sense on RF microstrip boards where the traces are about 1 or 2 mm from the plane, and are extremely wide. When you’re dealing with 50 ohm traces that are 100 mils wide, excess capacitance at the corner is a big deal, since the discontinuity acts for about 140 mils in distance (the diagonal across the corner). If built on an FR-4 type material with a $D_k = 4$, this corner discontinuity has about a 25 ps time duration, which can be significant. Additionally, RF engineers are always trying to reduce narrow band return loss to

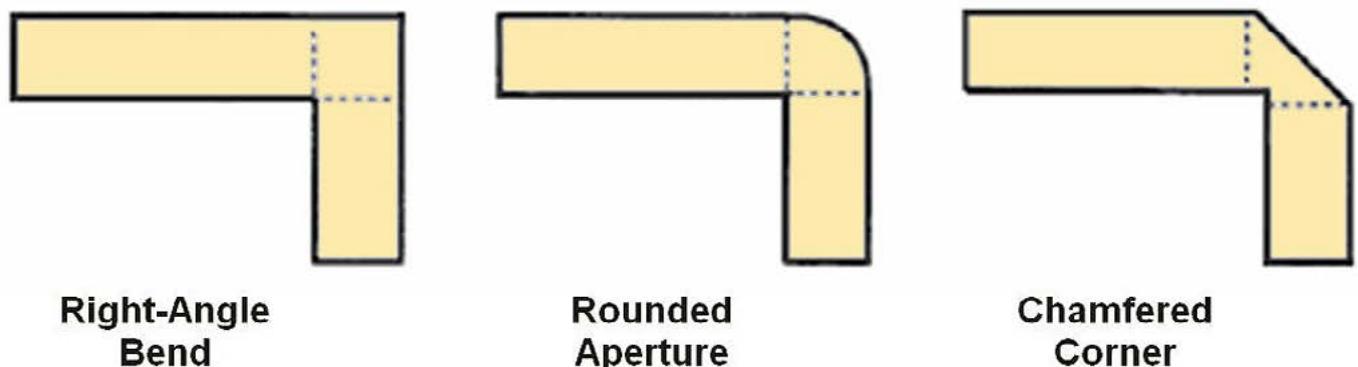


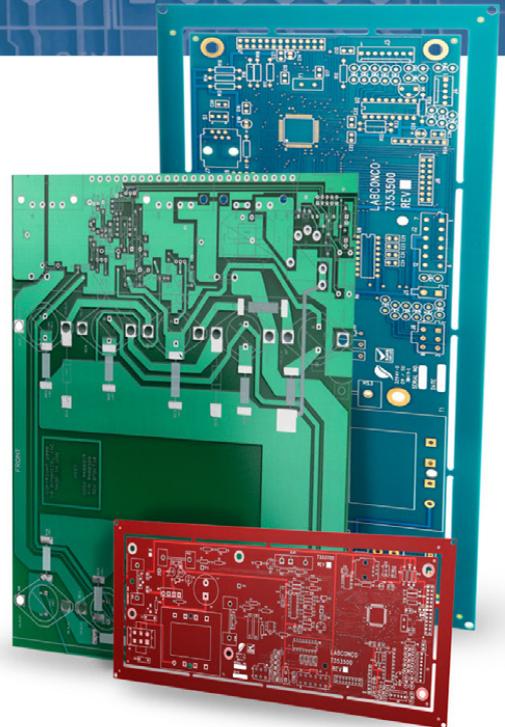
Figure 1: Right-angle bends vs. rounded apertures and chamfered corners.

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RIGHT-ANGLE BENDS IN PCB TRACES *continues*

extremely low levels, far beyond that which is necessary for broadband digital.

However, when we scale the traces down to 5 mil width, the discontinuity is the same relative size, but 1/20th the physical size, and acts for only about 7 mils, or about 1.25 ps. If a 1.25 ps discontinuity is a big deal to an engineer then this might matter, or if you have 20 corners, the cumulative effect of this discontinuity will span a duration of 25 ps, or 1/4 of a 10 Gbps bit time. But 1.25 ps of excess capacitance does not matter until we're designing for 50 Gbps, and only a fool would route a trace with 20 corners in it, so effectively corners are not an issue.

Lee, you are correct.

Jack,

I've decided to put some numbers to the Right Angle Bend discussion, since it's nice to know when we need to be concerned about a particular physical phenomena.

Your point regarding round apertures on traces is important, although slightly misleading. A round aperture is applied to the end of a trace with the center of the radius at the center of the trace width, such that the outside apex is rounded, while the inside apex is square. Thus, a trace corner with circular end apertures still has excess capacitance when compared to the optimal RF miter¹. If we use Eric Bogatin's approximation of a 50% miter (corner sliced diagonally in the center at 45 degrees, which is not quite correct, but is close) to compute the excess capacitance, then using a circular end aperture on traces at corners reduces capacitance by $(1-\pi/4)$, or about 21%, which helps, but still leaves us with excess capacitance.

Here are some calculations based on Bogatin's "Signal Integrity Simplified," page 317, which I've verified:

Square corner capacitance (pf) =
 $40/Z_0 \times \sqrt{\text{Er}} \times w$
 where w = width in inches

E_r = dielectric constant

Z_0 = characteristic impedance of trace

50 ohm impedance, $E_r = 4$

“
A round aperture is applied to the end of a trace with the center of the radius at the center of the trace width, such that the outside apex is rounded, while the inside apex is square.
 ”

10 Gbps (5 GHz Nyquist) with square apertures:

Case 1) A 100 mil wide trace - 160 fF = 199 ohm shunt Z at 10 GHz, produces a 40 ohm tdr blip for 17 ps (17% UI).

Case 2) A 10 mil wide trace - 16 fF = 1990 ohm shunt Z at 10 GHz, produces a 48.8 ohm tdr blip for 1.7 ps (1.7% UI).

Case 3) A 5 mil wide trace - 8 fF = 3980 ohm shunt Z at 10 GHz, produces a 49.4 ohm tdr blip for 850 fs (0.85% UI).

Case 4) A 1 mil wide trace - 1.6 fF = 19900 ohm shunt Z at 10 GHz, produces a 49.75 ohm tdr blip for 170 fs (0.2% UI).

20 Gbps (10 GHz Nyquist) with square apertures:

Case 1) A 100 mil wide trace - 160 fF = 99 ohm shunt Z at 10 GHz, produces a 33 ohm tdr blip for 17 ps (34% UI).

Case 2) A 10 mil wide trace - 16 fF = 995 ohm shunt Z at 10 GHz, produces a 47.6 ohm tdr blip for 1.7 ps. (3.6% UI).

Case 3) A 5 mil wide trace - 8 fF = 1990 ohm shunt Z at 10 GHz, produces a 48.8 ohm tdr blip for 850 fs (1.7% UI).

Case 4) A 1 mil wide trace - 1.6 fF = 9947 ohm shunt Z at 10 GHz, produces a 49.75 ohm tdr blip for 170 fs (0.3% UI).

20 Gbps (10 GHz Nyquist) with circular end apertures on traces (reduce excess shunt capacitance by 21%):

Case 1) A 100 mil wide trace - 126 fF = 126 ohm shunt Z at 10 GHz, produces a 36 ohm tdr blip for 17 ps (34% UI).

Case 2) A 10 mil wide trace - 12.6 fF = 1265 ohm shunt Z at 10 GHz, produces a 48

ohm tdr blip for 1.7 ps (3.4% UI).

Case 3) A 5 mil wide trace - $6.3 \text{ fF} = 2530$ ohm shunt Z at 10 GHz, produces a 49 ohm tdr blip for 850 fs (1.7% UI).

Case 4) A 1 mil wide trace - $1.26 \text{ fF} = 12650$ ohm shunt Z at 10 GHz, produces a 49.8 ohm tdr blip for 170 fs (0.3% UI).

So, for real traces, on real boards, with real CAD end apertures, a single corner on traces that are 1-10 mils wide, at frequencies of 10 GHz or below, effectively cannot be measured without specialized de-embedding methods. The discontinuity is too small and too short. For microwave width traces, those corners are large discontinuities with real consequences.

If we happen to be running at 56 Gbps (28 GHz Nyquist):

Case 2) A 10 mil wide trace - $12.6 \text{ fF} = 452$ ohm shunt Z at 10 GHz, produces a 45 ohm tdr blip for 1.7 ps (9.5% UI).

Case 3) A 5 mil wide trace - $6.3 \text{ fF} = 604$ ohm shunt Z at 10 GHz, produces a 46 ohm tdr blip for 850 fs (4.8% UI).

Case 4) A 1 mil wide trace - $1.26 \text{ fF} = 4518$ ohm shunt Z at 10 GHz, produces a 49.5 ohm tdr blip for 170 fs (0.9% UI).

There is nothing wrong with the information about square corners found in the RF and microwave literature. It applies to the wide, low-loss traces used in RF design, and it is quite correct; corners do matter.

For digital designs traces of 10 mil width or less are generally used, and as such corner design is essentially unimportant, due to the benefit of size scaling on reduction in the size and duration of the discontinuity.

As a figure of merit, I'd suggest we use 5% of UI, and +/- 5% Z0 as the point that we start considering that a particular type of discontinuity matters for SerDes channels. This is conser-

vative, but I like being conservative, and working with positive margin, rather than fighting against negative margin.

Up to 20-ish Gbps, 90 degree CAD layout corners on traces up to 10 mil in width have no significant impact on the signal. At 56 Gbps, 90 degree CAD layout corners become significant starting at 5 mil width.

At 28 Gbps and 56 Gbps designers may be fighting high copper and dielectric losses, forcing the usage of low loss dielectrics ($\tan\delta < 0.005$), smooth copper foils (surface roughness < 0.4 micron RMS), and wider traces. In these cases, corner mitering, or routing of traces using circular arcs, might be considered, when traces are wider than 10 mil @ 28 Gbps and 5 mil @ 56 Gbps.

Another way to look at corners is from the view of a transmission line with distributed loading. On page 317 of Eric Bogatin's book, he shows his geometric derivation for the computation of corner capacitance. We

can reduce his geometry into three square cells at a corner, which can be further divided into six equal sized triangular sections. One triangular section represents the excess corner capacitance. If we call this the "unit corner cell," then it's clear that corner capacitance represents an increase of the capacitance of the entire cell by $6/5$, or 1.2.

Knowing this, we can compute the distributed Impedance of the line as $Z(\text{distributed}) = Z0 \times \sqrt{5/6} = 0.91 Z0$. For 50 ohm impedance, that amounts to a distributed transmission line impedance of 45.6 ohms. So,

if we were to cascade corners in a diagonal stairstep fashion, the distributed impedance of the line would asymptotically approach around 45 ohms, since the capacitance becomes averaged across a longer distance. This is independent of the line width. In addition, the distributed delay of the transmission line is increased by $\sqrt{6/5}$ or by 1.095,

“
For digital designs traces of 10 mil width or less are generally used, and as such corner design is essentially unimportant, due to the benefit of size scaling on reduction in the size and duration of the discontinuity.
 ”

RIGHT-ANGLE BENDS IN PCB TRACES *continues*

across the unit cell section, or about 16 ps per inch of additional delay for $\epsilon_r=4$.

So, where could we have a problem? Using the distributed version of the analysis, we can see that stair step type structures might accentuate corner capacitance issues. One place where this can happen is in the routing escape pin fields of BGA and connectors. Another is the increase in actual delay that can be seen in trace delay matching serpentine sections. Even if coupling between serpentine sections is minimized, a unit rectangular serpentine section has four corners. For 5 mil trace width, each corner has an excess capacitance of 6.3 fF, an incremental delay adder of about 300 fs. For the four corners of a serpentine section, there is 1.2 ps of additional delay, not accounted for by net length calculations. Short squarish delay matching sections (so called delay bumps or blips along a line) with four corners per blip will experience a large percentage increase in delay over the net length calculation vs. longer

rectangular delay matching sections, with fewer corners in total.

*Best regards,
Scott McMorrow*

Teraspeed Consulting Group LLC **PCBDESIGN**

Jack Olson would like to thank Scott McMorrow of Teraspeed Consulting Group for donating his time, experience and resources to this question.

References

1. Experimental derivation of optimal miter can be found in: R.J.P. Douville and D. S. James, Experimental study of symmetric microstrip bends and their compensation; IEEE Trans. Microwave Theory Tech., vol. MTT-26, pp. 175-182, Mar. 1978.



Jack Olson, CID+, has been designing circuit boards full-time for more than 20 years. To contact Olson [click here](#).

video interview**A Talk with Murrietta Circuits**

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Next-Generation High-Speed Materials: An Updated List



by **Tom Doslak**

STREAMLINE CIRCUITS

The evolution of high-speed PCB materials moves just as quickly as the circuit that passes through them. It is no surprise that sometimes a very busy product developer might be confused by, or simply be unaware of, the newest advancements in cutting-edge substrates. Because of this, I would like to reach out to the product development community to help educate them and make them aware of the latest in PCB materials.

Designers must develop products with more functionality, at faster speeds, in smaller packages. This has been going on for generations, but there has been a major push by chip manufacturers. These chip packages (BGAs and now microBGAs) allow tremendous functionality with pin counts in excess of 7,000 points on .25 mm pitch microBGAs, while demanding extreme circuit speeds in excess of 50 gigahertz and tighter tolerances throughout the PCB.

This seems like an impossible task. But forward-thinking PCB and material manufacturers continue to reinvest in advanced equipment for

critical process consistency and advanced capabilities. We can now support today and tomorrow's next-generation high-speed requirements. This leaves a product designer or engineer with two critical decisions: Choosing the right PCB vendor, and selecting the product material that optimizes both performance and cost.

Analog or Digital?

Two basic types of circuits fall in the category of high-speed and low-loss materials. The first is high-frequency analog (RF/microwave), and the second is high-speed digital. The RF microwave circuits need to have process precision for tight tolerance on their signals. These material types have been developed over time for critical signal loss and high frequency. There are two types of critical signal loss—one is due to reflection and other is loss of circuit energy by way of the dielectric material. Signal reflection is caused by controlled impedance variations or mismatches. These impedance variations are caused mostly by the PCB vendor's process consistency and capabilities, along with material functionality that can vary with change in temperature and frequency.

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NEXT-GENERATION HIGH-SPEED MATERIALS: AN UPDATED LIST *continues*

The high-speed digital products are usually very complex, high-layer count, high-density (sub 3 mil traces) performing at very high frequencies and speeds. These products also have demanding material parameters, along with advance physical requirements as well. The overall industry still sees these two basic types of stand-alone circuit requirements, but the trend in the last couple years has been towards all-in-one next-generation materials.

These advanced materials now focus on both material parameters (Dk,Df,CTE,T_g,T_d, Z-axis) and physical structures (thin cores and consistent variation) with high-performance blends for manufacturing advantages and overall costs savings. These new materials help product developers in today's products with more robust thermal and electrical properties.

We deal with these high-speed materials every day, and we know what substrate works, and with which applications. We do not sell materials of any kind, so I believe we can provide an unbiased description of each material.

We have created this [updated list](#) of high-speed materials. We consider these to be the best next-generation, high-speed PCB materials available today. All of these materials have been tested, proven, and are ready for production. For easy reference, each material line item features a product name, vendor, summary, and data sheet.

This list will be continuously updated. I hope it proves to be a valuable resource for PCB designers, engineers and fabricators. I value your feedback. Let me know if you have any questions or comments about these materials. **PCBDESIGN**



Tom Doslak is vice president of sales and marketing for Streamline Circuits and has more than 22 years of PCB sales experience. To contact Doslak, [click here](#).

video interview

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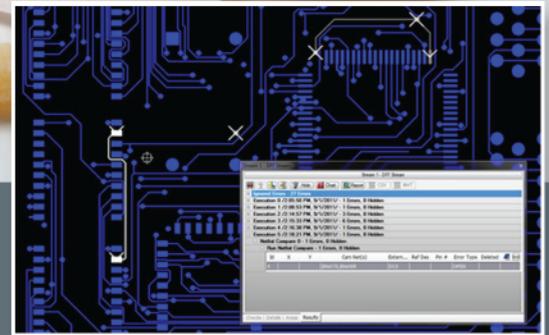
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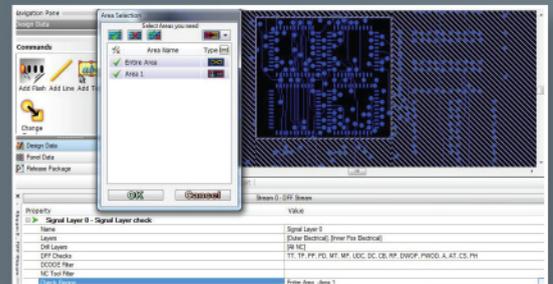
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News Highlights



[Rockwell Collins to Close Cedar Rapids PCB Unit](#)

Rockwell Collins, a provider of avionics and communications equipment, will close its Cedar Rapids, Iowa-based PCB manufacturing unit, in business since 1964, in the next six to nine months.

[Murrietta Earns MIL-PRF-55110G for Polyimide Materials](#)

Murrietta Circuits has completed all testing and been granted full MIL-PRF-55110 G qualification for polyimide material, which will allow the company to begin receiving military orders for polyimide material PCBs immediately.

[Invotec Awarded by Aero Engine Controls](#)

Invotec Group, Europe's leading manufacturer of time-critical, high-technology PCBs, has been awarded two major awards at this year's Aero Engine Controls (AEC) Supplier Conference. In addition to the Engineered Products Division Award 2012, Invotec also won the overall Supplier of the Year Award.

[Eltek Posts Drop in Q4, FY2012 Revenues](#)

Revenues for the year ended December 31, 2012 were \$45.6 million, a 2.5% decrease compared to revenues of \$46.8 million in 2011.

[DARPA Reveals First FANG Challenge Winner](#)

The Defense Advanced Research Projects Agency (DARPA) has awarded a \$1 million prize to "Ground Systems," a three-person team with members in Ohio, Texas, and California, as the winner of the Fast Adaptable Next-Generation Ground Vehicle (FANG) Mobility/Drivetrain Challenge.

[Counterfeit Parts the Focus of SMTA, CALCE Symposium](#)

The Counterfeit Electronic Parts and Electronic Supply Chain Symposium will feature Chair Professor and CALCE Director Michael Pecht sharing his knowledge and experience on the global electronics industry and how that creates the market for

counterfeit electronics. In all, eight sessions over two days will be offered June 25-27 in College Park, Maryland.

[Endicott Interconnect's SiP Tech Employed by Lockheed](#)

Endicott Interconnect Technologies, Inc. (EI) has announced that its System-In-Package technology performed successfully as a key subsystem of Lockheed Martin's Extended Area Protection and Survivability (EAPS) Program during a test on March 22 at White Sands Missile Range, New Mexico.

[Microtek Laboratories Wins Northrop-Grumman Contract](#)

Microtek Laboratories, a leading independent test laboratory, was awarded a contract from Northrop Grumman Aerospace Systems (NGAS) to perform PWB/PCB coupon testing for their Redondo Beach, California facility.

[Projects Expand Frontiers of Cyber-Physical Systems](#)

CPS technologies employ sensors, processors, and actuators to enable computers to perform in the physical world, providing useful, real-time information. They are used in cruise control mechanisms in passenger cars, auto-pilot systems in aircraft, control mechanisms in prosthetics, and for search and rescue in futuristic robotic devices.





The Integrated Solution



Murrietta Circuits Receives Raytheon's Highest Award !!!

Murrietta Circuits was recognized for its quality and performance by Raytheon Integrated Defense Systems when it received a Five Star Award during the Supplier Excellence Award Ceremony on May 8, 2013 in Andover, MA.



Raytheon recognizes its Five Star Suppliers based on three important factors: 100% On-Time Delivery, 100% Sustained Quality and Continuous Process Improvements. Raytheon has over 5000 global suppliers and Murrietta Circuits was one of only 14 suppliers to be recognized for this tremendous achievement.

Murrietta Circuits provides complete assemblies that are utilized in Raytheon's SM3 Missile and the Sparrow Program as well as supporting Raytheon in their relentless pursuit of excellence, new technologies and innovations. The Murrietta Circuits Team understands the importance of Raytheon's projects and every single one of our team members work tirelessly to provide excellent quality and customer service. We at Murrietta Circuits are very proud of our hard-working and dedicated Team Members.

Pictured left to right:

Robert Curbeam: Vice President, Mission Assurance, Quality & Six Sigma

Andrew Murrietta: Murrietta Circuits CEO

Sharon Waddell: Murrietta Sales Executive

David Crowley: President

Michael Shaughnessy: Vice President



Skewed Again

by **Barry Olney**

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When skew needs to be adjusted, it is best done at either end of the differential pair.

In this way, the coupling and signal quality of the remainder of the pair is maintained.

Differential signaling is a method of transmitting serial, high-speed, complementary signals down a pair of coupled transmission lines. The equal and opposite nature of the differential pair means that demand on the power distribution network (PDN) is less than for a similar, single-ended data path. And, since external interference tends to affect both signals equally, the noise is cancelled providing high immunity to common mode electromagnetic interference compared to single-ended transmissions. But that is assuming the pair are perfectly balanced and terminated correctly. Generally, on-die termination (ODT) compensates for this, which may otherwise have a significant impact on signal quality and power dissipation.

Differential skew refers to the time difference between the two single-ended signals in a differential pair. Any mismatch in delay (skew) will result in changing part of the differential signal power into common-mode power.

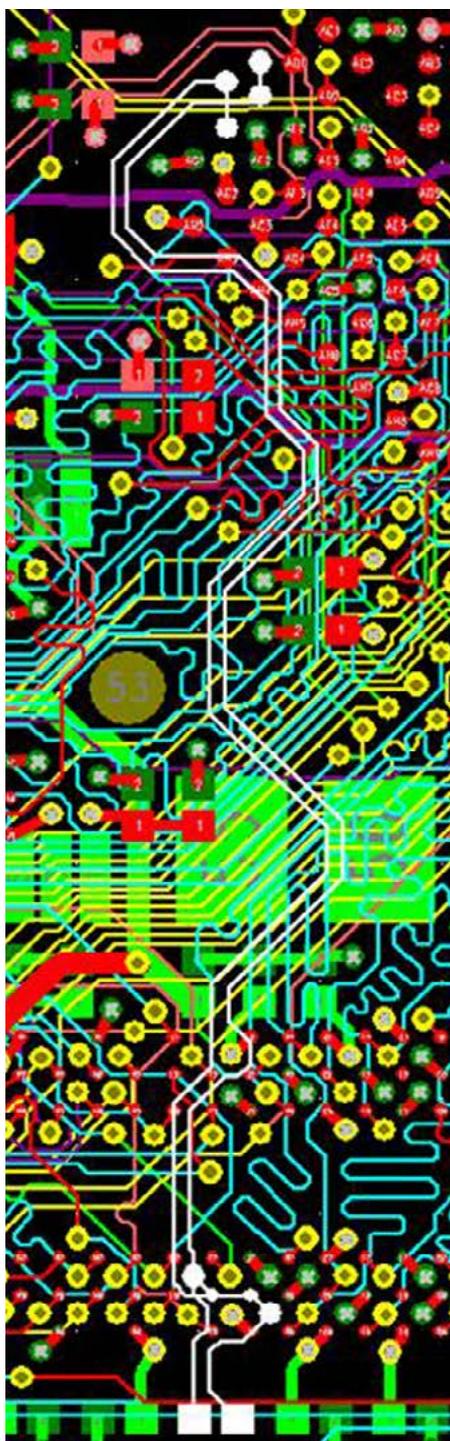


Figure 1: Multiple bends in the pair.

Differential skew has become a performance limiting issue for high-speed SERDES links. The operation of such links involves significant amounts of signal processing to recover clocks, reduce the effects of high-frequency losses, reduce inter symbol interference (ISI), and improve signal-to-noise ratio. Skew limits the bandwidth of these links, adds data-dependent jitter, and limits the possibility of equalizing links to compensate for high-frequency skin effect and dielectric losses.

Differential signaling evolved due to the fact that high-speed, synchronous, parallel busses were getting wider (consuming more real estate) and faster until signal integrity issues forced a fundamental change in strategy. Multi-gigabit design is now the norm with up to 10 Gbps SERDES devices commonly available in FPGAs. Beyond the theoretical 12 Gbps limit, optical interconnects become the only solution.

Skew is commonly caused by unmatched delays of a differential pair but as speeds (and rise times) increase skew can also be caused by non-uniform dielectric materials in the substrate.

The inconsistency of the dielectric material comes from that fact that the fiberglass and the epoxy resin that make



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SKEWED AGAIN *continues*

up PCB core and prepreg materials have a different dielectric constant. And because the fabricator cannot guarantee the placement of the fiberglass with respect to the location of the traces, the result is uncontrolled differential skew. One way to avoid this is to always route differential pairs diagonally across the board as the fiberglass matting is laid in the X,Y direction. Or, zigzag diagonally down the board as done in Figure 1.

In, [Differential Pair Routing](#), (*The PCB Magazine*, October 2011) I discussed the optimal settings for differential pair design rules. With regard to coupling, I also pointed out that it is best to not use tight coupling but rather couple the traces by twice the trace width. Thus, for a differential pair with a trace width of 4 mils, the separation (edge-to-edge) should ideally be 8 mils. This allows the pair to separate (Figure 1) around an obstacle (e.g., a via) without altering the impedance by more than 4%.

However, wider spacing of the differential signals also means that the skew introduced by bends in the pair will increase. It is best to always have an even number of bends as one to the left will counteract one to the right.

Placement can also help alleviate this problem. Try to align the chips in such a way so that the traces leave the first chip (driver) and enter the second chip (receiver) from the same direction as this will result in an even number of

bends dramatically reducing skew.

Also, the squarer the bend, the more skew introduced. Arcs are shorter than 45 degree bends, which in turn are shorter than orthogonal corners. But if they are all the same then it does not matter.

In Figure 2, I have used orthogonal corners to illustrate the disparity between various routing strategies of differential pairs. The required number of bends depends on the number of obstacles that the pair encounters along its path. These obstacles may be other devices, lands, mounting holes or vias, which means that the traces may also have to be separated.

Pair A is obviously not the best example. This pair has two long bends on one side and two short bends on the other, adding a skew of twice the bend length to the outer trace. On the other hand, Pair B represents the best-case scenario whereby the pair leaves the driver in the same direction as they enter the receiver. This always provides an even number of short and long bends on both sides allowing the accumulated skew on both sides to be equal. Pair C, although it looks a lot worse than Pair A, actually has the same amount of skew as A. This pair leaves the driver to the right and then enters the receiver to the left requiring an odd number of short and long bends on each side of the pair.

A few months ago, I had the opportunity to analyze a design that had a number of high-

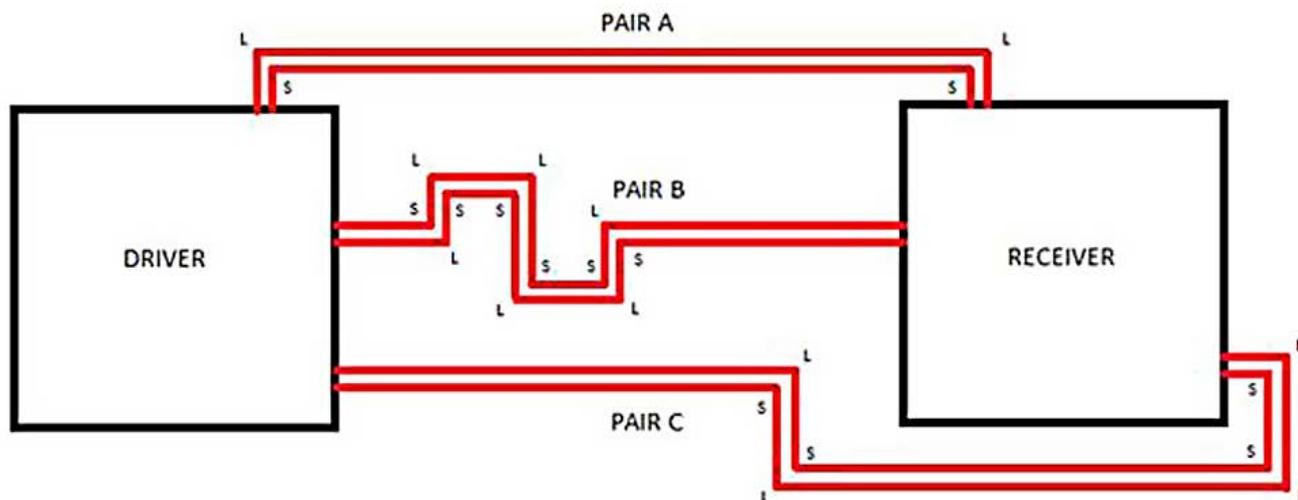


Figure 2: A driver and receiver chip with various routing strategies.

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SKEWED AGAIN *continues*

speed USB 3.0 differential pairs. This was the first time I heard the term “cauliflower routing.” Cauliflower routing refers to a routing pattern as illustrated in Figure 3, whereby, one

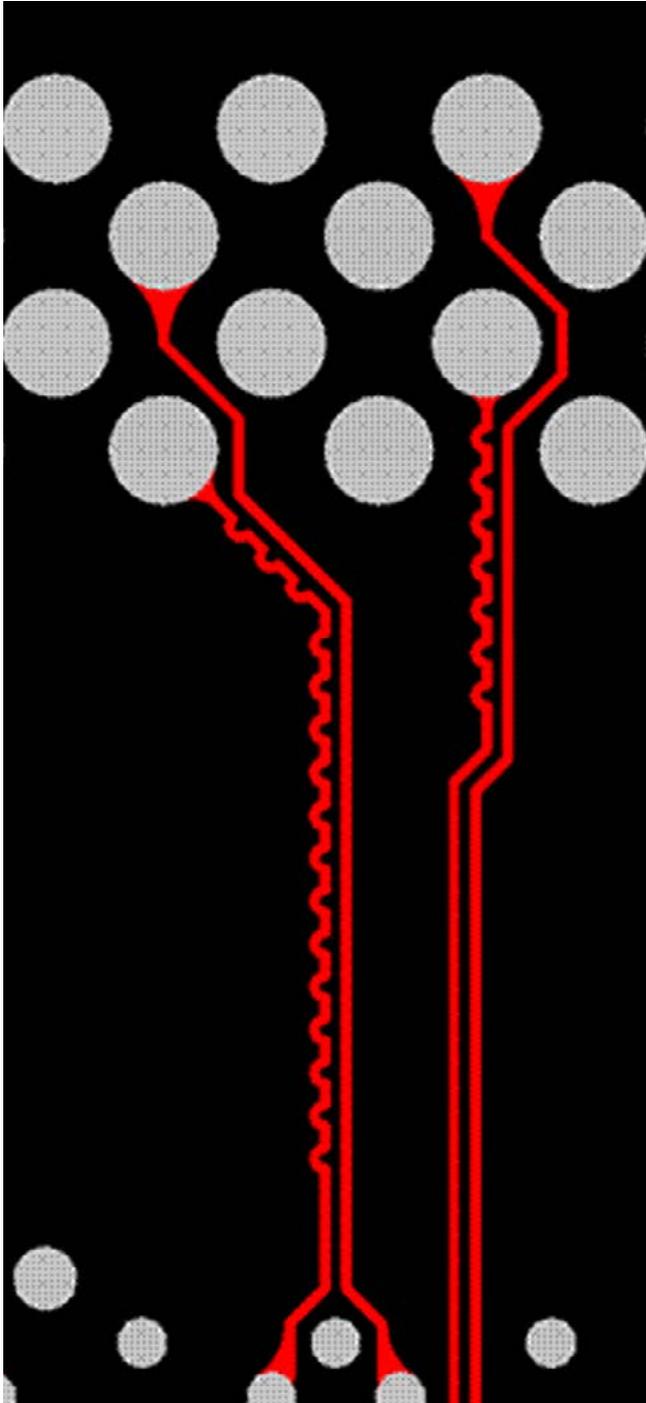


Figure 3: The dreaded cauliflower routing pattern.

side of the differential pair is lengthened by adding a number of semicircles (bumps). This is not good—please do not try this at home! The cauliflower pattern varied the differential impedance, in this example, from 90 ohms to 102 ohms. This dramatically reduces the quality of the signal adding numerous reflections.

In this case, the solution was simple. The USB 3.0 pairs went off the board through a connector to a piggy-back board that had the pins wired the opposite way around. This allowed the main board to be 200 mils longer for side A of the pair, and the piggy-back board side 200 mils longer for side B, thus cancelling out skew.

Since a differential pair is routed coupled, its entire length, the offset of one side of the pair to the other is rarely greater than 100 mils. So what is the best way to balance the skew?

When the skew needs to be adjusted, it is best done at either end of the pair—whichever has the poorest termination. In this way, the coupling and signal quality of the remainder of the pair is maintained along its length.

Figure 4 shows the skew control for coupled pairs. The idea is to keep the traces in close proximity for as long as possible. The trace to the left goes to pin AF3 on the BGA. To lengthen this side of the pair, we follow the other trace (on the right) as closely as possible and then wrap the left trace around the pin/land.

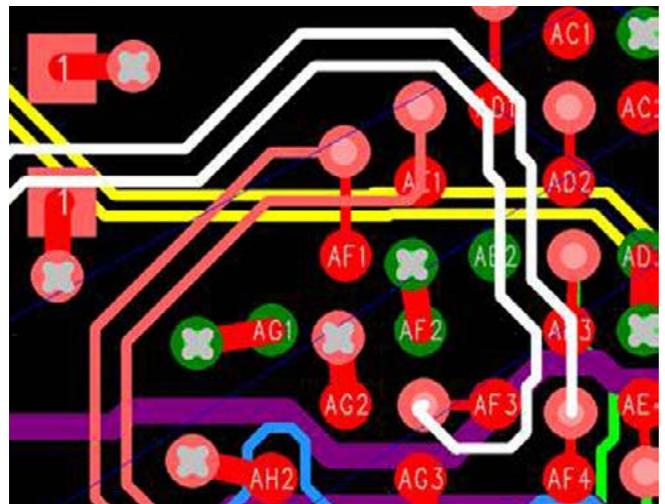


Figure 4: Skew matching is performed at the pin/land level.

Ideally, the delay of the differential pair should be confirmed by simulation rather than by matched length. I have mentioned in a couple of other columns on matched length and differential pair routing, that the length of the signal is not necessarily directly proportional to the delay. Delay can only be determined by simulation.

Points to remember:

- Any mismatch in delay (skew) will result in changing part of the differential signal power into common-mode power
- As speeds increase, skew can also be caused by non-uniform dielectric materials in the substrate
- It is best to not use tight coupling differential signals but rather couple the traces by twice the trace width
- It is good to always have an even number of bends as one to the left will counteract one to the right
- Align the chips in such a way so that the traces leave the first chip (driver) and enter the second chip (receiver) from the same direction. This always provides an even number of short and long bends, on both sides, allowing the accumulated skew on both sides to be equal
- Cauliflower routing should be avoided
- When the skew needs to be adjusted, this should be done at either end of the pair—whichever has the poorest termination. In this

way, the coupling and signal quality of the remainder of the pair is maintained

- Skew matching is performed at the pin/land level. The idea is to keep the traces in close proximity for as long as possible **PCBDESIGN**

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2. [Beyond Design: Differential Pair Routing](#), Barry Olney
3. [Beyond Design: A New Slant on Matched-Length Routing](#), Barry Olney
4. [Board Level Simulation and the Design Process: Plan B: Post Layout Simulation](#), Barry Olney
5. [Handling Differential Skew in High-Speed Serial Buses](#), Arnold Frisch
6. [High-Speed Signal Propagation](#), Howard Johnson
7. The ICD Stackup and PDN Planner can be downloaded from www.icd.com.au.



Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. ICD is a PCB design service bureau specializing in board-level simulation. The company developed the ICD Stackup Planner and ICD PDN Planner software. To read past columns or to contact Olney, [click here](#).

IPC: Book-to-Bill Highest in Nearly Three Years

IPC has released the April 2013 PCB book-to-bill ratio, which reached 1.10, its highest level since July 2010.

North American PCB shipments were down 7% in April 2013 from April 2012, but bookings increased 7.2% YOY. Year to date, PCB industry shipments were down 5.1% and bookings were down 2.3%. Compared to March, PCB shipments in April decreased 9.9%, and bookings

declined 14.3%. Bookings have outpaced shipments for the past five months.

"This is the fifth consecutive monthly increase in the ratio, which reinforces our hope that PCB sales will strengthen during the coming months," said Sharon Starr, IPC director of market research.



TOP TEN

PCBDesign007
News

News Highlights from PCBDesign007 this Month

① DownStream Hosting BluePrint-PCB Webinar in June

Do you dread the tedium of PCB documentation? Eliminate the barriers, while spending less time and creating better electronic documents with BluePrint-PCB. Discover how to ease the creation, distribution, and management of your PCB documentation during this technical webinar June 25, 2013.

② New Zuken Software Boosts Product Planning & Logical Design

Zuken has released new versions of its System Planner and Design Gateway engineering solutions that accelerate and streamline product planning and logical design for engineers.

③ Agilent Launches Design Tools for Satellite Comms

Agilent Technologies Inc. has released two reference libraries for SystemVue, its premier platform for communications and aerospace/defense systems design. Satellite and communications systems can now be verified under a variety of realistic impaired conditions before baseband or RF hardware is available.

④ Agilent Technologies' EMPro 2013 Targets EMI

EMPro 2013 allows engineers to simulate the radiated emissions of electronic circuits and components and then determine whether these emissions are within levels specified by common EMC standards.

5 ICD Releases 2013 Edition of ICD Stackup Planner

Managing Director Barry Olney said, "This is a major release with many new features. After more than four months development and beta testing, we now have a fully integrated, compelling product. We would like to thank our customer base for their input as this release is based on their feedback."

6 Intercept Technology Joins ODB++ Solutions Alliance

As a member of the IPC-2581 Consortium, IPC, the ODB++ Solutions Alliance, and various industry cross-vendor partnerships, Intercept strongly supports vendor collaboration for the promotion of improved design and manufacture practices.

7 IPC, PCB Libraries Partner to Update, Improve IPC-7351

IPC has teamed up with PCB Libraries, Inc. to provide updated library documentation and more powerful PCB library tools to support users of IPC-7351, Generic Requirements for Surface Mount Design and Land Pattern Standard.

8 DAC 2013 Honors EDA Industry

For 50 years, the Design Automation Conference (DAC) has provided a global forum for designers and engineers from around the world. As part of its 50th anniversary celebration, DAC 2013 will honor the geographic breadth and global reach of electronics innovation.

9 IEEE SA EDA Symposium Helps Users Understand Standards

IEEE, the world's largest professional organization advancing technology for humanity, has announced the launch of the IEEE Standards Association (IEEE-SA) Symposium on Electronic Design Automation (EDA) Interoperability.

10 PCB Design Software EAGLE V6 New Manual Now Available

EAGLE is a user-friendly, powerful, and affordable software for efficient PCB design and combines the schematic editor, layout editor, and autorouter on one single interface.



EVENTS

PCB Design Events

IPC Complete Calendar of Events

SMTA Calendar of Events



Innovations in Electronics Manufacturing for Medical Devices

June 12-13, 2013

Minneapolis, Minnesota, USA

Medical Devices Summit West

June 13-14, 2013

San Francisco, California, USA

Atlantic Design & Manufacturing Expo

June 18-20, 2013

Philadelphia, Pennsylvania, USA

NEPCON Thailand

June 20-23, 2013

Bangkok, Thailand

2013 CEA Market Research Summit

June 24, 2013

New York City, New York, USA

Counterfeit Electronic Parts Symposium East Tabletop Exhibition

June 25-26, 2013

College Park, Maryland, USA

2013 International Conference on Mechatronic Systems and Materials Application

June 26-27, 2013

Guangzhou, China

Upper Midwest Expo & Tech Forum

June 27, 2013

Bloomington, Minnesota, USA

Micromachine/ MEMS

July 3-5, 2013

Tokyo, Japan

Thermotec 2013

July 3-5, 2013

Tokyo, Japan

Ohio Valley Expo & Tech Forum

July 11, 2013

Cleveland, Ohio, USA

ISMSE 2013

July 27-29, 2013

Singapore



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Next Month in *The PCB Design Magazine*

Sometimes it feels as if we're floating in a sea of "Design For" acronyms: DFM, DFA, DFT, DFE, DFX, and into infinity. But in the end, isn't it all about profit? Next month, our writers and columnists tackle the most important "Design For" of all: Design For Profitability, or DFP.

See you next month—it just might be profitable!