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July 2013

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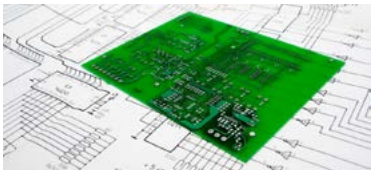
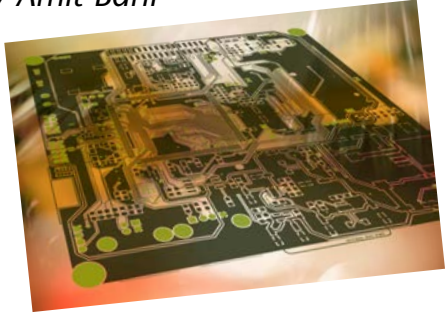
This Issue: DESIGNING FOR PROFIT

FEATURED CONTENT

We have become a "design for" industry: design for manufacturing, design for test, design for assembly, ad infinitum. But in the end, isn't it all about designing for profit? In this issue of *The PCB Design Magazine,* our expert contributors explain how good DFP techniques can add profit and remove costs from your design process.

FEATURE COLUMNS





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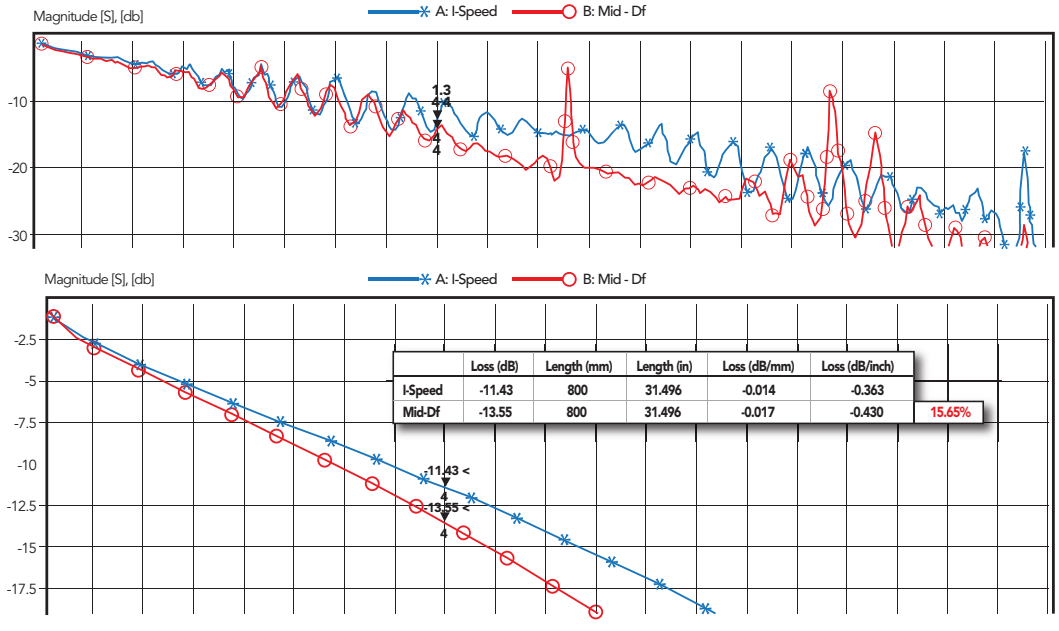

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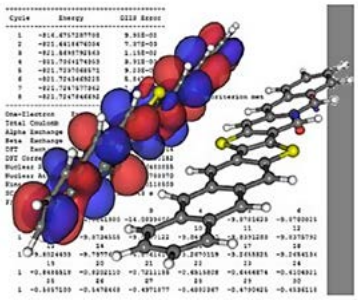

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Designing for Profitability

by Steve Hageman
ANALOGHOME

SUMMARY: What can designers do to increase the profitability of their designs? No list of do's and don'ts will work in every case, because each situation is just different enough that the list won't fit correctly and will need to be modified. But Steve Hageman shares some tips on virtual prototyping and other techniques that have made a real difference in his design process.

Let's start with this 1991[1] quote from Hewlett Packard: "Managers in marketing, manufacturing and especially research and development at HP are becoming more aware that they jointly manage a cross-functional process. Their people define and design a product and develop processes to manufacture and market that product."

The only thing that would be different today is the first word, which would now read "stakeholders," because even the term "employees" doesn't describe the interconnected web of internal and external design talent that goes into making a product today.

HP used their experience in product design to improve what they called break-even time (BET), which is the time to when their shipping product paid for all the development work and started to make a net profit. Many people use different metrics today, but they all boil down to some form of BET and this is as important today as it was in 1991.

So what can we as partners in the design process do to increase the profitability of our designs? I don't see how I can make a list of do's and don'ts that will work in every case, because I have found that every situation is just different enough that the list won't fit correctly and will need to be modified; but I can share with you the things that have made a real difference in my design process and where I would like to go next.

All of this is aimed at the goal of improving the BET of the widget that I'm working on at the time and that hopefully leads to happy customers.

Breadboard the Bugs Out

In the last century, nearly every engineer built a breadboard of their design, corrected what didn't work and then passed it off for PCB layout. This reduced the risk of the first PCB design. Then came the leadless and BGA IC packages and that changed breadboarding forever. One can't easily just sit down with a soldering

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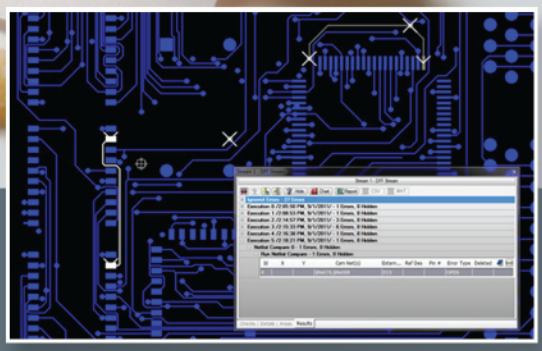
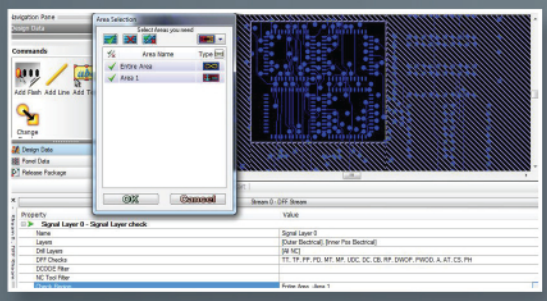


Netlist errors are quickly validated in DFMStream



Define DFM checks by area so components such as BGAs can be verified with unique rules different from rest of design

DownStream Technologies

iron and make a breadboard with these types of parts using the old way of doing things, so new means of putting breadboards need to be devised. Logic breadboarding can be done with various pre-made evaluation boards that can be bought, but RF and analog presents more of a problem.

With the explosion of quick-turn and very low-cost fabricators, along with the many free to very low-cost PCB design tools, engineers can (and do) still quickly make breadboards of their analog and RF designs.

As I have written before, even very respectable designs that work to 10 GHz or more can be made on the so-called "barebones" two-layer overnight prototype[2]. Several design iterations or different approaches can be tried in less than a week using these methods.

For a project that I was working on a while back I needed to decide on one of several proposed amplifier designs to get really good harmonic distortion performance. To help decide, I quickly used my PCB design tool to make a quick turn overnight prototype. In just a few days I had working boards, and I had real data on which design worked better.

Interestingly, this method also has the advantage of really testing the correctness of the PCB footprints and uncovering potential layout sensitivities and issues before the designer is committed to the actual PCB design! All this helps to reduce the risk of the first PCB iteration and that helps keep the schedule on track in within budget.

No matter what you may have heard, analog and RF breadboards are not dead yet!

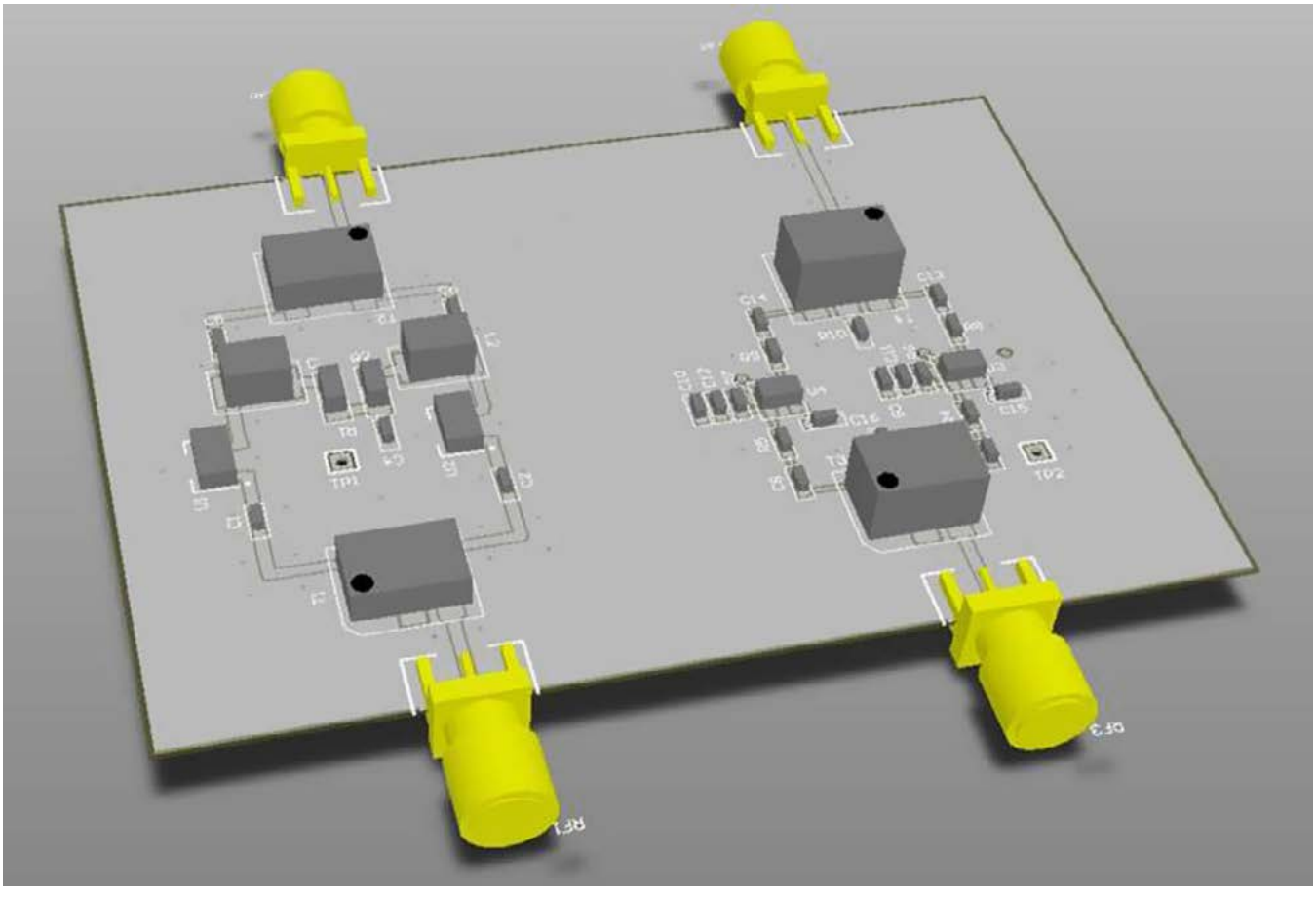


Figure 1: Engineering breadboards are now commonly made on real PCBs by quick-turn PCB shops. This is an example of two 50 MHz low-distortion amplifiers that were quickly prototyped and built in just a few days using this approach.

Virtual Prototypes: A Picture is Worth 1,000 words

Many modern PCB tools like Altium Designer[3] can handle many more tasks than just laying traces. I use Altium at every phase of the project from initial concept rendering to final assembly documentation. This was largely made possible by the addition of a 3D rendering engine in Altium and the total integration of 3D component bodies in the Altium footprint libraries.

This old adage "A picture is worth 1,000 words" holds true for PCB design. Instead of 2D sketches that never quite worked or were easily misunderstood, we can now do any level of modeling right in our familiar PCB design tool.

I use this capability to quickly rough out concepts with clients, sometimes within minutes of having a chat with them. Figure 2 and Figure 3 show an example of a virtual prototype using vendor-supplied 3D STEP models and a preliminary PCB layout. The important thing here was the I/O connectors and look of the finished product, not the detailed board design, which can come later.

I find that the requests for changes come earlier, rather than later, or even worse, after the design is done using the visualization tools up front in the design process, because everyone involved has a good idea of where the design is heading and can spot conceptual errors or misconceptions earlier. And that helps the project stay on schedule.

As a side benefit of this process the mechanical fit of the product is confirmed at every step in the process. I probably shouldn't admit to how many times I have slipped up and found that some capacitor, etc. didn't fit as expected

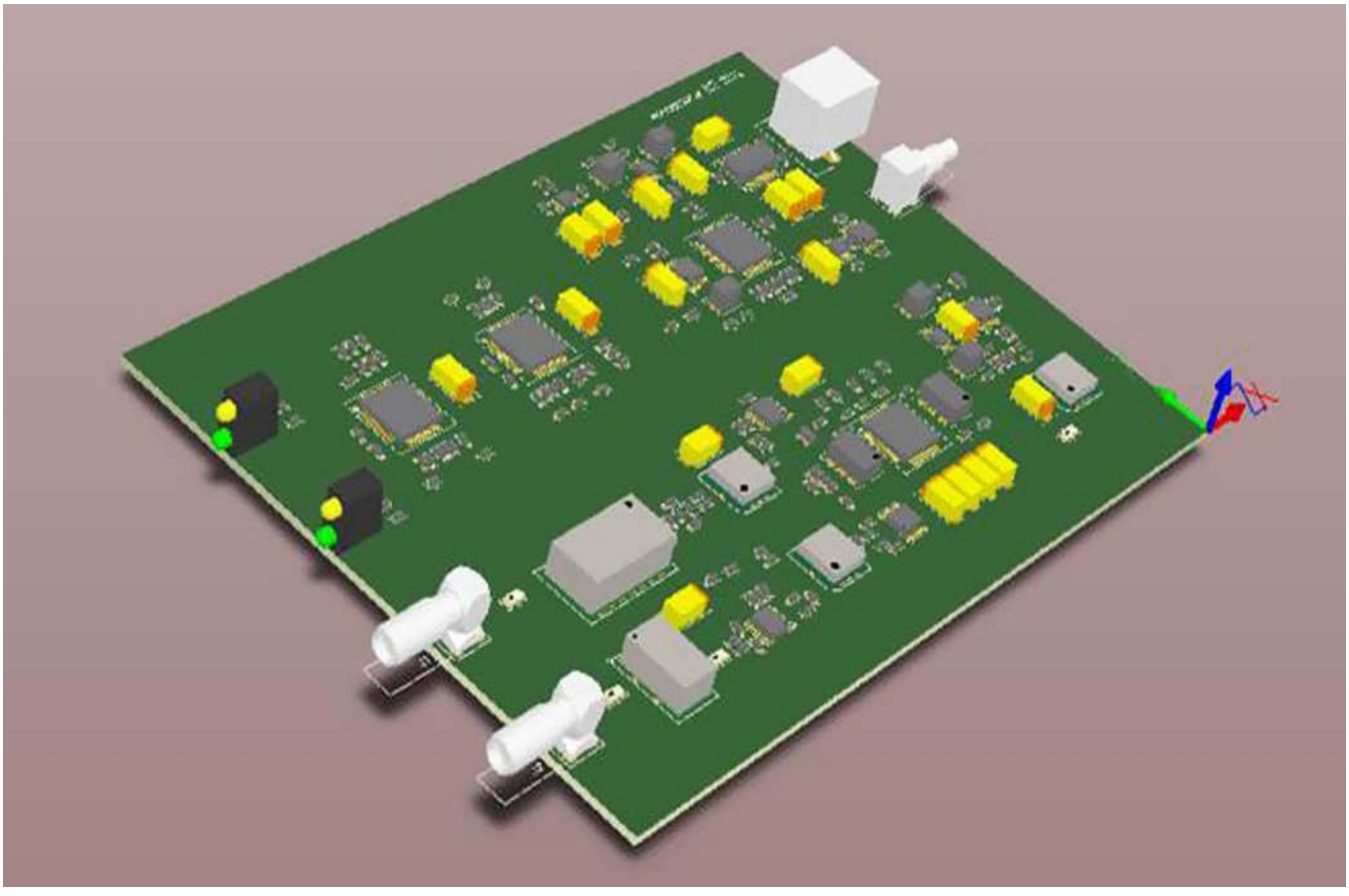


Figure 2: For this wireless project, at the preliminary stage I used the actual I/O connectors that the product was going to use and just "guesstimated" at the actual PCB parts. But this very real rendering, done in just an hour or so, really gets the point across to the client, while providing me feedback about whether I am on track with the client's vision.

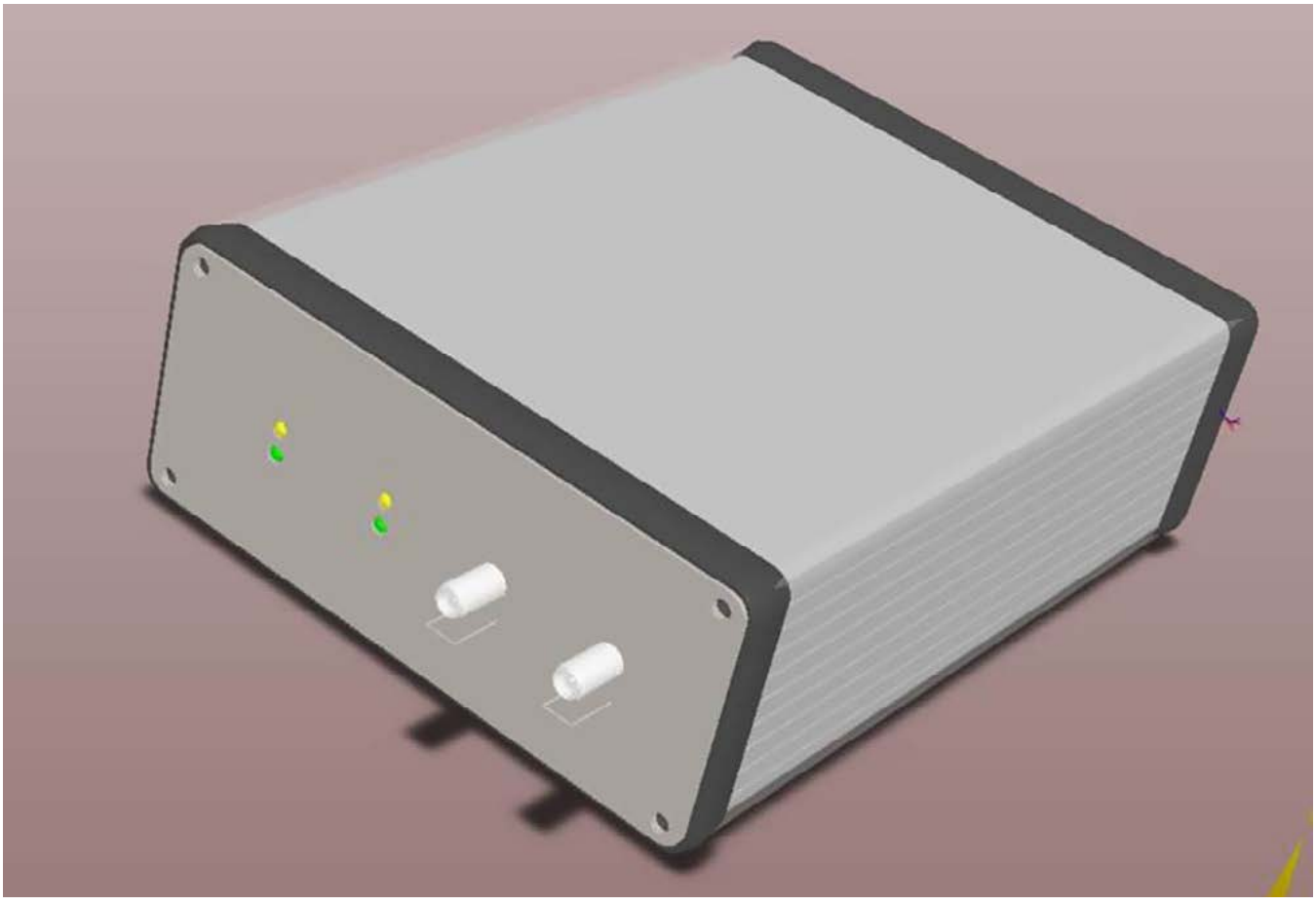


Figure 3: Taking the previous figure a step further, using vendor-supplied STEP models for the chassis a complete product can be virtually prototyped. This gives us real-time feedback even before any detailed schematic is ever drawn.

when the actual boards were built. These kinds of errors are a thing of the past now.

These virtual prototype techniques work in any situation for any type of client. If you are an employee, the development and marketing departments will appreciate the real look and feel of the proposals. If you are working with external customers, then getting the preliminary design right the first time with few changes will help to validate that everyone is on the same page, thus eliminating downstream problems.

If your design is more complex and, for instance, the housing model is not off-the-shelf, this can also be addressed. Many times the chassis maker (or mold maker) can produce suitable 3D models or you can find a mechanical designer willing to take on contract work. This is an example of the interconnected design web that we all work in now; outside resources are easy to find and engage to fill in the blanks as needed.

Pre-PCB Fabrication

Not too many years ago, we just contacted the PCB house to get their preferred stackup and design rule information. Now board shops make up an integral part of my design process. I still get the basic stackup and design rule information, but the shops can be a great source of information on suitable materials and how well they work in the intended manufacturing process. This includes information such as the higher heat required by lead-free soldering, as fabricators tend to get feedback pretty fast if their boards delaminate or have other issues in manufacturing.

Strangely enough, I find myself putting together the fab drawing first now instead of last. This helps get quotes on any proposed designs, materials, etc. As an extra bonus, this mocked-up fabrication drawing can also be passed on to the assembler for a "once over" to uncover any issues. I can recall several times where I thought I knew the requirements of the silkscreeners, pick-and-place or reflow ovens only to find out that the proposed board design didn't quite fit and needed subsequent tabs, holes or some other modification to fit the standard processes. The assembler can also take a look at the preliminary fab drawing and make recommendations based on their past experience with the materials, etc.

A good PCB house also will be up to date on the latest via hole and filled pad technologies. Keeping a good relationship with their design team will keep you abreast of the latest techniques without having to track down all this information for yourself.

A rather surprising role reversal for me is that now the PCB houses often have very sophisticated tools to do controlled impedance design, so much so that I usually get their help on defining layers and stackups to get the desired trace widths and layer thicknesses for a specific impedance instead of doing it myself. If they have the proper tools, they can also do excellent loss modeling and post-fabrication test verification also. This is a result of not only having the tools, but also using actual performance data to model the loss. After all, they make many more PCBs per month than I will ever see in my lifetime and have more data to get accurate results from.

A good PCB house also will be up to date on the latest via hole and filled pad technologies. Keeping a good relationship with their design team will keep you abreast of the latest techniques without having to track down all this information for yourself.

Post-PCB Design

Once the design is done and the PCB is fabricated, the product needs to be moved to prototype production. I have noticed that even companies with their own in-house production now may outsource their prototype production to outside assemblers just to keep the cycle time fast. The theory being that the internal shops are very skilled and efficient at volume production and optimum scheduling for shipments and the prototype process simply runs counter to this.

Many companies may also have a small SMT reflow oven and other equipment to make their own prototype runs outside the normal production flow. Setups can now be purchased for less than a thousand dollars. Another trend is for the manufacturing partner (internal or external) to use sophisticated software to model the PCB assembly before it even hits the production line. These programs take the outer layer Gerbers, soldermask, pick-and-place data, material list and part footprints and attempt to "build" the board in software.

This is really useful in finding all sorts of Gerber file issues that even the PCB fabricator may not automatically fix. Perhaps the biggest potential problem is a footprint on the PCB that does not match the actual part and prevents assembly. This is a huge potential problem and it can be caught even before the PCB is committed to fabrication by paralleling the tasks with the PCB fabrication and assembly shop instead of serially sending the design from process to process as is normally done.

The only problem I find in implementing this is that many of the assembly shops are not currently accustomed to working this early in the design process and as such don't price their services to include a separate data review, way before the board is even fabricated. So, it does take some explaining on the phone and going out of the standard process to get this level of parallelism, but this will change as time goes on and the need is realized more fully.

A simple model like the one used for DFM review at the PCB houses could be used here: Pay for the DFM up front and if no changes are required, that cost is applied to the cost of the final PCB fabrication.

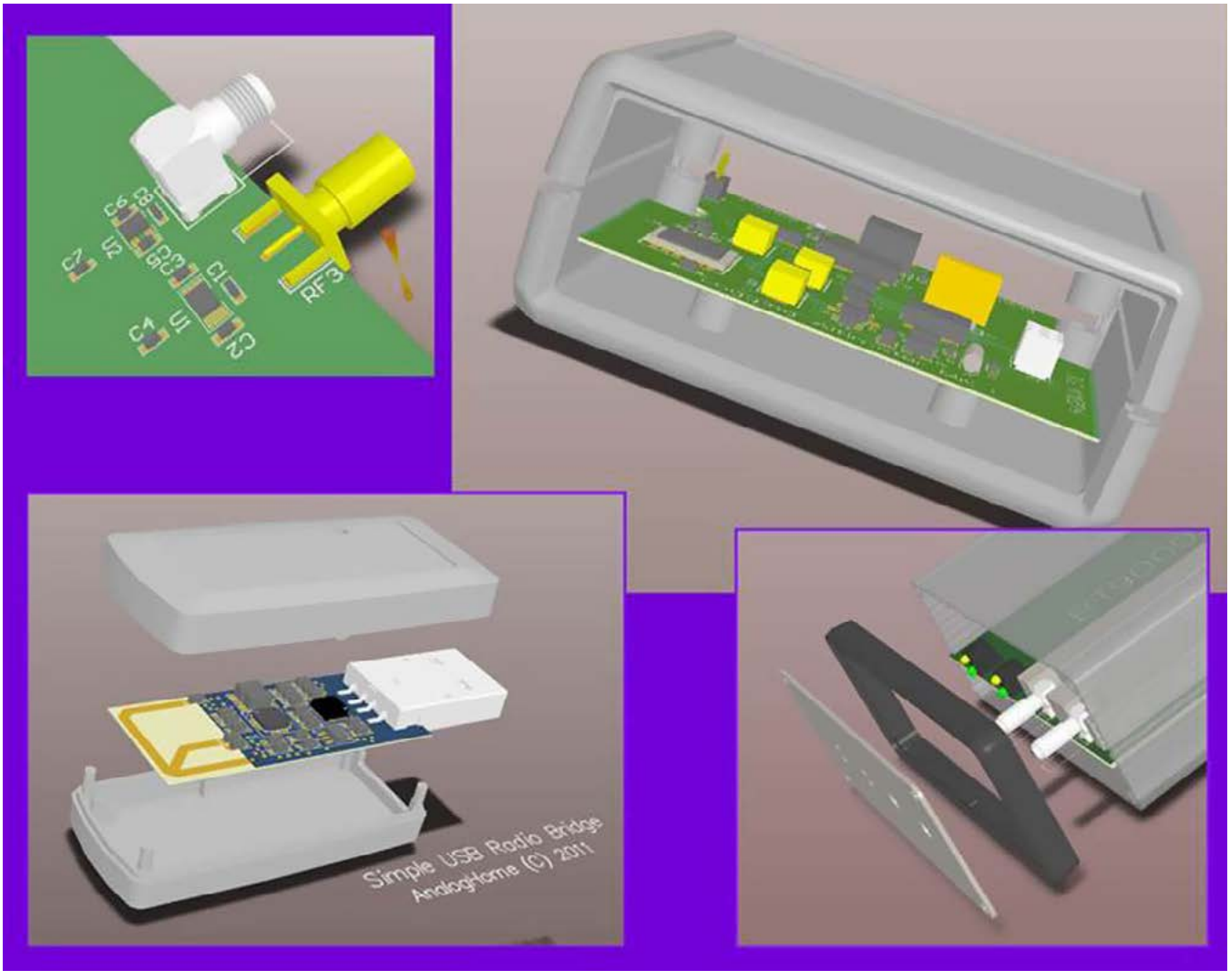


Figure 4: A simple exploded model produced in the PCB CAD tool can suffice to make detailed and quite useful assembly documentation. The advantages of using one database and software tool for this is the reduction of work duplication and fewer chances of translation errors.

Assembly Documentation

One trend in assembly is a minimal documentation of the step-by-step nature, instead using simple pictures to show the assembly steps required. IKEA uses this approach, and it is very effective especially since their products are sold to every country in the world; a good assembly pictorial is universal. These assembly pictures can be taken with a digital camera or in the CAD system itself and as we have seen, modern tools like Altium have a high level of integration with the mechanical world.

Figure 4 shows a few typical simple products in exploded view. Aids like these can be used to show the sequence, the parts required and the orientation of the various pieces. They are indispensable on the production line. Pulling these traditional mechanical engineering CAD operations up into the PCB tool has the advantage of using the same data base for the entire process, cutting down the need to recreate the same data and the chances for translation errors.

Look for more PCB tools to offer this level of integration in the future.

Improving BET

The end-result of this is really extending the PCB design process sooner up into R&D and fur-

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ther down into production in a parallel fashion. This has real advantages as the same software tool can often be used to accomplish this, thus saving time recreating work in other tools.

Allowing the client, whether fellow employees or paying customers, as well as the PCB board shop and the prototype assembler to see the direction that the project is going, up front before anything is built, makes it more likely that things will go smoothly and this can only improve the break-even time.

As Tracy Kidder so aptly wrote in his book, The Soul of A New Machine, a development project is like playing a pinball machine: If you win or are successful, you get to play again.

Keeping on schedule, reducing the inherent risk of the development process and paralleling the development process like never before can really help whatever metric is used to gauge performance. It all really boils down to BET, and how well we handle this determines whether we get to play again or not. **PCBDESIGN**

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1. S. Graves, W. Carmichael, D. Daetz & E. Wilson, "Improving the Product Development Process," HP Journal, June 1991. Click here.

2. Hageman, S., "Make a Quick-Turnaround PCB for RF Parts." Click here.

3. Altium Designer, www.altium.com.

4. Kidder, Tracy, "The Soul of A New Machine," 1981, ISBN-13: 978-0316491976, available on Amazon.

Steve Hageman has always looked for ways to decrease the cycle time and improve the accuracy of his designs. He currently serves a variety of clients designing and building analog and RF communications devices, instruments and subsystems with the goal of "Straight to Production" always in mind. Steve may be contacted through www.AnalogHome.com.

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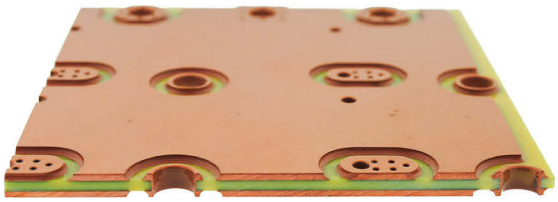

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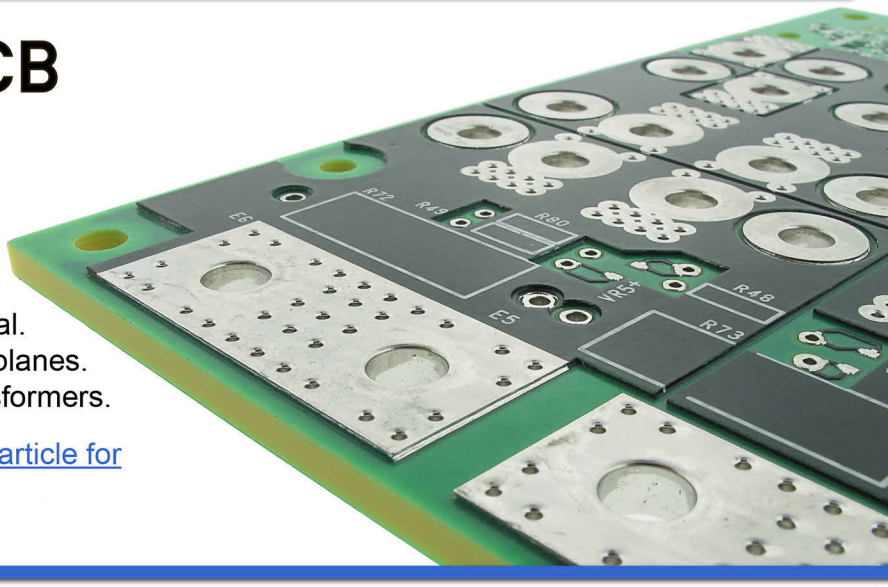

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A PCB Design Potpourri

by Mark Thompson, CID
PROTOTRON CIRCUITS

In this column, I will be revisiting topics covered in some of my older columns and fleshing them out with new, updated information. In this job, I truly learn something every day, and I'm happy to share a few notable nuggets with you.

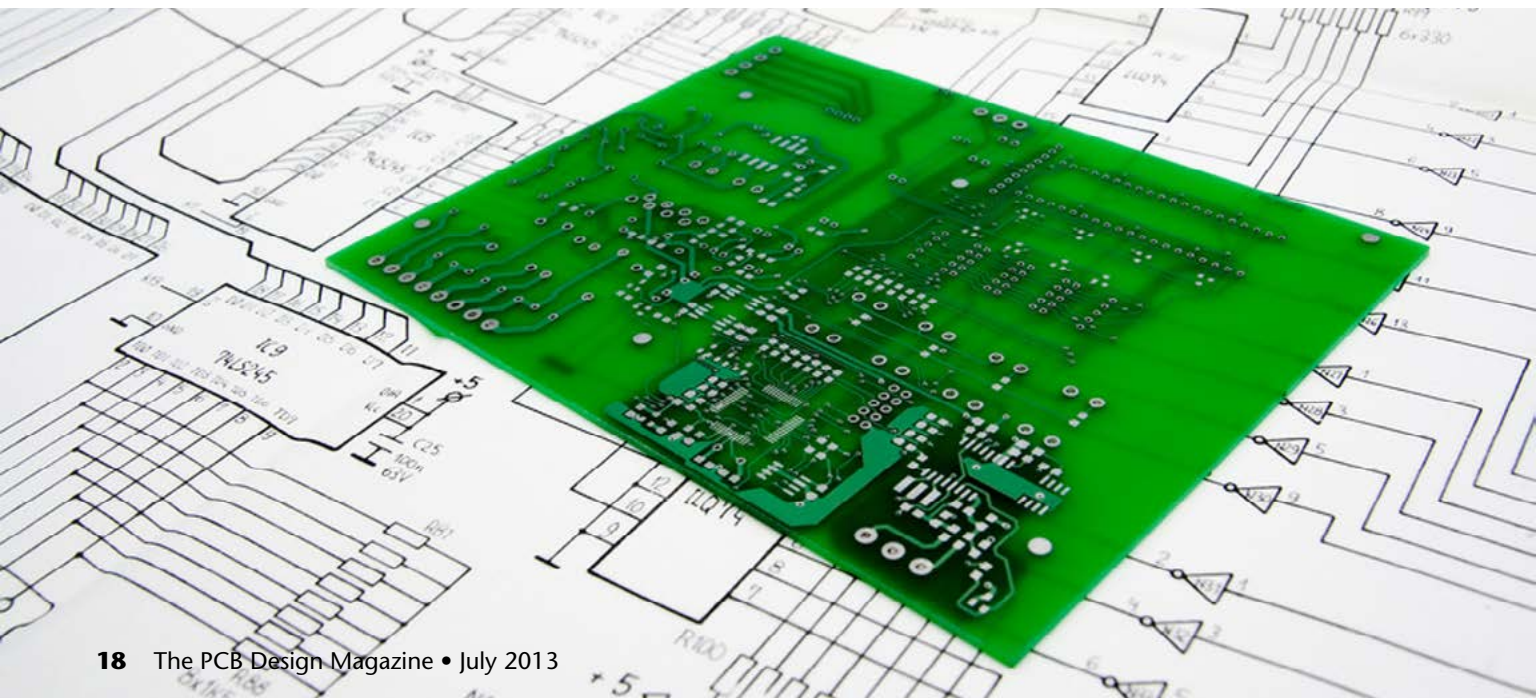
The Quote Process

Ultimately, whether it's a quick-turn or standard lead-time job, customers would like to see all quotes back within a couple of hours, not a couple of days. Additionally, they want to see accurate quotes that take into account all additional processes. It's never good when, once quoted, the fabricator comes back with additional costs for unforeseen processes. Again, this is why it is important to get a manufacturing review done if anything outside the norm is required on the drawing or quote. This includes a proper review of impedances to ensure that materials are available and the impedances work without requiring large variances in dielectric or line sizes, buy-offs for any deviations of material type or copper weights, etc.

Beyond the quote process, be sure that your fabricator is capable of all the processes necessary to ensure the board is built as expected. You want your board shop to be IPC-6012 Class 3 capable and ISO certified, and perhaps ITAR as well. Even if you can't visit the shop for a physical qualification, send them a job to quote and see how they respond. A good fabricator will be diligent and get back to you within a few hours after completing a preliminary examination of the files, impedance calculations and proposed stackup if the board is impedance/dielectrically controlled. They should also be able to let you know right away if the job does not meet their process minimums and can't be built. If deviations are allowed, a good fabricator will also have an alternative for many situations, such as a deviation for material type, starting copper weight, dielectrics or line sizes to be able to produce the job.

Impedance Control

Not long ago, a long-time customer of ours had a re-spin of a design. It happened to be a



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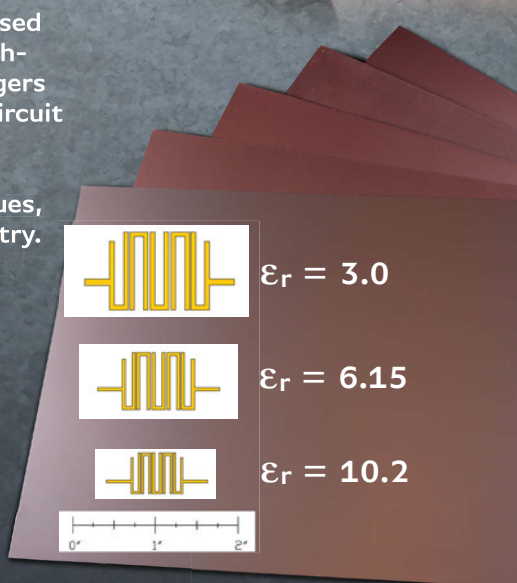

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A PCB DESIGN POTPOURRI *continues*

high layer-count multilayer PCB that previously had controlled impedance. This particular story goes all the way back to the original design and prototyping of this product overseas.

The original design came in with a standard note about controlled impedances that described the sizes of the traces to be impedance-controlled, where they resided, and their threshold and tolerance, along with a proposed stackup and standard allowance to either resize the traces or dielectrics to achieve the desired impedances. Fair enough. The job goes though the shop and ships along with impedance test results.

A few weeks later the customer needs a re-spin. This time, there are no notes on impedances, but amazingly, now the precise stackup that we used last time appears on the drawing. As you all know, this is not something I advise. A fabricator's stackup is the actual stackup to be used. Not all fabricators incorporate a "nesting" value between layers, so a dielectric listed as, say, .0074" may really press out to be .0068" or .0069" depending on the layer interfaces. This leads us to ask, are these mainly copper as full planes? If this is the case, they may stay close to the .0074" in the example here. Or are they split planes? In that case, they may press slightly thinner to fill the porous areas around the metal on that layer.

> ***What if these are pure signal layers? In that case, they may press out even thinner yet. For these reasons, I do not recommend including a fabricator's stackup on the drawing.***

What if these are pure signal layers? In that case, they may press out even thinner yet. For these reasons, I do not recommend including a fabricator's stackup on the drawing. A fabricator's stackup that accounts for all of the layer nesting can often be worse because if he's not careful, a fabricator can actually use these numbers prior to any pre-preg nesting, resulting in thinner-than-expected dielectrics and mismatches in impedance.

Fab Process Edits

What types of edits are performed on the artwork files before processing? One of the first edits done in a typical CAM department prior to fabrication is an etch compensation for image. This is an increase in feature size of the artwork that includes all lines, pads and other features in copper grown to account for the known loss at an etcher. The general rule of thumb is for every half ounce of starting copper, a fabricator will do a half mil of etch compensation to the artwork so that after etch, the lines/features are at the original size. An example of this would be a .005" line with a .005" space on 1 ounce starting copper, which would then have a 1 mil etch comp on the artwork, so the lines prior to etch would be .006" lines with .004" spaces.

Does imposing an etch compensation ever cause a problem? It certainly could. If the etch compensation cuts into the available air gap/space value to the point when you cannot produce the part based upon your process minimums, you may receive a phone call from the fabricator asking to start on a lighter copper weight (and therefore have less etch comp imposed so that available air gap or space value is not compromised.)

This is not to be confused with drill compensations. Depending upon the surface finish, we typically drill some .004"–.005" over the finished hole size (or FHS as depicted on your drill drawing). Even for the most experienced PCB designers, the lack of this type of knowledge can easily result in insufficient pads size at best or, at worst, gap violations resulting in either a "no bid" or a request for a lighter starting copper weight.

Knowing Your Customers' Desires

More than ever we need to pay special attention to our customers' desires and idiosyncrasies. Over many years of building PCBs for the same customer, a fabricator amasses a certain amount of additional knowledge about the customer. For instance, special features on the artwork that would cause delays at other fabricators are easily identified as intentional features by a fabricator who has already asked the right

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questions. It is therefore crucial that these small details are documented and archived in a database of customer-specific requirements. Having said that, there are certainly times when deviations from "what has been" and "what is" warrant that these questions are to be asked again. Here again, it is good to have that background knowledge of previous dispositions, so that the questions can be answered easily and with less delay.

Another example of this would be things not necessarily noted on a drawing or "read me" file, but are known as a customer's special "hot buttons" or undocumented requirements. This includes even things like packaging and shipping requirements not noted by the drawing or purchase order. With so many customers comparing fabricators these days and scrutinizing the way we deal with artwork or fabrication snags, having that undocumented knowledge documented so that the questions or concerns be quickly resolved can give you a big leg up on the competition. This frequently means the difference between and win and a loss when quoting.

Thanks again for your time. **PCBDESIGN**

Mark Thompson is in engineering support at Prototron Circuits. To contact him, click here or call 425-823-7000. Feedback is appreciated.

Flexible Yarn Conducts and Stores Electricity

UOW scientists have developed a strong and flexible yarn that conducts and stores electricity and could be used to create wearable medical devices and smart clothes.

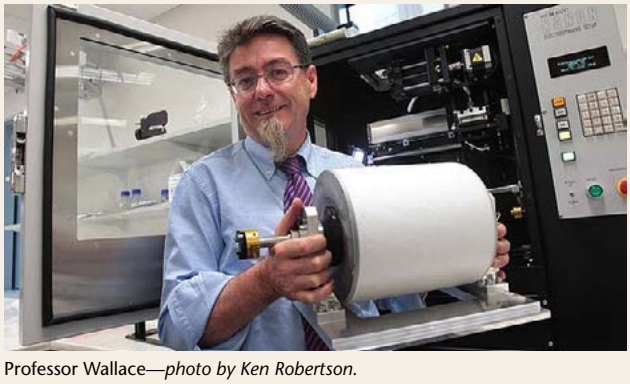
Researchers from the ARC Centre of Excellence for Electromaterials Science (ACES) at UOW worked with an international team of engineers to develop a novel way to turn small fibres into powerful batteries with ultrafast charge and discharge rates.

The result, published in the journal Nature Communications, is a flexible, wearable supercapacitor yarn—about the width of a human hair—that is made by weaving two nano materials together to form a super-strong carbon nanotube. Hundreds of layers of nanotubes, which are coated with small molecules of plastic, are woven together with a thin metal wire. This is then spun into a yarn in a similar way to how you would spin wool into thread, ACES Executive Research Director and Australian Research Council laureate fellow, Professor Gordon Wallace, said.

"The highly functional fibres can be integrated into complex 2D and 3D structures using our integrated knitting braiding machines. These facilities were recently commissioned as part of an Australian National Fabrication Facility Materials Node expansion," said Wallace.

The yarn's flexibility means it can be knitted or sewn into clothing to power wearable electronics, which could be used to monitor movement during training or physiotherapy or to power high-tech fashion accessories. The mechanical properties of the yarn mean it can add strength to composites often used in automotive components and could be especially useful in electric vehicles.

Professor Wallace said the outcomes from this research were a direct result of the ability to combine expertise and facilities from across the globe to tackle a critical area of research—developments of new materials for energy storage.



Professor Wallace—*photo by Ken Robertson.*

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PCB007 News Highlights

AT&S to Close PCB Plant in Austria

In light of the continued decline in the market for the technology used in single-sided PCBs and a lack of options for utilising available capacity, AT&S Austria Technologie & Systemtechnik Aktiengesellschaft has made the decision to close its production facility in Klagenfurt at the end of 2013.

New Etching Tech Could Revolutionize PCB Fabrication

The growing functional range of smartphones, digital cameras, and tablets requires a high level of integration density in the semiconductor field and the miniaturization of electronic modules. Until now, the use of faster microchips was virtually impossible due to increased heat generation.

FastPrint Completes Acquisition of eXception's PCB Business

Mark O'Connor, CEO of eXception Group Ltd. commented, "This successful conclusion comes after a period of due diligence where all areas of the eXception business continued to work diligently and successfully toward its end-of-year goals…"

Sumitomo Begins Mass Production of New Type FPCs

Sumitomo Electric has developed a new flexible printed circuit with circuit layers connected by conductive paste based on the company's original metal nanoparticle technology. In April of this year, the company began full-scale operation of its mass-production line at Minakuchi Works.

IPC: PCB Book-to-Bill Ratio Highest Since July 2010

"North American PCB sales in April continued to lag behind 2012 levels, although sales in the flexible circuit segment are strengthening," said Sharon Starr, IPC director of market research. "Rigid PCB orders for the month exceeded last year's orders and continued to push the book-to-bill ratio up to a strong 1.10."

Spirit Circuits Invests in Viking Test's Optima System

Innovative PCB-manufacturer, Spirit Circuits, has recently invested in a high-technology CCD camera AOI system from equipment provider Viking Test. The system, Optima AOI, which was installed this May, uses high-resolution CCD camera systems and a unique software algorithm.

IPC: Economic Growth Ahead

Global economic growth is picking up, but the continuing economic crisis in the 17-nation Euro area is delaying a meaningful recovery. Leading macroeconomic indicators and electronics supply chain indicators point to slow growth in the second quarter of 2013.

Viasystems Newest Member of EICC

Viasystems Group, Inc. has been accepted as a member of the Electronics Industry Citizenship Coalition (EICC), a coalition of the world's leading electronics companies working together to improve efficiency and social, ethical, and environmental responsibility in the global supply chain.

Global PCB Industry Could Reach $93.9 Billion in 2017

According to a new report from Research and Markets, the global PCB industry is forecast to a CAGR of 8.1% during 2012-2017. By regional growth rates, Asia Pacific (APAC) is likely to be the leader of the industry over the next five years.

AT&S Sales Up 5%; Venturing into IC Substrate Market

The company finished the financial year 2012/2013 with sales of approximately EUR 542 million, 5% higher than the previous financial year. AT&S also plans to focus on building up its requisite expertise for the production of IC substrates and to prepare for the entry into the market.

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Increase Productivity and Profit: A Fresh Perspective

by Tom Hausherr
PCB LIBRARIES

SUMMARY: There are a myriad of ways to adopt a design for profit (DFP) approach. In this article, Tom Hausherr addresses one surefire method: increase your productivity.

Increasing productivity will result in increasing profit all the way from engineering and PCB layout through fabrication and assembly. Increasing productivity can also make you more competitive, as well as help you earn a pay raise or a higher position in the company. As anyone who constantly strives for perfection, high quality, reduced errors and cost knows, every now and then it's a good idea to start with a clean slate and question everything.

After 40 years in the PCB design industry, I can offer the PCB designer plenty of tips that will increase productivity. Consider the following essential factors.

• Avoid duplication for effort. Create "start files" for various layer configurations and trace/space rule sets. This may require you to perform impedance calculations to determine layer stackups that produce the best results.

• Create documentation for your design flow to consistently improve your process.

• Create checklists for every aspect of the PCB design process to ensure you don't miss any details. The design flow checklists should be broken down by basic functions like library construction, database setup, part placement, rule creation, routing and post-processing. It does not make any difference how many PCB layouts you've done in your career, no one can remember all the details that go into a PCB layout.

• Create a drafting library that includes details for the silkscreen and fabrication drawing.

• Work with your PCB manufacturer to refine your fabrication notes.

• Create your standard title blocks to automate the creation of fabrication and assembly drawings.

• Create a PCB library system so that you can easily build new parts and locate existing parts. There is nothing more frustrating than

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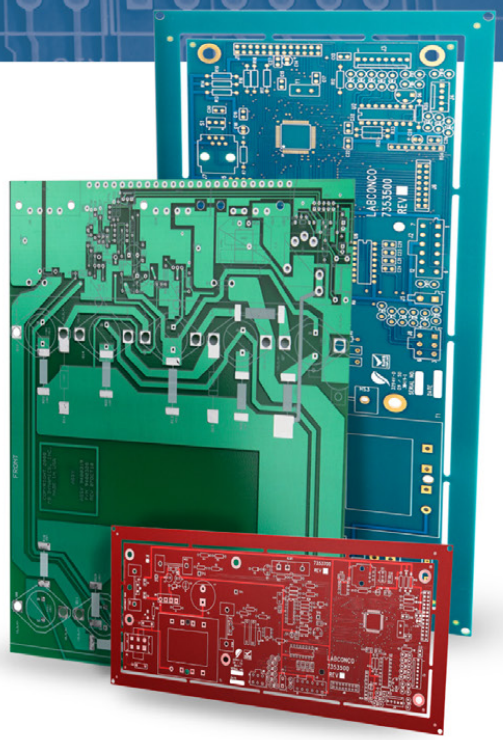

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not being able to quickly locate library parts that you built in the past.

• Whatever working units you use for PCB layout, your PCB library should be constructed with the same units. So if you're designing in mil units, all of your library parts should be constructed in mil units. Mixing units can be confusing, and confusion leads to errors, which cause rework. I know that many designers build their PCB library in metric units and then place them in a mil unit PCB layout. This is OK, but it lacks full optimization. My recommendation is to do everything in metric millimeter units. I have found that metric PCB layout is vastly superior to the imperial measurement system. Once you are successful in designing in metric units, you will never return to imperial unit PCB layout and your productivity will increase. But the mechanical engineer must also produce drawings in metric units.

• Create a fabrication quote form and Gerber data Readme files that explain all the data files you provide the manufacturer.

After a PCB designer has completely set up all of these items, the only recurring task is PCB library management. The data coming from the electrical engineer (EE) to the PCB designer is mostly straightforward, but the EE can make life tough on the PCB designer if he lacks the important information necessary for the PCB layout. The accuracy and completeness of this data directly affects the PCB layout turnaround time:

1. Schematic
2. Bill of materials
3. Netlist
4. Design rules
5. Mechanical constraint drawing for board outline and mounting hole locations
6. Component datasheets

Of all these items, it's the "component datasheets" that most EEs seem to lack, even though they have possession of them at some time during the schematic creation. Why the engineer does not save all the component datasheets or even web links to the datasheets is a mystery to me. Component datasheets are necessary for component package dimensions and/or recommended footprint pattern for library verification or construction. Often, the engineer will tell the PCB designer that the BOM has sufficient information so that the PCB designers can web-search the component manufacturer's part number and hopefully locate the correct datasheet. It is very time consuming for the PCB designer to gather all the component datasheets in the BOM. When the PCB designers collect all the datasheets, they have to figure out which component package they already built the library parts for and which ones are new and require new PCB library construction. This is very time-consuming and the biggest waste of time is due to duplication of effort. So I will focus the remainder of this article on automating CAD library solutions.

Over the years CAD vendors have vastly improved schematic tools and PCB layout features like autorouters. Until a few years ago library construction in the CAD tool had not changed much. Library construction remains one of the most error-prone and time-consuming PCB layout tasks and it's not getting any easier. Component manufacturers are intentionally creating unique packages that require custom footprints and the number of new component packages on the electronics market increases every day. To top this off, there is no mapping or cross-reference of component manufacturer logical part numbers to physical package dimensional data.

It almost seems that the electronic industry is in a state of chaos when it comes to components due to the massive availability of over 50 million electronic device part numbers and 500,000 different component package styles. When you factor in 3D STEP modeling (Figure 1) PCB library organization gets even more complicated. If you can imagine that all 50 million logical part numbers require a schematic symbol library part that should be linked to one of the 500,000 component package footprints, which are in turn linked to the 3D STEP model.

There are simultaneous multiple sources trying to automate all of this information in an attempt to reduce duplication of effort and increase the speed of the library creation and database organization to track existing libraries. However, this fragmented effort is only

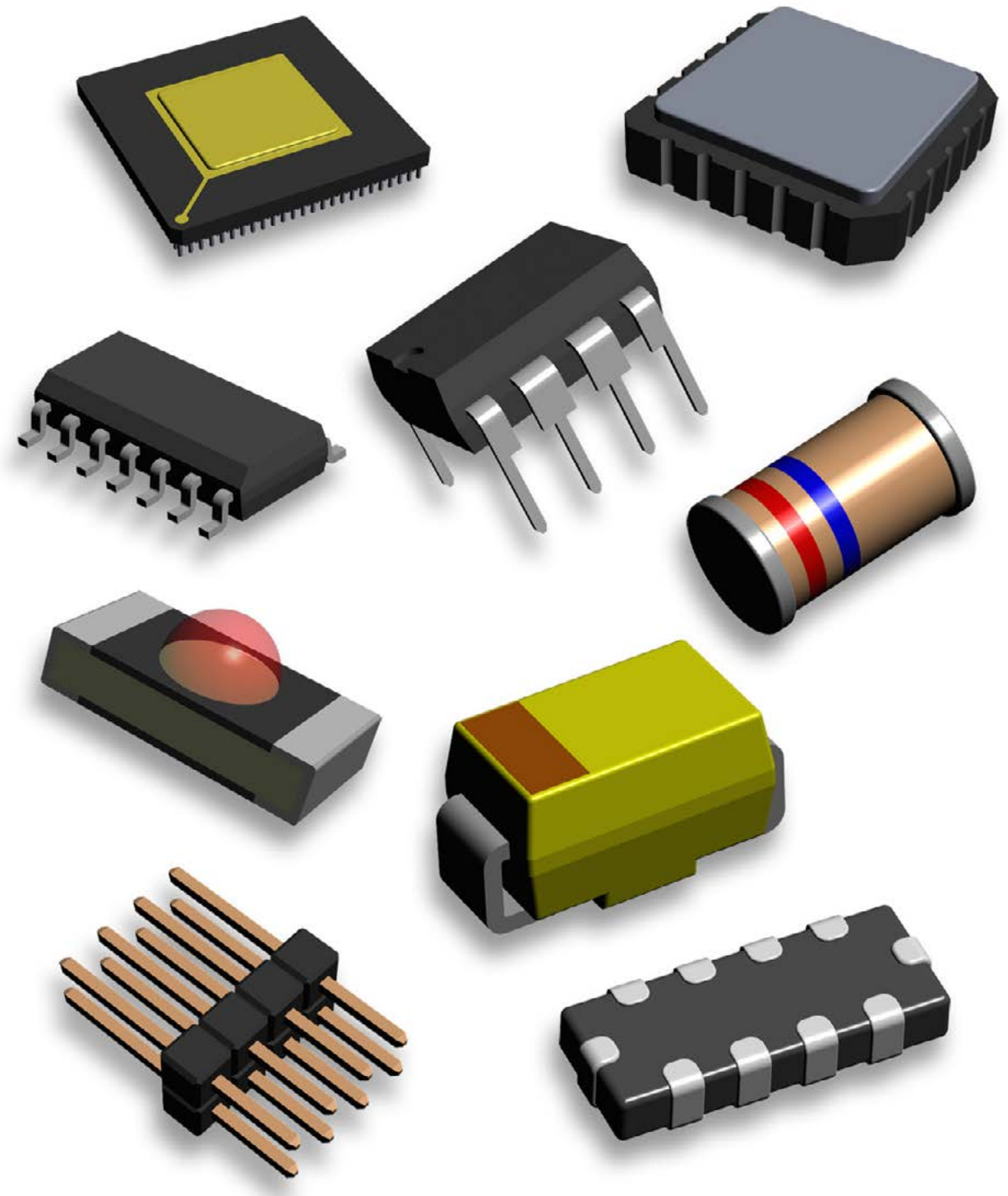

Figure 1: 3D modeling.

causing further confusion and chaos because everyone has a different methodology standard for library creation. A standard schematic symbol library is impossible to create because the symbols are used in various electronic products and the symbol pins are constantly being rearranged to eliminate lines crossing each other. Plus, engineers are particular about the way the schematic symbol pins are arranged.

If you gave 10 engineers the same compo-

nent datasheet and told them to create the logical schematic symbol for that part, the end result would be 10 different schematic symbols. So having the component manufacturers, CAD vendors and third-party library vendors provide schematic symbol library parts is not the solution; the symbol would be edited by the EE prior to using it. This is one big reason why engineers don't share their schematic symbol libraries with other people because they don't meet other EEs' quality standards. However, having a basic schematic symbol to start with is better than no symbol because revising existing symbols is faster than creating new symbols from scratch.

For the PCB footprint library parts, there are many construction aspects that need to be considered. Some of these aspects are pad shape (oblong, rectangular, D-shape or rounded rectangular), units (metric or imperial), footprint rotation (Pin 1 upper left or lower left), environment level (most, nominal, least or user), outline line widths (silkscreen, assembly, polarity, 3D model and courtyard), footprint/padstack name, and the list goes on. So anyone who provides a PCB library can never satisfy the unique requirements for every company. Any company that has developed strict library construction rules will never use canned library parts provided by the CAD vendor, the component manufacturer or the third-party developer. Can you imagine a CAD library that was created by downloading parts from different vendors with different rules? Your PCB layout would look more like a circus than neat organized artwork.

3D model libraries are also vastly different due to the unlimited construction techniques available in the mechanical drafting tools. There are dozens of ways to create the same 3D model. Depending on the level of quality you require, finding 3D model libraries that you like can be very time consuming. In fact, it can take so much time that in the end, you will likely opt to either use a lower quality part, or create the 3D model manually yourself.

> ***I am convinced that by the next generation, productivity solution will be based on the latest trends of web-based technology: cloud computing and central data storage.***

To add another layer of complexity to library construction, some companies assign a corporate part number to every library part and rename the library part to match the corporate part number. To me, this is one layer of bureaucracy that is unnecessary and time consuming and everyone who does this has a different reason why they do it.

I have been trying to automate library creation and documentation throughout my entire CAD career. I tried all different approaches to solve this age-old dilemma by manually creating PCB library parts and offering them to the industry, printing books that document the library, creating multiple software calculators and spreadsheet applications to track library development. I have seen what works. I have also seen what doesn't work and my team figured out why. I am convinced that by the next generation, productivity solution will be based on the latest trends of web-based technology: cloud computing and central data storage. Taking advantage of this technology is the end solution of elimination of duplication and offering data that can be acceptable to everyone. Here are the guidelines that will offer a global automated solution that would far surpass those established years ago on old technology.

1. Create a software tool that uses component package dimensions to auto-generate PCB footprint library parts. The tool would have to be able to allow the user to completely define personal rules for every aspect of footprint creation standardization.

2. The software tool would have to store the component dimensions and necessary attributes like the footprint name, physical description, mfr. case code, mfr. name, mfr. logical part number, mfr. logical description and mfr. logical datasheet web links. This data must be stored in a human readable ASCII format to allow the exchange of data files throughout the industry.

3. Create a website to allow the industry to gather and upload all of the component manu-

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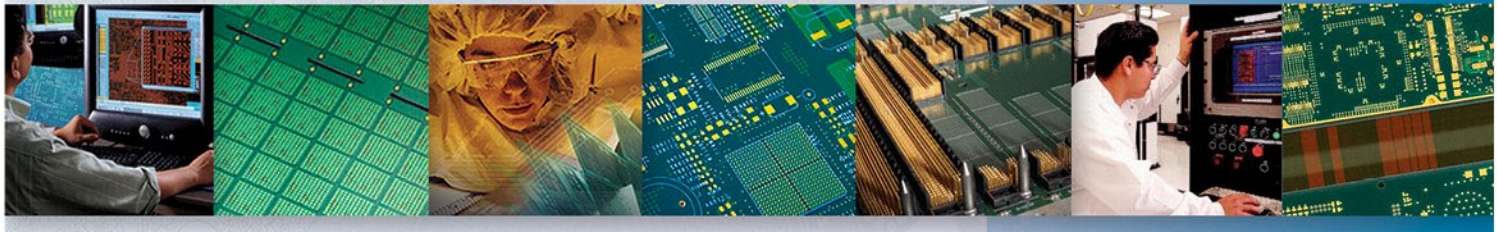

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facturer's part numbers in the neutral data format. Why does this need to be an industry effort? Because no single organization can create over 50 million part numbers and keep up with new electronic devices being introduced daily. Everyone should be able to "Search > Find > Download > Import" the neutral data files into the software program to batch build all the necessary library parts required for any specific PCB CAD tool using customized rules established created by the company managers or PCB designer or use the IPC-7351 rules. This neutral data would also become the library documentation.

4. The same tool that automates footprint creation using component dimensions should also auto-generate the 3D STEP model so that the 3D model name, rotation and origin matches the footprint 100%.

5. The same tool should be able to create schematic symbols by importing neutral CSV file data and organize the pin locations using the recommendations from the component manufacturer's datasheet. The schematic symbol created by the tool is generic and will probably be modified by the EE who wants to rearrange the pin locations. But this is much faster than starting from scratch.

Remember that anything you can do to increase your productivity will likely increase your profit. And as we have seen here, there are a variety of ways to raise your productivity level. **PCBDESIGN**

Tom Hausherr is the founder and CEO of PCB Libraries. He can be reached at Tom.Hausherr@pcblibraries.com.

Designers Take Control: Design for Profit

by Barry Olney
IN-CIRCUIT DESIGN PTY LTD | AUSTRALIA

Completing the project on time and within budget minimizes costs. Reducing the design cycle generates higher profits due to shorter time to market which in turn extends the product life cycle.

Design for profit (DFP) typically eliminates inefficiency in the traditional design process. Reducing part count and simplifying assembly results in lower cost, better quality and higher profits, all delivered before manufacture begins. DFP also encompasses design for manufacturability (DFM). DFM is the practice of designing board products that can be produced in a cost-effective manner using existing manufacturing processes and equipment.

DFP is gaining more recognition as it becomes clear that the cost reduction of printed circuit assemblies cannot be controlled by manufacturing engineers alone. The PCB designer now plays a critical role in cost reduction.

However, as we grow as PCB designers our focus changes from basic considerations to more complex system level initiatives. PCB designers require attention to detail, an artistic talent, the capacity to accept change and the ability to deliver on time under constant pressure. Also, the requirements for a PCB design can vary considerable from one design to another. However, attributes that increase profit are self-taught and require time to develop.

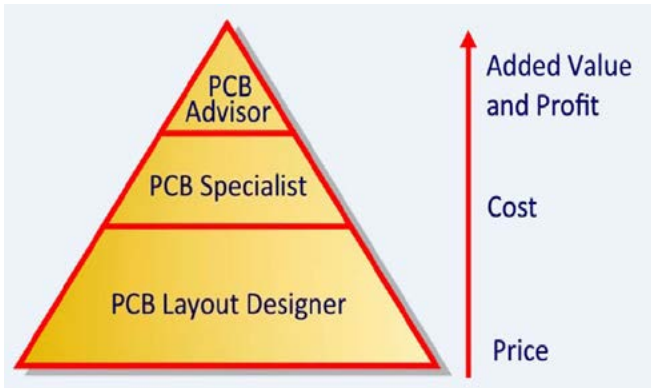

Figure 1. Three levels of the PCB designer. Which level are you?

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DESIGNERS TAKE CONTROL: DESIGN FOR PROFIT *continues*

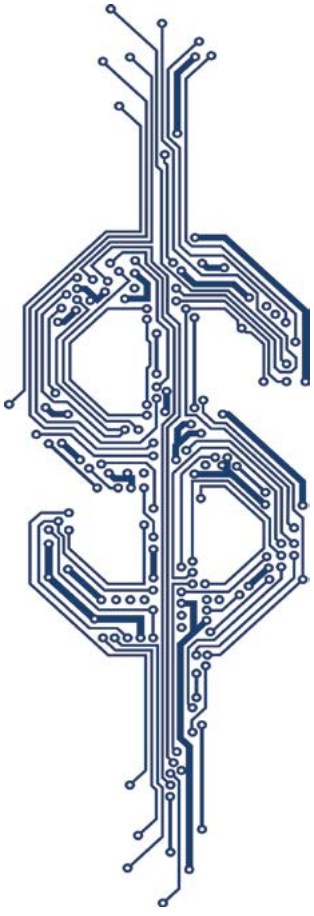
It helps to understand the three levels of the PCB designer:

1. The PCB Schematic and Layout Designer

I guess this is where we all first started many years ago. His focus is on a single event: the current product and the ability to design at the technology level involved in the project. He uses features within the tools to enhance the design. He takes price of components into account in order to reduce the total price of the build. He absorbs information such as design rules and best practices to constantly improve his skills.

At this level of knowledge, the enhancements that can be made to the design include basic setup costs:

- Standard design rules: Consistency encourages good design practice and streamlines design
- Technology: Trace width/clearance, via type and complexity 4/4 technology and through-hole vias are cheaper than 3/3 and microvias
- Layer count: The fewer the layers and the fewer number of core materials the cheaper the fabrication
- Hole size: Reducing via holes below 8 mils will incur more cost
- Copper thickness: Thinner copper is cheaper but there are trade-offs between cost and reliability
- Stencil apertures: Correct apertures improves production yields



2. The PCB Specialist

This guy manages other PCB designers, or runs his own business, and has years of experience. He has a business agenda and focuses on the overall costs of development and manufacture and the benefits he can deliver from a strategic point.

The PCB specialist's interest lies in the development, fabrication, assembly and testing processes. He improves the process by reusing existing design snippets, standardizing library components, to reduce stock holding costs, panelizes boards for mass production and schedules delivery times to work in with the requirements of the testing and manufacturing sectors.

The PCB specialist reduces overall cost by employing the following:

- Design reuse: Reuses existing snippets that saves time and adds confidence
- Panelization and standard form factor: Standardizes jigs to reduce production, assembly and testing costs
- Test fixture reuse: Minimizes the movement of test points during revisions
- Dielectric materials: Selects correct materials for performance and price
- Symmetrical stackup: Ensures symmetry which reduces wrapping during both fabrication and reflow
- Standardization of library components and values: Reduces stock holding costs and assembly setup time
- Component packaging: Selects packages that produce higher yields and reduce size
- Volume production and off-shore manufacture: Higher volume—the less the cost
- Delivery time and premiums: Plans the delivery to scheduled production

3. The PCB Design Advisor

The PCB design advisor is a design consultant who advises others on the best possible outcome for the project. He works at the executive level to add value and profit to the solution. He focuses on the overall product reliability, system integrity and the solution space from concept to final market deployment.

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DESIGNERS TAKE CONTROL: DESIGN FOR PROFIT *continues*

His insight into development is profit making at the competitive level. He controls time to market, competitive advantage and the market window.

The PCB design advisor leverages the following:

- Operating environment: Considers the entire product environment, heat flow, EMI, etc.
- Reliability: Performs signal integrity and timing analysis to improve product reliability
- System integrity: Analyses the stackup, PDN, signal integrity, crosstalk and EMI
- Competitive advantage: Ensures ease of use, speed and functionality
- Time to market: Reduces development time
- Market window: Ensures the product is in the market longer to increase profits

Allow me to put on my marketing hat for a moment. If we are designing a computer-based consumer product, then the market window (time to sell the product) is probably about one year. Let's say that the design fails to work properly—or at all—on the first build. The next iteration of the board will typically take three months, delaying the time to market by one-quarter of its life cycle. If the sales department expects to make $10 million on this product during its projected life, then the profit is reduced by $2.5 million (not to mention the redesign costs). This is where the PCB design advisor comes in.

Having the project completed on time and within budget means that costs are cut by reducing the design cycle and generating higher profits due to shorter time to market and an extended product life cycle.

Price and cost are two different things. The price paid to develop the product is an investment—not a cost. But, it is important to remember what it costs if things go wrong. For each day, week or month that the project is delayed, costs not only in additional labor but also in lost opportunity in getting you product to market.

In a previous column, Intro to Board-Level Simulation and the PCB Design Process, I mentioned that the cost of development is dramatically reduced if simulation is employed during the design cycle. If changes are made late in the design process, then it takes more time, people, material and therefore money to complete the project. The advantage of board level simulation is that it identifies issues early in the design process and rectifies them before they become a major problem.

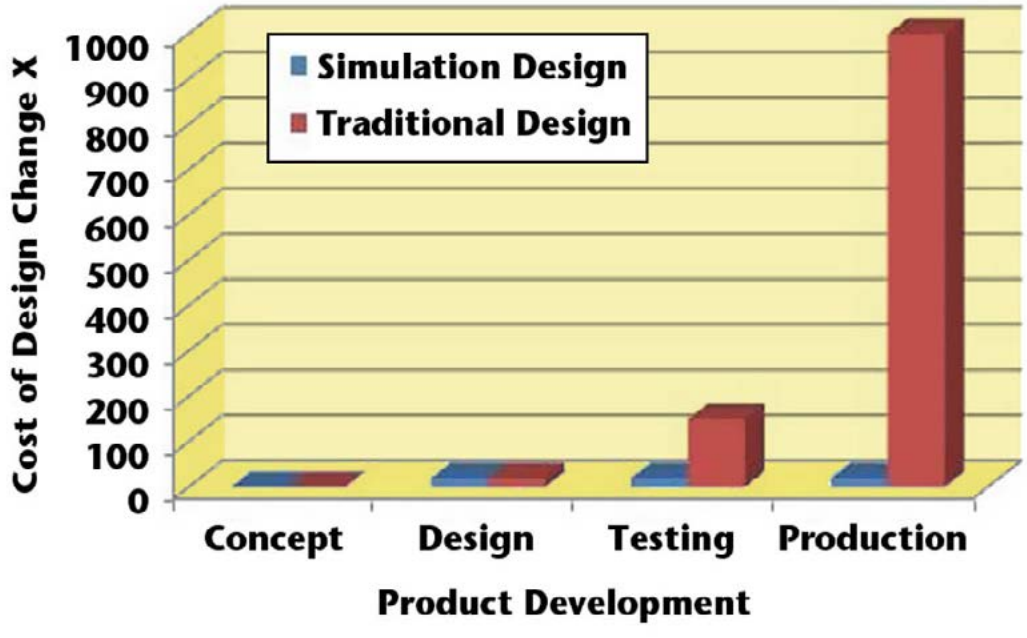

Figure 2: The estimated cost of design change during product development.

As can be seen from the graph in Figure 2, design changes that occur in the conceptual stage cost nothing; during the design stage requires just a little extra time, and during the test stage means that you have to go back one stage and

redesign. And during production, or—worse still—in the field, it can cost millions to fix and possibly damage your company's reputation.

However, using board-level simulation cuts costs: A pre-layout simulation identifies issues in the conceptual stage so that they can easily be avoided. And, the post-layout simulation catches the issues during the design process eliminating the potentially disastrous final stage changes. Of course, we also need to keep our eye on the ball during the entire design process catching any small issue before it becomes a major problem.

The PCB design advisor adds value and profit at many levels by performing reliability and system integrity checks before and during the design process:

1. Plans the board stackup from the beginning, ensuring that both single-ended and differential impedances conform to the technology requirements. And, ensures that the selected materials are available from the chosen fabrication shop—this step is regularly missed.

2. Ensures that there is a stable power delivery system. Power distribution network (PDN) analysis, of all supplies, ensures that the AC impedance is low over the entire spectrum. The PDN design is also a very important part of the conceptual design process that is often overlooked.

3. Performs a pre-layout simulation to calculate placement and routing constraints. Pre-layout simulation allows the designer to predict and eliminate signal integrity, crosstalk and EMC issues early in the design process. This is the most cost-effective way to design a board with fewer iterations rather than starting with the post-layout simulation.

4. Ensures that the correct design rules, based on simulation, are set up prior to placement and routing. Design rules should be defined and attached to critical nets in the schematic. This allows the engineer to transfer his desired intent, with regard to placement and routing, to the PCB designer without the information being lost in the process.

5. Performs a post-layout simulation to ensure the timing is to spec. Simulates trouble spots identified by the batch analysis in order to further resolve the issues with greater accuracy.

You are not just a PCB designer: You need to add value to each design and continue to increase profit for your employer. A good PCB designer prevents rather than reacts to problems.

Points to remember:

- The PCB designer plays a critical role in cost reduction
- There are three levels of PCB designer: PCB layout designer, PCB specialist and PCB design advisor
- Having the project completed on time and within budget, means that costs are cut by reducing the design cycle and generating higher profits due to shorter time to market and an extended product life cycle
- The cost of development is dramatically reduced if simulation is employed during the design cycle
- The PCB design advisor adds value and profit, at many levels, by performing reliability and system integrity checks before and during the design process
- A good PCB designer prevents rather than reacts to problems **PCBDESIGN**

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2. Intro to Board-Level Simulation and the PCB Design Process,Barry Olney

3. Board Level Simulation and the Design Process: Plan B: Post Layout Simulation,Barry Olney

4. The ICD Stackup and PDN Planner can be downloaded from www.icd.com.au

Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. The company is a PCB design service bureau that specializes in board level simulation, and is the developer of the ICD Stackup Planner and ICD PDN Planner software. To contact Barry, click here.

CONNECTING THE DOTS

The CAD Library

by Jack Olson, CID+

Before we look at libraries, it will be helpful to have a basic understanding of how circuit boards are fabricated. Study the 10 steps listed in Figure 1, which briefly describe the fabrication process. Notice that the final result in the last step is a surface mount capacitor labeled, "C1," and each end of the capacitor is connected to a plated through-hole ("via").

Start with double-sided cores, thin sheets of insulating material (usually fiberglass) copper-plated on both sides.

Print circuit patterns for all inner layers on both sides of the cores using an etch-resist material.

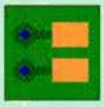
Etch away the copper that isn't protected by the etch-resist, and then strip the resist off.

Laminate with two more single-sided copper layers for top and bottom, and insulating sheets in between.

Drill the holes that will be used to connect the layers of circuitry together (unplated holes may be drilled later).

Plate the hole walls and surface layers with copper.

Print and etch the patterns for the outer layers (top and bottom) using a similar procedure as the inner layers.



Cover the board with a protective coating called soldermask, except where exposed circuitry is desired.

Plate the exposed circuitry with a final finish to protect and maintain solderability after storage & handling.

Apply silkscreen (epoxy ink) as a reference legend.

Figure 1: Circuit board fabrication in 10 easy steps.

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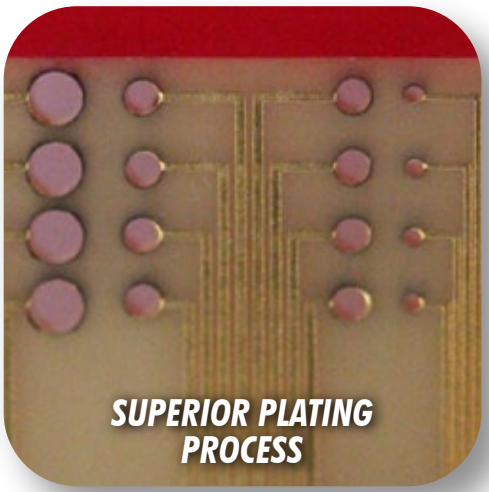

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THE CAD LIBRARY *continues*

Now we'll use this small example as our desired goal. Let's assume that we need to design a small board that supports a single capacitor connected to two plated holes. This simple design goal will be enough to illustrate several important concepts.

The provisions made for the component named C1 in this example are nothing more than two rectangular conductive areas (lands), connected by short copper connections (traces) to the plated holes. We need to keep the green soldermask away from those areas, where the solder will join the lands to the component pins, and we will also add white ink to help identify the component on the finished product. This is the type of land pattern that we would create for a surface mounted capacitor, or for any other two-pin surface mounted component (resistor, diode, LED, etc.). Since there are different sizes of surface mount components available, the conductive land on the circuit board must be sized appropriately to ensure good solder joint formation.

Although modern components are dimensioned using metric units, the majority of two-pin discrete components were defined using inches when they were developed a few decades ago. For example, a common component style is the 0805, which is nominally .08" long and .05" wide. The next smaller size was the 0603, which is .06" x .03", and using the same naming convention, there are component styles named 0402, 0201 and smaller, and also larger styles named 1206, 1210, 1812, 2512, etc.

Knowing the physical size of the component will allow us to determine the optimum dimensions of the land pattern rectangles, but that's beyond the scope of this article. The publication IPC-7351, "Generic Requirements for Surface Mount Design and Land Pattern Standard," is probably the best place to start, and is available from IPC.org/7351. The author, Tom Hausherr, has also written many articles on CAD library development. His website (and free software tool) at www.PCBLibraries.com is a good place to learn more.

But the point I want to make here assumes that you have obtained the recommended rectangle size and spacing for the land pattern to be used on the circuit board. What then? Well, you could draw the rectangles as polygons on the top or bottom conductive layer of your circuit board design, place them an appropriate distance apart, and then draw slightly larger rectangles on the soldermask layer, and add lines and text for the silkscreen or legend layer. That's one way to do it, but there are three significant problems with this approach:

1. If you decide to move the component, you would have to move all the individual elements, keeping them in proper relationship to each other.
2. You would have to repeat the process over and over again for each component in the design.
3. Changing the dimensions of any land pattern type would be a tedious process.

There's a better way to do it. Any good CAD software for circuit board design provides a way to enter all of the elements needed for a particular component type once, save it in a common library as a single entity, and then use it as needed for all of the components in the design that have a similar package style. The library could store a default land pattern for an 0805 component, and another one for 0603, 0402, etc. You could even make variations for special cases, and save them with unique names. Although we have been looking at a simple 2-pin

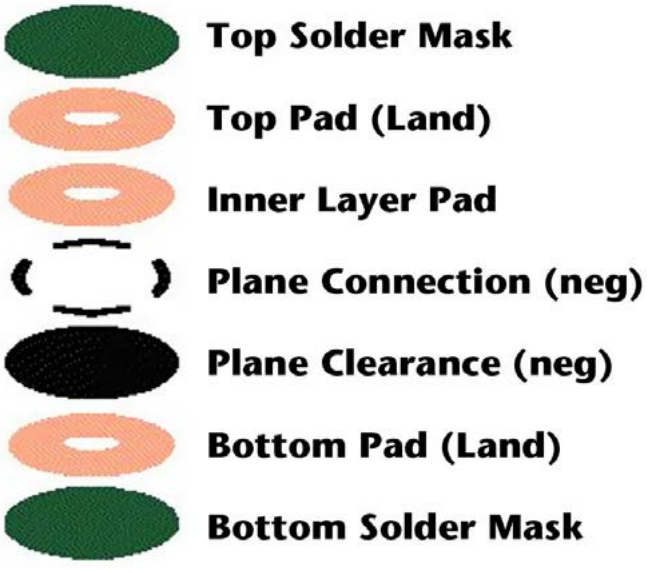
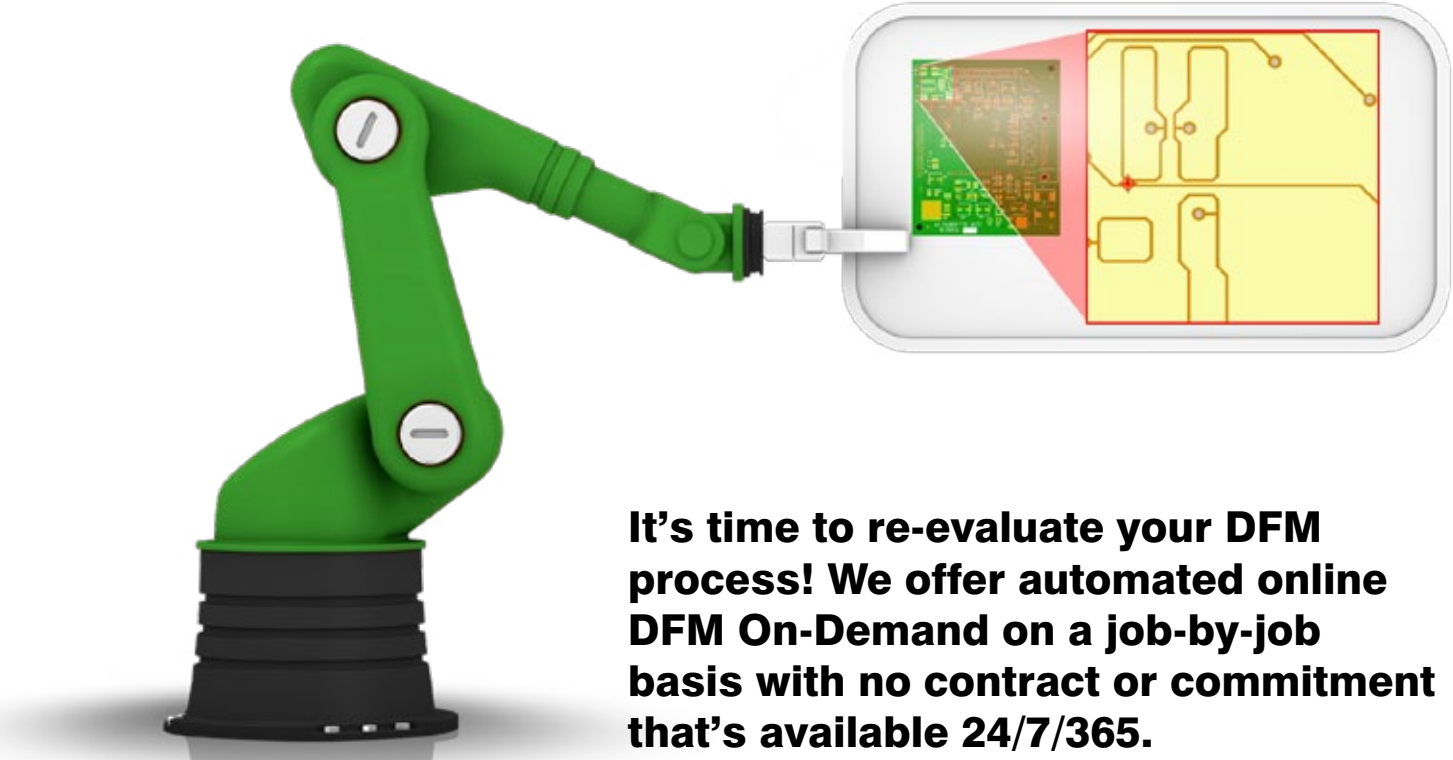


Figure 2: Padstack construction.

Automated On-Demand PCB DFM is here.



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THE CAD LIBRARY *continues*

SMT component for our example, land patterns can be created for all component families (SOICs, BGAs, connectors, etc.). You will be building up a large collection of parts, so it's a good practice to use a consistent library naming convention to stay organized. You may be using your library for many years, so assign a logical name for each unique library entity to make it easier to identify later.

In this manner you can build up your CAD library in advance, available for use in all designs as needed. The ability of the CAD system to permanently store unique library entries opens up some other possibilities:

- The CAD software developers can supply starting libraries installed by default or available separately
- Designers using the same software can share component land patterns
- Library components can be created by outside services on an as-needed basis,
- Large collections are available for purchase from independent developers for specific CAD systems.

Ok, let's take a quick look at the plated holes used in our simple example, because they can also be stored as library entities. Holes of various diameters will be needed for circuit board mounting, for vias (which are plated holes that connect conductive layers together), for leaded components and for SMT components that require holes for additional mounting hardware. **PCBDESIGN**

Jack Olson, CID+, has been designing circuit boards full-time for over 20 years. He would like to thank Tom Hausherr of PCB Libraries for his continuing efforts to systemize and standardize CAD library development. To contact Olson click here.

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Dynamic Supply Chain Visibility Cuts Re-spins

by Lawrence Romine
ALTIUM

SUMMARY: Real-time supply chain information reduces risks, cuts design iterations and accelerates time-to-market. When real-time supply chain data are visible to the design team, designers can reduce or eliminate expensive downstream design changes and re-spins.

Every electronic design project makes compromises between four competing parameters: form factor, performance requirements, delivery time and cost. Supply chain information impacts each of these parameters. Many organizations manage their supply chain externally to the design team and reside in product management or procurement functions. Other companies require their design teams to flesh out the BOM at the beginning of the design process.

The Problem: Limited Supply Chain Visibility

The latter approach focuses on the costly components that heavily influence functionality. In either of these conventional design processes (or their variants), limited or non-existent supply chain visibility by the design team poses a problem. In almost all design processes, the cost parameter remains a static element. Given that the lead-time on components varies as a function of global, industry or other market conditions, static cost data imposes a number of risks. By making real-time supply chain data visible to the design team, designers can reduce or eliminate expensive downstream design changes and re-spins. It's important to consider the consequences of ignoring those risks of limited design team access to supply chain data.

Four Major Risks

Risk 1: Delayed or disrupted supply

As shown in the 2012 Supply Chain Executive Survey (Figure 1), more than 70% of respondents cited delayed or disrupted supplies as the number one risk.

In many organizations, the prototype design team operates as a separate function from their production counterparts. In such an organization, the prototype team focuses on developing a design that fits form and function, free from the con-

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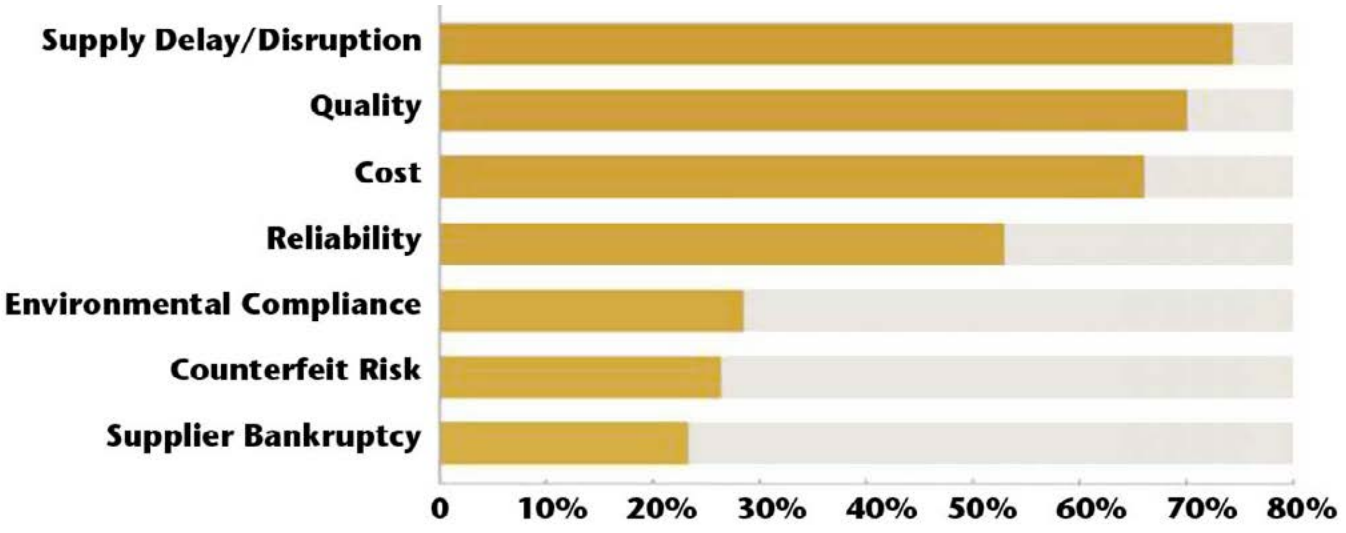

Figure 1: Results from the 2012 Supply Chain Executive Survey.

straints of cost. In this design flow, the production team receives the prototype design and in almost all cases, completely re-spins the design to reduce the costs. Their objective: optimize the BOM, simplify supply chain requirements and meet DFM guidelines.

Prototype and production design teams may be located in different offices, on a different continent, or if outsourcing some of the design process, in a different company. Today, managers realize the difficulty of integrating such a design process. Until recently, senior management usually calculated that the additional design time and labor costs were offset by the larger savings realized during production.

This design process has come under increasing scrutiny due to the raw cost of making design changes after production receives the design. Additionally, the extra design cycle delays time-to-market, imposing a potentially lethal opportunity cost. Combined, the cost of retaining this process has become prohibitive. Careful tracking of out-of-budget design costs often points the finger at a supply chain issue. In most cases, supply chain data is a static element in the process. Static access will almost certainly fail to accurately identify component lead times for one or more components.

Even if lead times were reported, the process still falls down due to the single, static point of access during the design process. An unexpected delay or disruption in supply availability will almost certainly arise, but remain unrecognized. This situation always imposes tremendous costs on the project. The team must either re-spin the design using alternate components or wait for part availability. In either case, the lack of supply chain information penalizes the engineering manager in the form of additional re-spin costs and missed time-to-market objectives.

Risk 2: Component quality

Just less than 70% of respondents to the same survey (Figure 1) reported quality as the second largest risk. Quality risks include functionality issues such as performance variances from published specifications. When a component specified in a design does not meet quality standards, the design cost and time-to-market suffer the consequences. In response, the design team must re-spin all or significant parts of the design to incorporate reliable high-quality components.

Risk 3: Cost

As seen in Figure 1, the third-highest ranking risk, cost, was cited by 65% of respondents. One driver for cost as a risk is the accelerating monthly commodity price volatility since 2006. The standard deviation of monthly price changes for a basket of commodities include gold and

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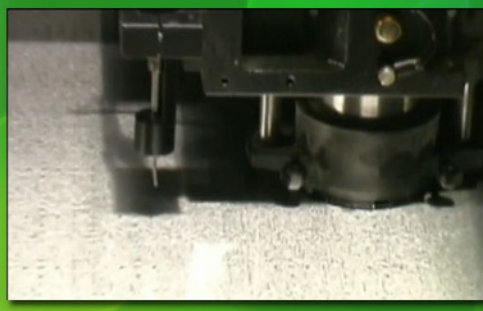

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copper has risen to the 8-9% range from lows near 5% during the late 1990s. Another source, online electronic parts database Octopart, published a chart of global electronic pricing changes for the period June 1, 2011 to June 1, 2012 (Figure 2). Over the 12-month period, overall component pricing ranged from approximately +0.3% in the late summer 2011 to a low of -2.9% early in Q4 2011. Prices then rebounded with an extremely sharp spike up and down, from -1.5% up to +0.3%, and just as quickly dropped in the spring of 2012. This chart sampled approximately 200,000 parts, which tends to average out sharp price increases or declines in individual components. It seems safe to conclude that specific individual components may have experienced much wider fluctuations during this period.

If designers lack access to price data during the actual design process, they will find it nearly impossible to adjust the design based on price data. This lack of exposure leaps up painfully as a cost blow-out at a later point and leads to a design re-spin.

Risk 4: Feature bloating

Also known as "creeping elegance," this risk almost always results in costly misdirection in the design process. Without dynamic cost data, the initial design team may unwittingly specify a challenging part. With open access to dynamic supply chain data, engineering managers can intercept such design misdirection early in the design cycle and make more informed selections. In the process, they will save considerable design time and costs.

Reducing Design Cycle Time to Production

Engineering managers now recognize the necessity of establishing common ground between their design engineers and supply chain management. In most organizations, supply

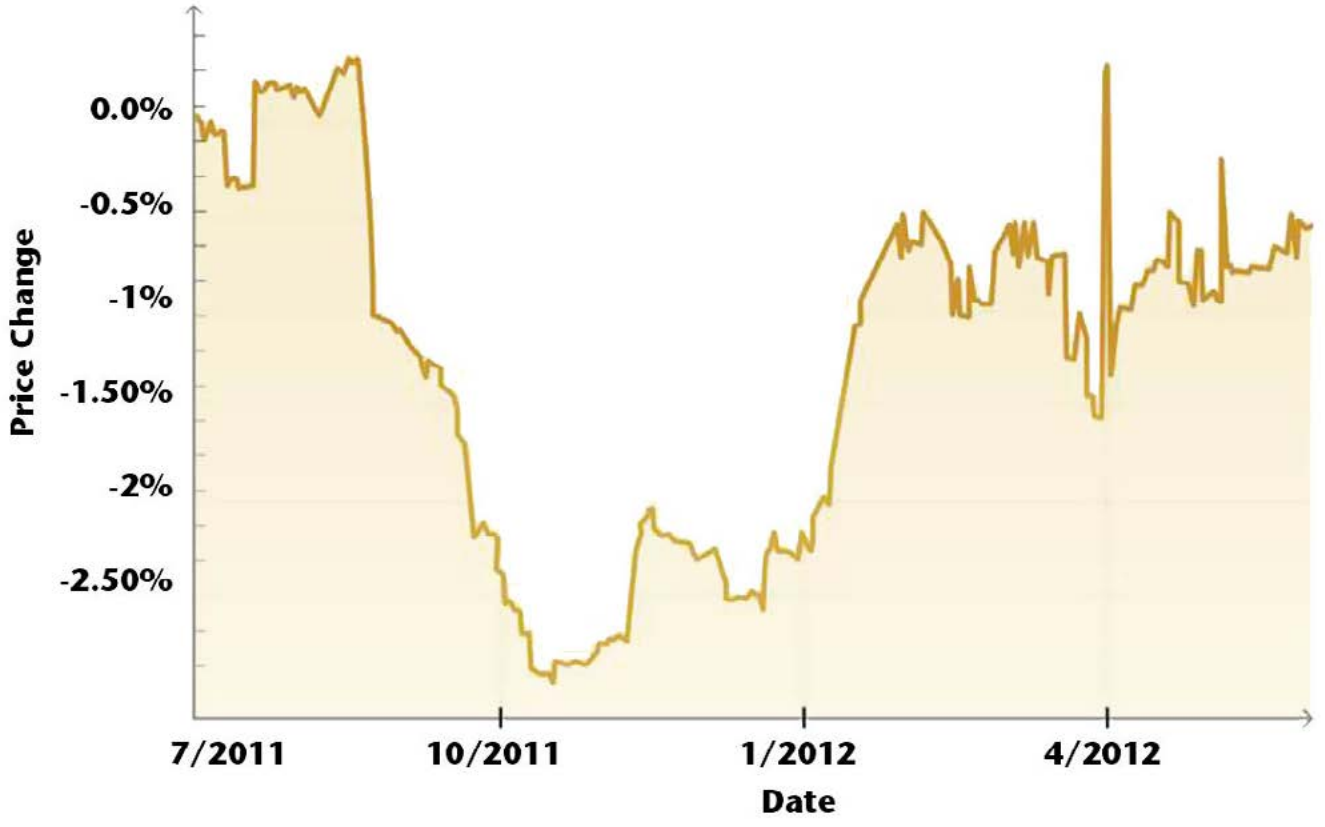


Figure 2: An Octopart chart showing global electronic pricing changes from June 1, 2011 to June 1, 2012.

chain management resides in a finance or administration function. Building the bridge empowers design team members to access dynamic, centralized, real-time, ready-to-use qualified data for every component in the design. To be truly useful, all data necessary to fabricate, load and assemble boards must also be included.

Achieving Component Supply Chain Clarity

Real-time dynamic supply chain data mitigates and minimizes the clash between the classic design parameters that always require trade-offs. With a single view of a real-time BOM, engineering managers can more rapidly balance form factor, performance requirements and time-to-market objectives with cost.

Real-time supply chain information reduces risks, cuts design iterations and accelerates time-to-market. It also identifies any supplier interruptions or delays quickly, reducing the number one risk identified by supply chain managers. With dynamic updates, quality issues such as a change in materials or reliability appear as soon as available. This data also forestalls design misadventures due to "feature bloating" in early stages of the design. Most importantly, access to real-time BOM information empowers design teams to confidently achieve time-to-market objectives. **PCBDESIGN**

References

1. The top three risks were identified in an IHS and Supply & Demand Chain Executive Magazine, 2012 Survey Results and reported in the online presentation "Managing Supply Chain Risk," slide 13. Click here to view.

2. "Generic Quality Risks for Software and Hardware," Rex Black, adapted from Managing the Testing Process, Second Edition, by Rex Black, published by Wiley. Copyright 1999-2002 Rex Black. Available online by clicking here.

3. Ibid., "Supply Chain Risk," slide 9.

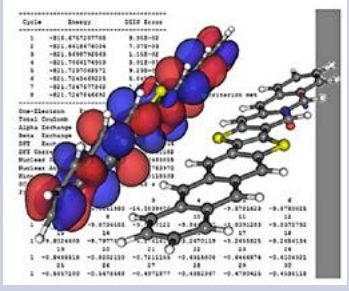
4. "Octopart Trends: Electronic Component Prices (June 2011–June 2012)," available by clicking here.

Lawrence Romine is business development manager for Altium. Following his time in the semiconductor industry, Romine made the move to EDA, where he has held various positions within Altium, including sales, support, business development and marketing.

Harvard Rates Solar Energy Potential of 2.3M New Compounds

The search for more versatile and less expensive materials for solar energy received a boost today as Harvard launched a free database that catalogues the suitability of 2.3 million organic, carbon compounds for converting sunlight into electricity.

IBM's World Community Grid made it possible for the Harvard Clean Energy Project to conduct the most extensive investigation of quantum chemicals ever performed. This has yielded information on millions of new organic compounds, some of which can one day be developed into low cost, highly efficient solar cells. Harvard is open-sourcing the information it compiled on these compounds, which scientists are invited to continue investigating.



Scientists can now use Harvard's resource, www.molecularspace.org, to continue investigating the most promising candidates. It can be used to help advance the development of organic semiconductors, new materials, and ultimately, electricity-generating devices such as solar cells.

Approximately 1,000 of the molecular structures that were characterized in Harvard's research show a potential to convert 11% or more of captured sunlight into electricity, while 35,000 may achieve an efficiency of 10% or more. Most organic cells explored to date only convert 4% to 5% of sunlight into electricity.

Mil/Aero007 News Highlights

Invotec Achieves Nadcap Merit Status at Tamworth Facility

Invotec Group announces that its Tamworth Facility has been awarded Nadcap Merit status for electronics, covering rigid, flex-rigid, and HDI products. Nadcap recognises the facility for its superior performance and commitment to continual improvement in aerospace quality.

New Sales Team to Market Lazer-Tech's Defense PCBs

Jamie Armitage, president and owner of Lazer-Tech, said, "Selling in the high-tech and defense areas requires having sales professionals like Jim Hyde and his team to represent our company. I am extremely confident that Jim and his team will take us to the next level as we continue to focus on the quick-turn market as well as the military and defense sectors."

ZESTRON Renews ITAR Registration

ZESTRON, the globally leading provider of high-precision cleaning products, services, and training solutions, is pleased to announce its renewal of the International Traffic in Arms Regulations (ITAR) registration with the U.S Department of State, Directorate of Defense Trade Controls.

Tin Whiskers Focus of Papers Sought by IPC, CALCE

IPC and CALCE (University of Maryland) have issued a call for papers for the 7th International Symposium on tin whiskers. Sponsored by Lockheed Martin, the symposium will take place November 12–13, 2013. Expert presentations are sought on the full range of tin whiskers theory and practice in every market sector.

Multilayer Technology Achieves 2013 Best of Irving Award

For the fifth consecutive year, the company was selected for the 2013 Best of Irving Award in the printed circuit boards category by the U.S. Commerce Association. The award program recognizes outstanding local businesses throughout the country.

Cofan Secures UL Listing for Aismalibar/Cobritherm

Cofan has received its UL listing for Aismalibar/Cobritherm thermally conductive IMS/prepreg. The company is now certified to use the UL stamp on Aismalibar's Cobritherm Alcup-G, Alcup, and HTC materials.

Microtek Names Shepherd VP of Operations

Microtek Laboratories, an independent test laboratory, has announced the promotion of Russ Shepherd to the position of vice president of operations. Shepherd has worked for the company for more than 25 years and has been an integral part of its growth and success since first being hired in 1987.

Ground Robot Market to Reach $12.0 Billion by 2019

Military ground robot market growth comes from the device marketing experts inventing a new role as technology poised to be effective at the forefront of fighting terrorism. Markets at $4.5 billion in 2013 are expected to reach $12.0 billion by 2019.

Global Military Radar Systems Market to Hit $8.6B in 2013

In 2013, the global military radar systems market is evaluated at nearly US $8.6 billion. Developed countries lead the overall market in terms of radar technological developments.

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DFP: Yield Drives HDI Profit

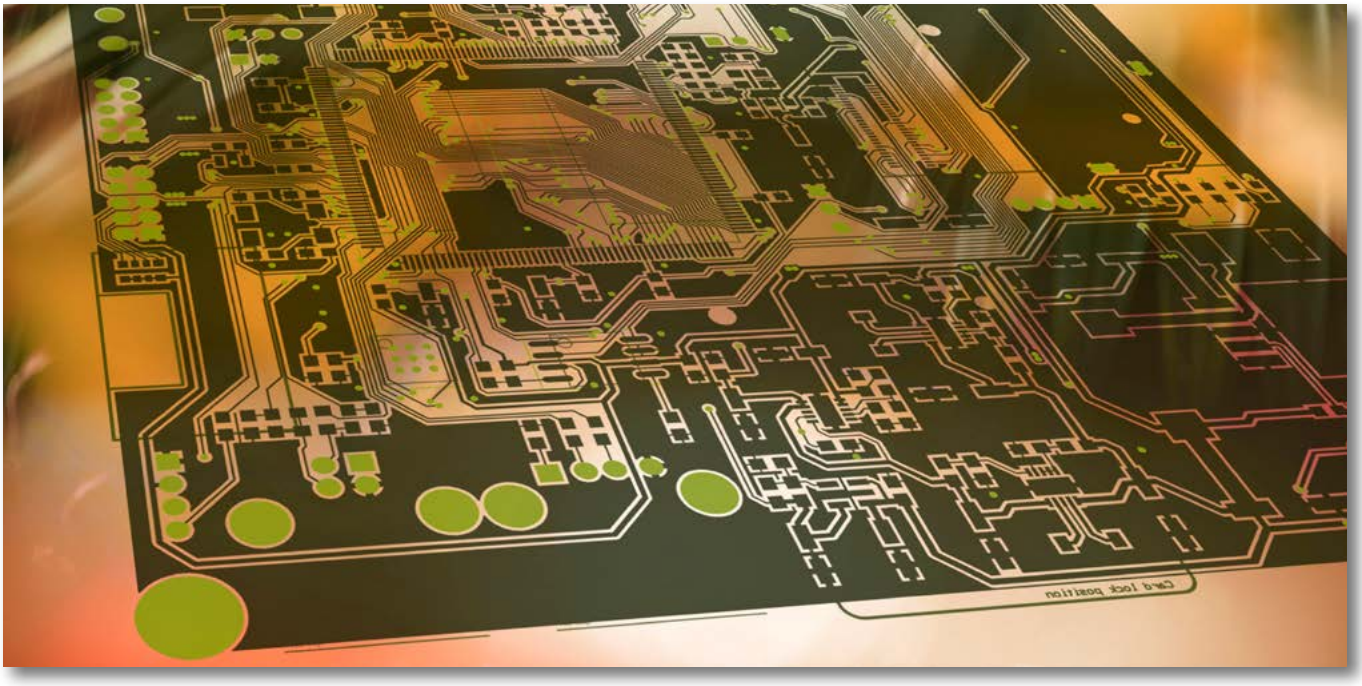
by Amit Bahl
SIERRA CIRCUITS

The first step toward designing a printed circuit board is to identify the least expensive materials that satisfy the electrical and environmental requirements of the application. Data sheets and price lists for materials provide basic guidance, but offer no clue about how much a board would actually cost to fabricate using one material versus another. Often, data sheets will show two materials to have nearly identical characteristics, but one may be relatively more or less challenging to process than another, especially for HDI technology. Their raw prices have little correlation to their ease of manufacture and consequently to board yield, and it is manufacturing yield that drives profits.

Broadly, the manufacturing yields of HDI designs for which a material is specified are determined by whether a material is dimensionally stable, susceptible to or resistant to copper migration such as conductive anodic filament (CAF) growth, able to withstand multiple laminations, and able to be laser drilled with consistent good results.

A circuit whose response remains relatively flat over its frequency range will faithfully propagate signals without distortion. The dielectric constant (Dk or E_r) of a material decreases as frequency increases. High-speed digital signals involve broad bands of frequencies and thereby are subject to distortion caused by impedance variations resulting from changes in the Dk of board materials with frequency. Changes in the dissipation factor (Df) of board materials with frequency degrade signal integrity as well. Materials whose Dk and Df are low and vary little across the frequency domain of a circuit propagate signals faster and maintain signal integrity better than materials with higher Dk and Df.

Suppose you've ruled out dielectrics in the FR-4 category because their Dk and Df values are too high and vary too much over the signal spectrum of your circuit. Suppose as well that your board will incorporate several high-speed devices in BGAs, each with a dense pin matrix that will require via-in-pad routing. Your design will therefore involve blind microvias and



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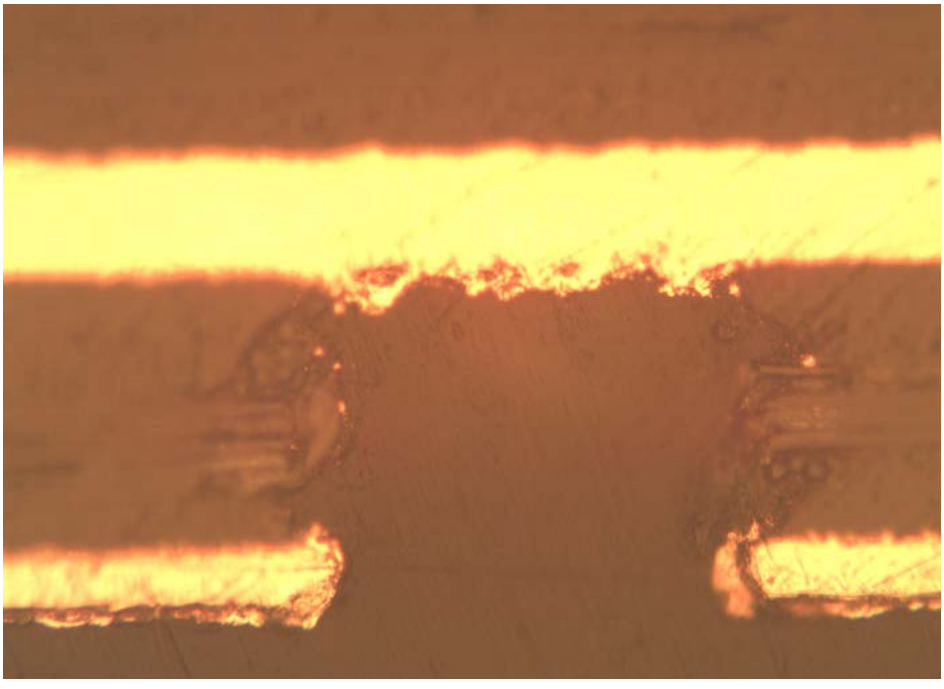

Figure 1: The resin in N4000-13 SI (3 mil core in photograph) tends to ablate at a much faster rate than the glass reinforcement during laser drilling, relative to Megtron 6, leaving fibers that protrude into holes and interfere with the Cu deposit.

require a material thin enough that the aspect ratio of those laser-drilled vias does not exceed 0.8:1 or plating could become difficult. Remember, at a given Dk, the thinner the substrate, the narrower the traces must be to maintain a 50 ohm impedance. You'll favor materials that have a low Dk so trace width can be wide enough to be easily manufactured and provide the necessary impedance value.

Let's say a Dk under 3.7 at 1 GHz is acceptable and you've decided Isola FR408HR, Nelco N4000-13 SI, and Panasonic Megtron 6 are prospects, based on their data sheets. I choose these three materials, which my fabrication company deals with routinely, to illustrate my point about hidden manufacturing issues, yield, and ultimate PCB cost.

FR408HR has a higher dielectric constant and higher loss factor than both N4000-13 SI and Megtron 6, but it is cheaper in price. The Nelco 4000-13 series of materials, and in particular N4000-13 SI, have excellent electrical properties for high-speed digital applications. The SI material—SI for signal integrity—is based on a glass cloth specially formulated to have a very low Dk over a wide frequency range that is closely matched to the Dk of its resin. Megtron 6 incorporates a unique low-Dk fabric known as flat glass. Unlike FR408 HR and N4000-13 SI, in which resin resides throughout the glass fabric weave, its resin is essentially a "butter coat" evenly distributed across the woven flat-glass fabric surface. Megtron 6 has a slightly higher average Dk value than Nelco 4000-13 SI, from 1 GHz to 10 GHz, but a much lower Df. It is somewhat more expensive than the Nelco material and is often used for RF and microwave applications, as well as for high-speed digital circuits.

The three products are comparable on paper (all are widely employed for high-speed digital PCBs), but they have quite different manufacturing characteristics when used for HDI board designs. There are three key qualities a material must possess for HDI fabrication. First, it must be dimensionally stable, a quality that, of course, applies to non-HDI construction as well. All materials shrink and stretch to some extent during manufacturing processes, and patterning must be scaled to compensate, which is not an issue provided the material movement is predictable. Second, the material must be easily machinable: For HDI that means it can be laser drilled without problems. Third, a material must be able to survive multiple laminations. Let's restrict this comparison of manufacturability to laser drilling, with regard to the three materials.

The word drill is really a misnomer to describe how a laser makes holes. A better term would be vaporization. Highly concentrated energy is directed in a focused beam on a specific area, which is absorbed by the material until it

vaporizes. The energy must be carefully controlled to ablate material to form a hole without destroying the landing pad beneath. However, dielectric constituents absorb energy at different rates, and it is in this respect that N4000-13 SI, FR408HR, and Megtron 6 differ in manufacturability.

Let me interject a disclaimer. Though my company has extensive experience with the three materials, that experience isn't quantified and therefore must be considered subjective. There's no bias toward one rather than the others, except for HDI from manufacturing experience. We'll build whatever a customer wants, if it can be constructed. The point to bear in mind is simply this: If a board is challenging to build in limited, prototype quantities, it will be no less challenging to manufacture in production runs. To repeat, yield drives profit.

Figure 2: Plating was compromised in this microvia in FR408HR because glass bundles extend from the hole wall.

My company has found that achieving clean laser-drilled holes in the Nelco material and in FR408HR requires more effort compared to creating them in Megtron 6. The resin in the Nelco fabric burns off at a much different rate than the glass fibers and too much energy is required to consume all the fibers in the hole without compromising the surrounding dielectric and the landing pad itself. FR408HR is less prone to have glass fibers protrude from hole walls than is N4000-13 SI but is less predictable in that respect. Glass bundles extend in perhaps only 5% of the holes but such inconsistency itself complicates processing. The flat-glass fabric of Megtron 6 can be ablated cleanly by contrast to the other two materials, in our experience.

Nelco is continually investigating resin formulations, glass, and fabric constructions that would improve the manufacture of HDI architectures. The firm recently introduced a new material, N4800-20 SI, which it recommends in place of N4000-13 SI for HDI manufacture. My company is evaluating that material and anticipates better results.

The upshot of all this is that you should consult your board manufacturer at the outset of design to identify materials that would provide the optimum balance of price, manufacturability, and performance based on your construction. I'll dedicate this column as the first installment regarding materials and manufacturability. The next one will regard materials with the highest electrical performance for digital high-speed circuits, and for RF and microwave applications. **PCBDESIGN**

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TOP TEN

News Highlights from PCBDesign007 this Month

① Agilent Partners with Mentor on FPGA Development Kit

Agilent Technologies has introduced the U5340A FPGA development kit, powered by a custom Mentor Graphics design engine, for high-speed digitizers. The kit enables customers to deploy advanced, real-time signal processing into the FPGAs on board Agilent high-speed digitizers.

② Quadra Receives Zuken's Distributor of the Year Award

Zuken has recently awarded its European CADSTAR Distributor of the Year Award to recession-beating reseller Quadra Solutions for the fifth time. Quadra Solutions had a record year in 2012-13, growing 20% on the previous year and achieving ISO 9001 accreditation.

③ IPC to Hold ITAR/EAR Webinar Series in July

This July, IPC will offer an ITAR/EAR webinar series, bringing the latest information on current changes, possible upcoming changes, and the impact these regulations may have on the supply chain. Such regulations specifically address PCBs and PCB designs and affect the entire electronics supply chain, from OEMs to board manufacturers and designers.

④ Millitech Selects Agilent 3D EM Simulation Tools

The integration of ADS and EMPro enables engineers to simultaneously optimize linear and nonlinear aspects of their designs. This is important when designing nonlinear devices, such as mixers, multipliers and various passive devices.

5 AWR Releases New eBook

AWR Corporation announces a new eBook, "RF Electronics: Design and Simulation," which is available free of charge to students, graduates, professors, and industry professionals through the company's new Professors in Partnership web portal.

6 DesignCon 2014 Seeks Technical Papers

The organizers of DesignCon 2014 are now inviting the industry to submit abstracts for technical papers and tutorials for the upcoming event next year.

7 Ucamco Proposes to Extend Gerber Format

The company proposes to extend the Gerber Format with attributes to store the extra information associated with the image. This will allow CAD systems to not only transfer the images to a CAM system in a standard and machine-readable way, but also this necessary extra information.

8 Polar Upgrades Atlas Si SET2DIL Test System

The Polar Atlas Si insertion-loss test system enables PCB fabricators to achieve multi-GHz performance using the most economic PCB laminates and enables accurate testing to be carried out, in a fraction of the time of traditional frequency domain testing, by either QA or production line operators.

9 Zuken Enhances Design Productivity & IP Management

Zuken addresses the needs of global design teams and their downstream partners with new versions of its Design Force and Design Gateway software, part of the CR-8000 multi-board design solution.

10 DownStream Web Event Date Change: July 25

Discover how to ease the creation, distribution and management of DownStream's PCB documentation during this technical webinar. The event takes place Thursday, July 25. Note the date change.

events

PCB Design Events

IPC Complete Calendar of Events

SMTA Calendar of Events

NANOTEXNOLOGY 2013
July 6–13, 2013
Thessaloniki, Greece

6th International Symposium on Flexible Organic Electronics (ISFOE13)
July 8–11, 2013
Thessaloniki, Greece

Printed Electronics Asia 2013
July 9–10, 2013
Tokyo, Japan

Semicon West
July 9–11, 2013
San Francisco, California, USA

ITAR and EAR: How Will Export Control Reform Impact Your Business?
July 9, 16 and 23, 2013
Online Webinar

Ohio Valley Expo & Tech Forum
July 11, 2013
Cleveland, Ohio, USA

Surface Mount Rework of BGA, PoP, CSP & QFN Components
July 11, 2013
Dublin, Ireland

Techno-Frontier 2013
July 17–19, 2013
Tokyo, Japan

ISMSE 2013
July 27–29, 2013
Singapore

Microscopy & Microanalysis 2013
August 4–8, 2013
Indianapolis, Indiana, USA

Philadelphia Expo & Tech Forum
August 15, 2013
Cherry Hill, New Jersey, USA

NEPCON South China
August 27–29, 2013
Shenzhen, China

IPCA EXPO 2013
August 29–31, 2013
Gujarat, India

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Next Month in *The PCB Design Magazine*

It's not a question of whether you'll encounter signal integrity problems. It's a question of when. In the August issue of *The PCB Design Magazine,* the industry's top SI experts weigh in with the latest tips, tricks and techniques for achieving signal integrity.